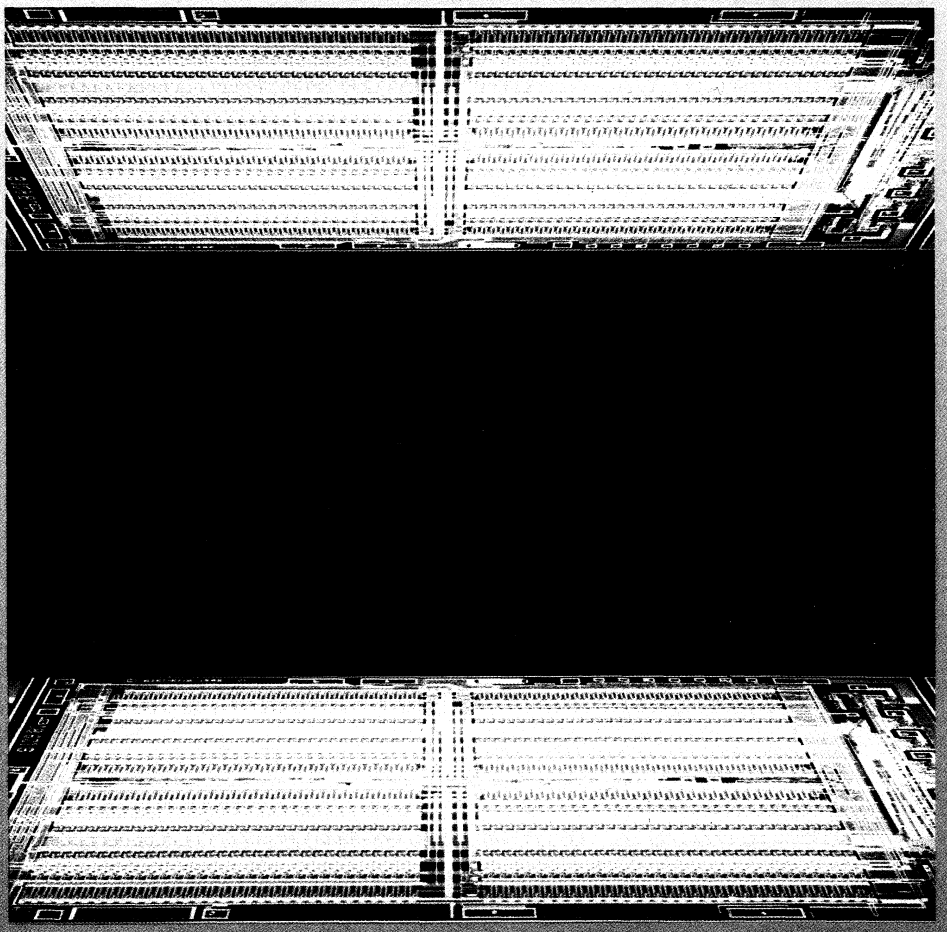
SIEMENS

ICs for Industrial Electronics

Data Book 1989/90



ICs for Industrial Electronics

Data Book 1989/90

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SMD = Surface Mounted Device

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1.2 Types in application-oriented order

Summary of Types

General Information

2.1 Type-Designation Code for ICs

IC type designations are based on the European Pro Electron system. The code system is explained in the Pro Electron brochure D 15*), edition 1988.

*) Available from Pro Electron, Avenue Louise, 430 (B.12)
B-1050 Brussels, Belgium.

2.2 Mounting Instructions

2.2.1 Plastic Package

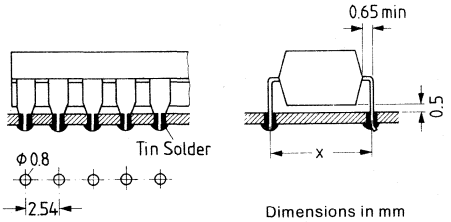
The pins of the cases are bent downwards by an angle of 90° and fit into holes with a diameter of between 0.7 and 0.9 mm spaced 2.54 mm apart. The dimension x is given in the corresponding drawing.

The bottom of the package will not touch the PC board after insertion because the pins have shoulders just below the package **(see figure 1).**

After insertion of the package into the PC board it is advisable to bend the ends of two pins at an angle of approx. 30° to the board so that the package does not have to be pressed down during soldering. Plastic packages are soldered on that side of the PCB facing away from the package.

The maximum permissible soldering temperature is 350 °C (max. 3 s) for manual soldering and 260 °C (max. 10 s) for dip soldering and wave soldering.

Figure 1



Dimensions in mm

2.2.2 Power Package with 5, 7, or 9 Pins

Power packages generally have wider pins than stated in paragraph 2.2.1, meaning that the hole diameter on the PCB must be between 1.1 and 1.8 mm. If the pins are bent, there should be no stress between the pins and the package. The minimum distance between the package and the bending point is 2 mm.

Refer to paragraph 2.2.1 for soldering temperatures.

2.2.3 Plastic Packages (P-DSO and PL-CC) for Surface Mounting (SMD)

Iron soldering:	soldering temperature 350 °C for max. 3 s; minimum distance between package and soldering point 1.5 mm package temperature max. 150 °C; no mechanical stress on the pins
Vapor phase soldering:	soldering temperature 215 °C, max. soldering time 40 s, 2 x.
Wave soldering:	soldering temperature 260 °C, max. soldering time 8 s. (pins and package are dipped into the tin bath)

2.2.4 Storage, Pretreatment for Processing of ICs in PL-CC-68 Packages

The components are to be stored in a dry place. For soldering methods which may lead to a thermal shock stress (e.g. vapor phase soldering) it is recommended to dry the ICs in PL-CC package at 125 °C for a period of 24 hours.

2.2.5 Other Points to Note

Ensure that no current is able to flow between the solder bath or soldering iron and the PCB. It is advisable to ground the pins that are to be soldered as well as the solder bath or soldering iron.

When they are being prepared and inserted in a PCB, circuits should be protected against static charging. Under no circumstances may the components be removed or inserted whilst the operating voltage is switched on.

The increase in chip temperature during the soldering process results in a temporary increase in electrostatic sensitivity of integrated circuits. Special precautions should therefore be taken against line transients, e.g. through the switching of inductances on magnetic chutes, etc.

2.2.6 MIKROPACK (SMD)

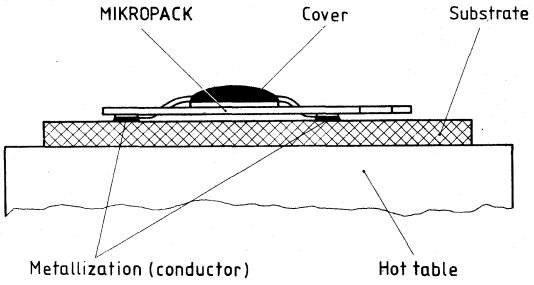
MIKROPACK components are delivered on film reels.

Mounting Suggestions

a) We recommend vapor phase soldering: soldering temperature 215 °C, soldering time max. 40 s.

b) For prototypes and small quantities (up to approximately 50.0 items/y), the hot table soldering method can also be used **(figure 2)**.

Figure 2



Required Equipment and Accessories

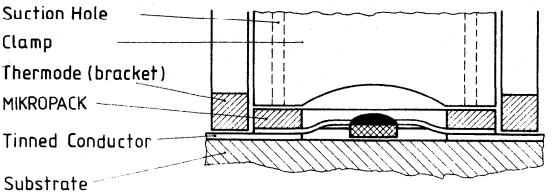
- cutting device
- hot table, temperature regulated (e.g. Weld-Equip, Unitek)
- stereo microscope (e.g. Wild, Zeiss, magnification 6...40 times)
- substrate material: epoxy resin; hard paper; ceramic (thick thin film)

Soldering Data

- soldering temperature: 210 °C max.
- solder coating on substrate: Pb/Sn (e.g. 60/40) wave-tinned or electrodeposited
- soldering time: approx. 10 s
- flux: e.g. colophony, dissolved in alcohol
- cleaning agents (as required): e.g. Freon TP-35, TE, TF

c) For large quantities (e.g. more than 50.0 items/y) thermode soldering is also suitable **(figure 3)**.

Figure 3



Required Equipment

- soldering equipment (e.g. Weld-Equip, Farco, Jade)
- substrate material: epoxy resin; hard paper; flexible materials, e.g. polyamide

Soldering Data

- soldering temperature: 220 °C max.
- solder coating on the substrate: Pb/Sn (e.g. 60/40), wave-tinned or electro-deposited
- soldering time: approx. 10 s
- flux: e.g. colophony dissolved in alcohol
- cleaning agents (as required); e.g. Freon TP-35, TE, TF

2.3 Processing Guidelines for ICs

Integrated circuits (ICs) are electrostatic-sensitive (ESS) devices. The demand for greater packing density has led to smaller structures on semiconductor chips, with the result that today every IC, whether bipolar, MOS, or CMOS, has to be protected against electrostatics.

MOS and CMOS devices generally have integrated protective circuits and it is virtually impossible for them to be destroyed by purely static electricity. On the other hand, there is acute danger from electrostatic discharges (ESD).

Of the multitude of possible sources of discharge, charged devices should be mentioned in addition to charged persons. Low-resistive discharges can produce peak powers amounting to kilowatts.

For the protection of devices the following principles should be observed:

a) Reduction of charging voltage, below 200 V if possible.
   Means which are effective here are an increase in relative humidity to $\geq 60\%$ and the replacement of highly charging plastics by antistatic materials.
b) With every kind of contact with the device pins a charge equalization is to be expected. This should always be highly resistive (ideally $R = 10^6$ to 10^9 Ω).

All in all this means that ICs call for special handling, because uncontrolled charges, voltages from ungrounded equipment or persons, surge voltage spikes and similar influences can destroy a device. Even if devices have protective circuits (e.g. protective diodes) on their inputs, the following guidelines for their handling should nevertheless be observed.

2.3.1 Identification

The packing of ESS devices is provided with the following label by the manufacturer: 

2.3.2 Scope

The guidelines apply to the storage, transport, testing, and processing of all kinds of ICs, equipped and soldered circuit boards that comprise such components.

2.3.3 Handling of Devices

1. ICs must be left in their containers until they are processed.
2. ICs may only be handled at specially equipped work stations. These stations must have work surfaces covered with a conductive material of the order of 10^6 to 10^9 Ω/cm.
3. With humidity of $> 50\%$ a coat of pure cotton is sufficient. In the case of chargeable synthetic fibers the clothing should be worn close-fitting. The wrist strap must be worn snugly on the skin and be grounded across a resistor of 50 to 100 kΩ.

4. If conductive floors, $R = 5 \times 10^4$ to 10^7 Ω are provided, further protection can be achieved by using so-called MOS chairs and shoes with a conductive sole ($R \approx 10^5$ to 10^7 Ω).
5. All transport containers for ESS devices and assembled circuit boards must first be brought to the same potential by being placed on the work surface or touched by the operator before the individual devices may be handled. The potential equalization should be across a resistor of 10^6 to 10^8 Ω.
6. When loading machines and production devices it should be noted that the devices come out of the transport magazine charged and can be damaged if they touch metal, e.g. machine parts.

   Example 1) conductive (black) tubes.
   The devices may be destroyed in the tube by charged persons or come out of the tube charged if this is emptied by a charged person.
   Conductive tubes may only be handled at ESS work stations (high-resistance work-station and person grounding).

   Example 2) anti-static (transparent) tubes.
   The devices cannot be destroyed in the tube by charged persons (there may be a rare exception in the case of custom ICs with unprotected gate pins). The devices can be endangered as in 1) when the tube is emptied if the latter, especially at low humidity, is no longer sufficiently anti-static after a long period of storage (> 1 year).

   In both cases damage can be avoided by discharging the devices across a grounded adapter of high-resistance material ($\approx 10^6$ to 10^8 Ω/cm) between the tube and the machine.

   The use of metal tubes – especially of anodized aluminum – is not advisable because of the danger of low-resistance device discharge.

2.3.4 Storage

ESS devices should only be stored in identified locations provided for the purpose. During storage the devices should remain in the packing in which they are supplied. The storage temperature should not exceed 60 °C.

2.3.5 Transport

ESS devices in approved packing tubes should only be transported in suitable containers of conductive or longterm anti-static-treated plastic or possibly unvarnished wood. Containers of both high-charging plastic or very low-resistance materials are unsuitable.

Transfer cars and their rollers should exhibit adequate electrical conductivity ($R < 10^6$ Ω). Sliding contacts and grounding chains will not reliably eliminate charges.

2.3.6 Incoming Inspection

In incoming inspection the above guidelines should be observed. Otherwise any right to refund or replacement if devices fail inspection may be lost.

2.3.7 Material and Mounting

1. The drive belts of machines used for the processing of the devices, in as much as they come into contact with them (e.g. bending and cutting machines, conveyor belts), should be treated with anti-static spray (e.g. anti-static spray 100 from Kontaktchemie). It is better, however, to avoid the contact completely.
2. If ESS devices have to be soldered or desoldered manually, soldering irons with thyristor control may not be used. Siemens EMI-suppression capacitors of the type B 81711-B31...-B36 have proven very effective against line transients.
3. Circuit boards fitted and soldered with ESS devices are always to be considered as endangered.

2.3.8 Electrical Tests and Application Circuit

1. The devices should be processed with observation of these guidelines. Before assembled and soldered circuit boards are tested, remove any shorting rings.
2. The sockets or integrated circuits must not be conducting any voltage when individual devices or assembled circuit boards are inserted or withdrawn, unless works' specifications state otherwise. Ensure that the test devices and power supplies do not produce any voltage spikes, either when being turned on and off in normal operation or if the power fuse blows or other fuses respond.
3. When supplying bipolar integrated circuits with current, the negative voltage ($-V_S$ or GND) has first to be connected. In general, an interruption of this potential during operation is not permissible.
4. Signal voltages may only be applied to the inputs of ICs when or better after the supply voltage is turned on. They must be disconnected when or better before the supply voltage is turned off.
5. Power supplies of integrated circuits are to be blocked as near as possible at the supply terminals of the IC. With bipolar ICs it is recommendesd to use a low-inductance electrolytic capacitor or at least a paralleled ceramic capacitor of 100 nF to 470 nF for example.

   Using ICs with high output currents, the necessary value of the electrolytic capacitor must be adapted to the test or application circuit. Transient behavior and dynamic output resistance of the power supplies, line inductances in the supply and load circuit and in particular inductive loads or motors have to be considered. When switching off line inductances of inductive loads, the stored power has to be consumed externally, unless otherwise specified (e.g. by an electrolytic capacitor, diodes, Z diodes or the power supply). Also a switching off of the supply voltage prior to the load rejection should be taken into account.
6. ICs with low-pass character of the output stages (e.g. PNP drivers or PNP/NPN end stages), normally need an additional external compensation at the output. This applies particularly to complex loads. The output of AF power amplifiers is compensated by the Boucherot element. In individual cases, bridge circuits

only need a capacitance for bypassing the load. Depending on the application it is, however, also recommended to connect one capacitor from each output to ground.

7. Observe any notes and instructions in the respective data books.

2.3.9 Packing of Assembled PC Boards or Flatpack Units

The packing material should exhibit low volume conductivity:
$10^5\ \Omega/cm < \rho < 10^{10}\ \Omega/cm$.

In most cases – especially with humidity of > 40% – this requirement is fulfilled by simple corrugated board. Better protection is obtained with bags of conductive polyethylene foam (e.g. RCAS 1200 from Richmond of Redlands, California).

One should always ensure that boards cannot touch.

In special cases it may be necessary to provide protection against strong electric fields, such as can be generated by conveyor belts for example. For this purpose a sheath of aluminum foil is recommended, although direct contact between the film and the PCB must be avoided. Cardboard boxes with an aluminum-foil lining, such as those used for shipping our devices, are available from Laber of Munich.

2.3.10 Ultrasonic Cleaning of ICs

The following recommendation applies to plastic packages. For cavity packages (metal and also ceramic) separate regulations have to be observed.

Freon and isopropyl alcohol (trade name: propanol) can be used as solvents. These solvents can also be used for plastic packages because they do not eat into the plastic material.

An ultrasonic bath in double halfwave operation is advisable because of the low component stress.

The ultrasonic limits are as follows:

sound frequency	f	> 40 kHz
exposure	t	< 2 min
alternating sound pressure	p	< 29 kPa
sound power	N	< 0.5 W/cm²/liter

2.4 Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A = 25\,°C$ and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

2.5 Quality Assurance

2.5.1 Quality Assurance System

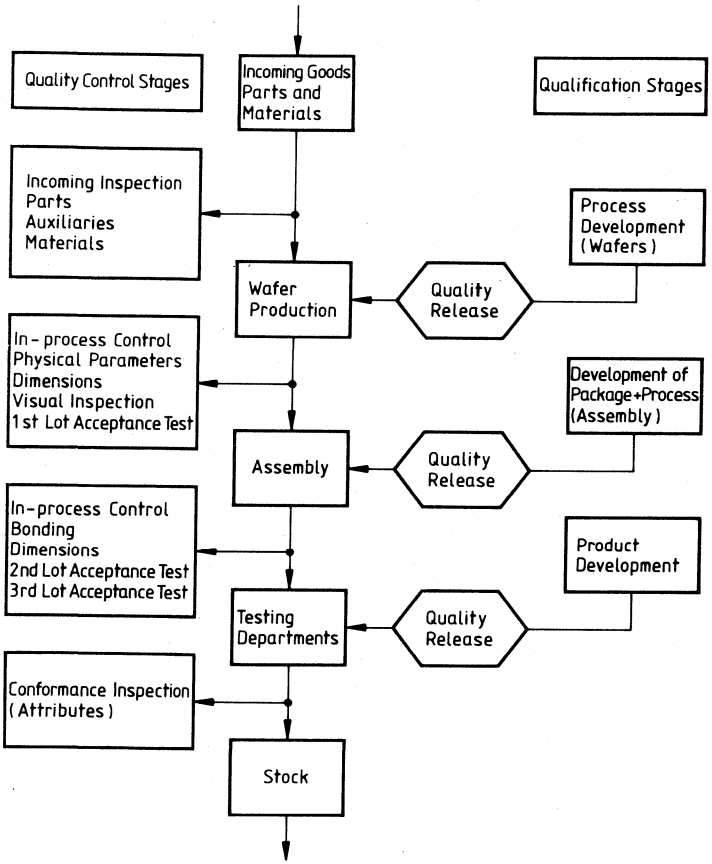
The high quality and reliability of integrated circuits from Siemens is the result of a carefully arranged production which is systematically checked and controlled at each production stage.

The procedures are subject to a quality assurance system; full details are given in the brochure 'Siemens Quality Assurance – Integrated Circuits' (SQS IC).

Figure 1 shows the most important stages of the "SQS IC". A quality assurance (QA) department which is independent of production and development, is responsible for the selected control measures, acceptance procedures, and information feedback loops. This department has state-of-the-art test and measuring equipment at its disposal, works according to approved methods of statistical quality control, and is provided with facilities for accelerated life and environmental tests used for both qualification and routine monitoring tests.

The latest methods and equipment for preparation and analysis are employed to achieve continuity of quality and reliability.

Figure 1


Quality Control Stages
Incoming Goods Parts and Materials
Qualification Stages
Incoming Inspection Parts Auxiliaries Materials
Process Development (Wafers)
Wafer Production
Quality Release
In-process Control Physical Parameters Dimensions Visual Inspection 1st Lot Acceptance Test
Development of Package+Process (Assembly)
Assembly
Quality Release
In-process Control Bonding Dimensions 2nd Lot Acceptance Test 3rd Lot Acceptance Test
Product Development
Testing Departments
Quality Release
Conformance Inspection (Attributes)
Stock

2.5.2 Conformance

Each integrated circuit is subjected to a final test at the end of the production process. These tests are carried out by computer-controlled, automatic test systems because hundreds of thousands of operating conditions as well as a large number of static and dynamic parameters have to be considered. Moreover, the test systems are extremely reliable and reproducible. The quality assurance department carries out a final check in the form of a lot-by-lot sampling inspection to additionally ensure this minimum percent defectives as well as the acceptable quality level (AQL). Sampling inspection is performed in accordance with the inspection plans of DIN 40080, as well as of the identical MIL-STD-105 or IEC 410.

The table shows the results of such sampling inspections performed with hundreds of thousands of ICs during 1987. These results correspond to the average outgoing quality (AOQ), and are specified as defectives per million (DPM).

	Inoperatives AOQ (DPM)	Sum of electrical defectives AOQ (DPM)	Sum of mechanical defectives AOQ (DPM)
LSI/VLSI ≥ 1000 gate functions	90	144	250

2.5.3 Reliability

2.5.3.1 Measures Taken during Development

The reliability of ICs is already considerably influenced at the development stage. Siemens has, therefore, fixed certain design standards for the development of circuit and layout, specifying e.g. minimum width and spacing of conductive layers on a chip, dimensions and electrical parameters of protective circuits for electrostatic charge, etc. An examination with the aid of carefully arranged programs operated on large-scale computers, guarantees the immediate identification and elimination of unintentional violations of these design standards.

2.5.3.2 In-Process Control during Production

The manufacturing of integrated circuits comprises several hundred production steps. As each step is to be executed with utmost accuracy, the in-process control is of outstanding importance. Some processes require more than a hundred different test measures. The tests have been arranged such that the individual process steps can be reproduced continuously.

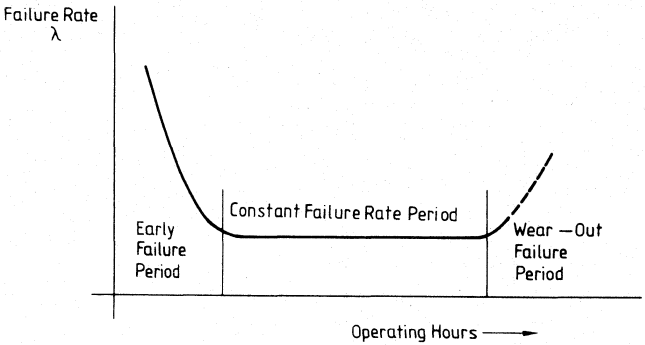
The decreasing failure rates reflect the never ending effort in this direction; in the course of the years they have been reduced considerably despite an immense rise in the IC's complexity.

So in 1987 the typical random failure rates estimated for accelerated life tests with almost 2 million ICs of all complexities are found to be around 80 fit.

2.5.3.3 Reliability Monitoring

The general course of the IC's failure rate versus time is shown by a so-called "bathtub" curve **(figure 2)**. The failure rate has its peak during the first few operating hours (early failure period). Afgter the early failure period has decayed, the "constant" failure rate period starts during which the failures may occur at an approximately uniform rate. This period ends with a repeated rise of the curve during the wear-out failure period. For ICs, however, the latter period usually lies far beyond the service life specified for the individual equipment.

Figure 2



Reliability tests for ICs are usually destructive examinations. They are, therefore, carried out with samples. Most failure mechanisms can be accelerated by means of higher temperatures. Due to the temperature dependence of the failure mechanisms, it is possible to simulate future operational behavior within a short time by applying high temperatures; this is called life test.

The acceleration factor B for the life test can be obtained from the Arrhenius equation

$$B = \exp\left(\frac{E_A}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)$$

where T_2 is the temperature at which the life test is performed, T_1 is the assumed operating temperature, and k is the Boltzmann constant.

Important for factor B is the activation energy E_A. It lies between 0.3 and 1.3 eV and differs considerably for the individual failure mechanisms.

For all Siemens ICs, the reliability data from life tests is converted to an operating temperature of $T_A = 40\,°C$, assuming an average activation energy of 0.4 eV. The acceleration factor for life tests at 125 °C is thus 24, compared with operational behavior. This method considers also failure mechanisms with low activation energy, i.e. which are only slightly accelerated by the temperature effect.

Various reliability tests are periodically performed with IC types that are representative of a certain production line – this is described in the brochure "SQS IC". Such tests are e.g. humidity test at 85 °C and 85% relative humidity, pressure cooker test, as well as life tests up to 1000 hours and more. Test results are available in the form of summary reports.

2.6 Logic Functions and Symbols

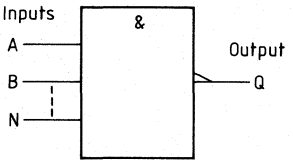
in accordance with DIN 40900, part 12

Logic Levels

For digital microcircuits, the two possible binary states are designated L (low) and H (high). The values of the L range are closer to $-\infty$ and those of the H range closer to $+\infty$. Similarly, the index A applies to the upper limit value (closer to $+\infty$) and index B to the lower limit value (closer to $-\infty$).

Gate Symbols

NAND



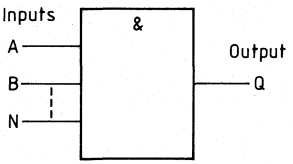
Truth table of NAND with two inputs.

Inputs A	Inputs B	Output Q
L	L	H
L	H	H
H	L	H
H	H	L

Logic function: $Q = \overline{A \wedge B \quad \ldots \wedge N}$

Definition: an L signal will only be present at the output if A and B and . . . and N show an H signal.

AND



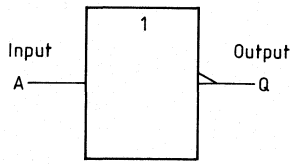
Truth table of AND with two inputs.

Inputs A	Inputs B	Output Q
L	L	L
L	H	L
H	L	L
H	H	H

Logic function: $Q = A \wedge B \quad \ldots \wedge N$

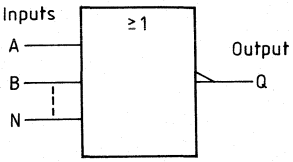
Definition: an H signal will only be present at the output if A and B and . . . and N show an H signal.

Inverter



Logic function: $Q = \overline{A}$

NOR

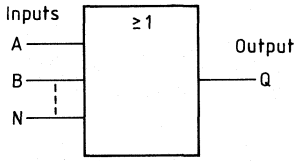


Truth table of NOR
with two inputs

Inputs A	B	Output Q
L	L	H
L	H	L
H	L	L
H	H	L

Logic function: $Q = \overline{A \vee B \vee \ldots \vee N}$
Definition: an H signal will only be present at the output if A and B and . . . and N show an L signal.

OR

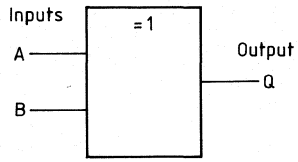


Truth table of OR
with two inputs

Inputs A	B	Output Q
L	L	L
L	H	H
H	L	H
H	H	H

Logic function: $Q = A \vee B \vee \ldots \vee N$
Definition: an L signal will only be present at the output if A and B and . . . and N show an L signal.

Exclusive OR

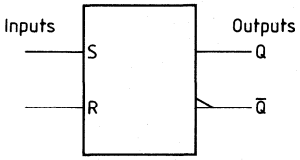


Truth table of exclusive-OR
with two inputs

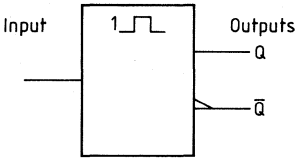
Inputs A	B	Output Q
L	L	L
L	H	H
H	L	H
H	H	L

Logic function: $Q = (A \wedge \overline{B}) \wedge (\overline{A} \wedge B)$
Definition: an H signal will only be present at the output if either only A or only B shows an H signal.

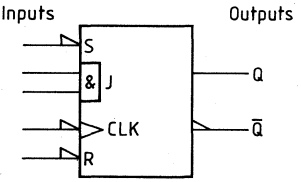
Symbols for Bistable and Monostable Elements



Bistable element (flipflop)



Monostable element (monoflop) with an input acting upon both outputs



J 1, J 2 and K are information inputs. J 1 and J 2 are AND connected. Inputs J and K are (clock-) controlled by the input CLK. S and R are independent set and reset inputs.

2.7 Introduction to Operational Amplifiers

Integrated operational amplifiers (op amps) are dc voltage amplifiers with a very broad scope of applications in control technology, industrial electronics, and in audio frequency engineering.

2.7.1 Graphical Symbols and Terms Used

The graphical symbol "operational amplifier" shows only signal inputs and outputs. **Figure 1** shows the graphical symbol used, with an "inverting" input 1, a "non-inverting" input 2, and an output 3. A positive signal at input 1 results in a negative signal at output 3.

Figure 1

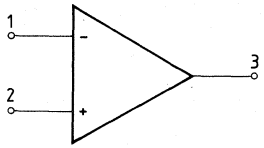
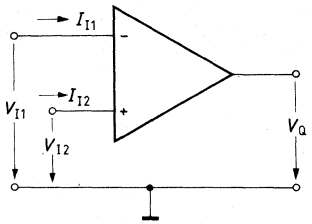


Figure 2



Definitions of the most important terms generally used to characterize an operational amplifier, are listed below. All definitions refer to symmetrical supply voltages.

a) Input offset voltage V_{IO} is that voltage difference which must be applied to the input terminals to achieve an output voltage of 0 V **(figure 2).**
$V_{IO} = V_{I1} - V_{I2}$ at $V_Q = 0$ and generator resistance $R_G = 50\ \Omega$.

b) Input current I_I is the average static input current required for op amp operation **(figure 2).**

$$I_I = \frac{I_{I1} + I_{I2}}{2}$$

c) Input offset current I_{IO} is the difference between the input currents in the operating range. At high values of generator resistance, I_{IO} may cause difficulties **(figure 2).**

d) Open-loop voltage gain G_{V0} is the amplification without feedback **(figure 3).**

$$G_{V0} = \frac{V_Q}{V_I}$$

e) Common-mode voltage gain G_{VC} is the amplification of an in-phase signal applied to both inputs **(figure 4).**

Figure 3

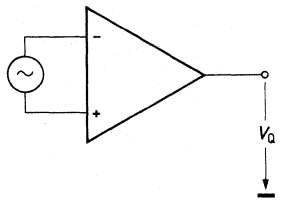
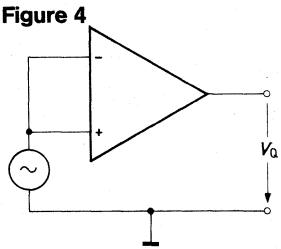
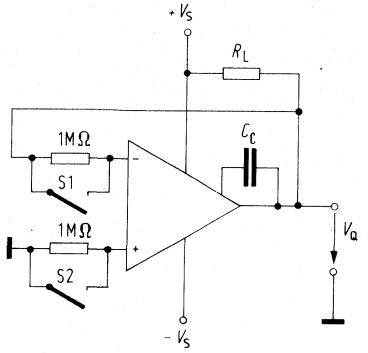


Figure 4



2.7.2 Test Circuits for Operational Amplifiers

Input Current, Input Offset Current



S1 open – S2 closed;

$$I_{I-} = \frac{V_Q}{1\,M\Omega}$$

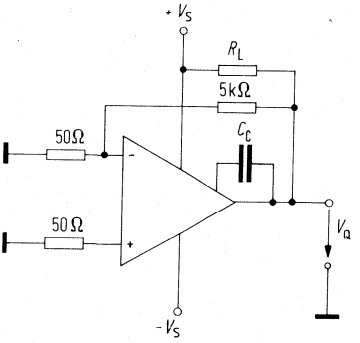
S2 open – S1 closed:

$$I_{I+} = \frac{V_Q}{1\,M\Omega}$$

S1 + S2 open:

I_{IO} approx. $\frac{V_Q}{1\,M\Omega}$

Input Offset Voltage

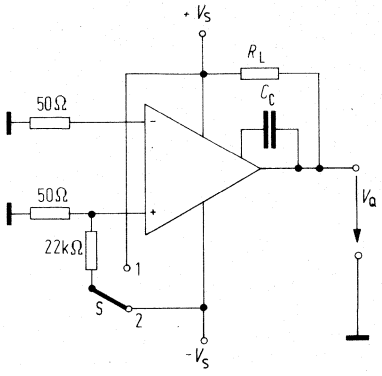


$$-V_{IO} = V_{QO}/G_{V0}$$

$G_{V0} = 100$

$$-V_{IO} = \frac{V_{QO}}{100}$$

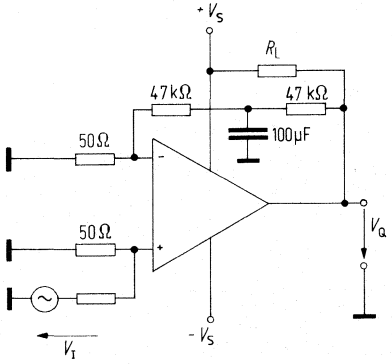
Output Voltage, Control Range



S in position 1: $V_Q = V_{QL}$

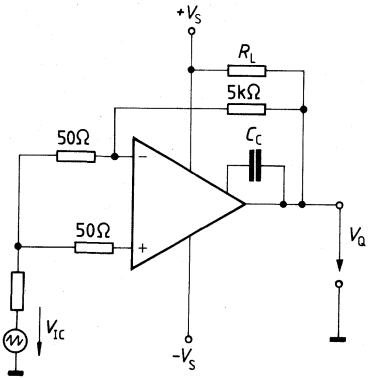
S in position 2: $V_Q = V_{Q0}$

Open-Loop Voltage Gain at $f = 1$ kHz



$$G_{V0} = 20 \log \frac{V_Q}{V_I} \text{ [dB]}$$

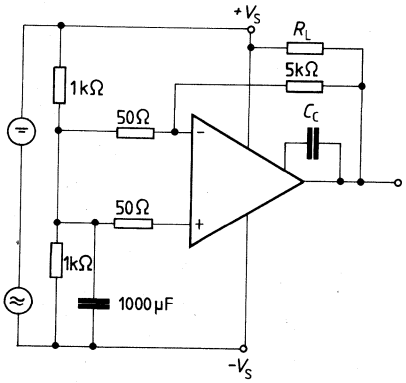
Common-Mode Rejection



$$G_{VC} = \frac{\Delta V_Q}{\Delta V_{IC}}$$

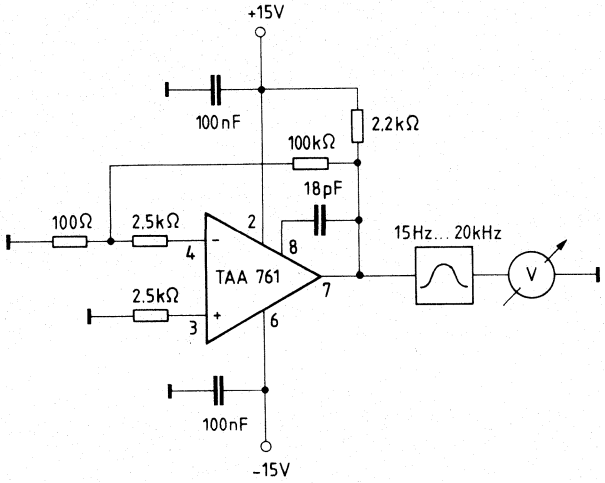
$$k_{CMR} = 20 \log \frac{G_{V0}}{G_{VC}} \text{ [dB]}$$

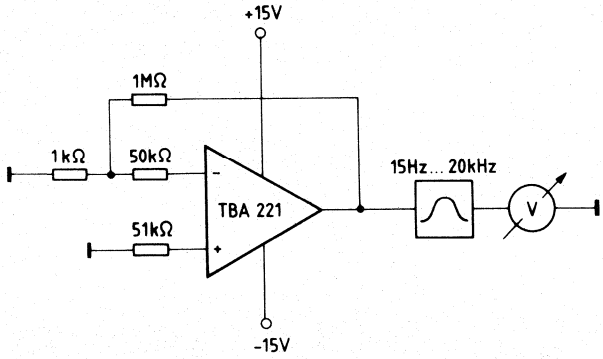
Supply Voltage Rejection



$$\frac{\Delta V_{IO}}{\Delta V_S} = \frac{\Delta V_Q}{100 \times \Delta V_S}$$

Noise voltage in accordance with DIN 45405
Psophometer U 2033 (from Siemens)
Position: noise voltage; evaluation peak/zero





Relationship between Slew Rate *SR* and Cutoff Frequency for High-Signal Output Voltage Swing (Power Bandwidth f_p)

The slew rate of an operational amplifier is determined by the charge/discharge of capacitors. For a capacitor the charge is

$$Q = C \cdot V \text{ or } Q = \int I \cdot dt.$$

The voltage of capacitors changes as:

$$dv/dt \approx \Delta V/\Delta t = I/C$$

For the given current, faster charging or discharging of capacitors is not possible. This maximum speed of the voltage change is indicated for op amps by the factor *SR* (so-called slew rate) which is given in V/µs. Usual values are of the order of 0.3 to 20 V/µs.

The maximum frequency of a sinewave signal that is amplified without distortion is determined by the steepness of the sinewave signal at the zero crossover ($t = 0$).

The sinewave signal of amplitude V_{QS} and angular frequency ω ($= 2\pi f$) has a steepness that is described by the first derivative of this function:

signal: $V_q = V_{QS} \cdot \sin(\omega t)$

1st derivative: $dvq/dt = V_{QS} \cdot \omega \cdot \cos(\omega t)$

for $t = 0$: $\cos(\omega t) = 1$

thus: $dvq/dt_{max} = V_{QS} \cdot \omega \cdot 1 = V_{QS} \cdot 2\pi f$

This value must be less than or equal to the slew rate of the op amp for a distortion-free output signal.

$$SR \geq V_{QS} \cdot 2\pi f$$

Therefore:

$$f_p = \frac{SR}{2 \cdot \pi \cdot V_{QS}} = \frac{SR}{2 \cdot \pi \cdot \sqrt{2} \cdot V_{Qrms}}$$

$$V_{Qrms} = \frac{SR}{2 \cdot \pi \cdot \sqrt{2} \cdot f_p}$$

Example 1: $SR = 0.5\ V/\mu s$ (corresponding to 500 000 V/s)

$V_{Qrms} = 10\ V$

$$f_p = \frac{500\,000}{2 \cdot \pi \cdot \sqrt{2} \cdot 10} = 5.62\ kHz$$

If a signal of 10 kHz is to be transmitted, this is possible without distortion up to an rms voltage of 5.62 V.

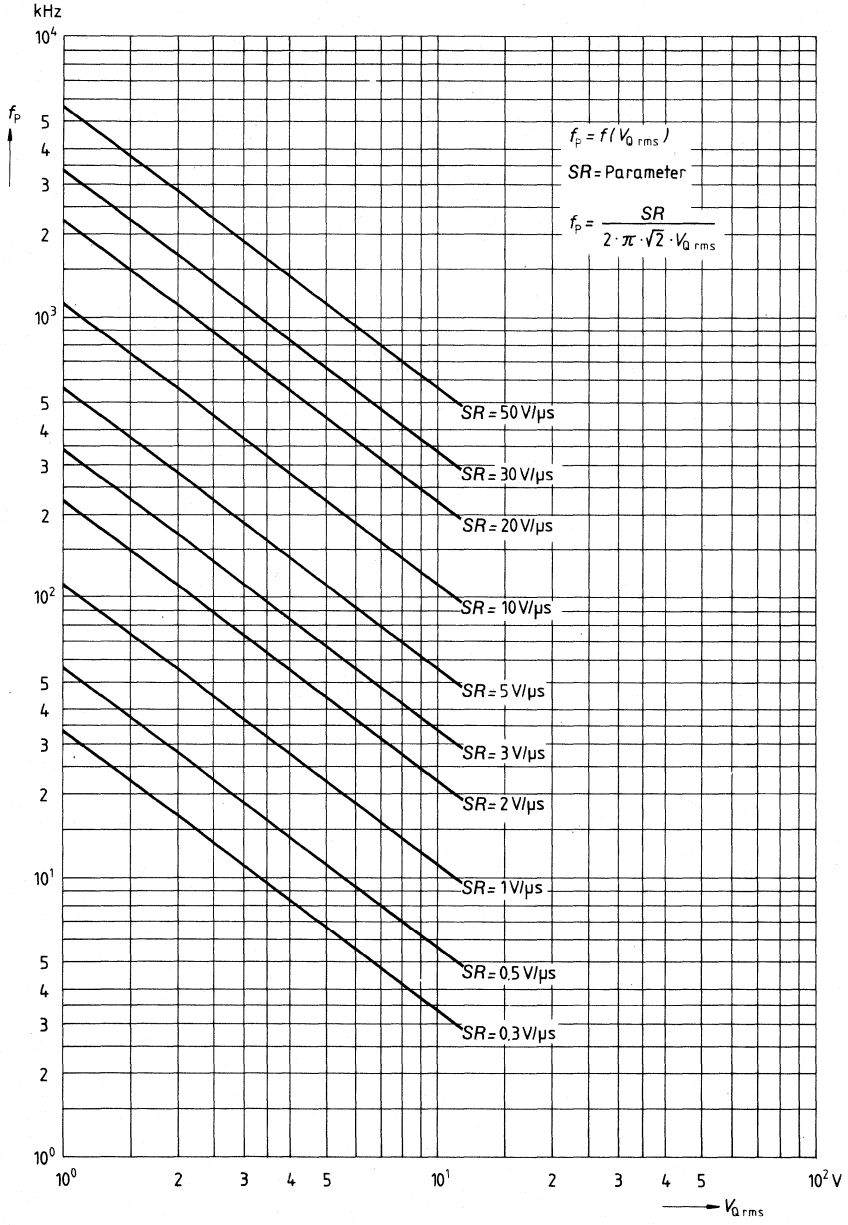
Example 2: $SR = 10\ V/\mu s$

$V_{Qrms} = 10\ V$

$f_p = 112\ kHz$

The bandwidth cannot of course be infinite (as is possible in the equation). Additionally there is a limitation due to the small-signal cutoff frequency (f_T).

Slew Rate and Power Bandwidth



Instructions for the Use of Integrated Operational Amplifiers

Preventive measures are implemented in most operational amplifiers, to reduce the risk of interference and failure.

Malfunctions or failure may however arise if several limiting conditions are simultaneously reached (e.g. max. output current, max. T_A, short circuits etc.)

This is also the case if the outputs are subject to high inductive and capacitive loads since inductive loads, flyback voltages and capacitive loads >1 nF generate extreme current surges.

High capacitive loads (≥100 pF) may lead to stability problems in op amps with high slew rates and high output currents (e.g. TAE 2453/TAE 4453).

There are two known remedies for this;

- Limitation of the output current surges **(figure 1, 3, 4)**
- Stronger or additional frequency compensation **(figure 2)**

Not driving the output hard into saturation i.e. setting the quiescent point in the middle of the control range, when the analogous output signal is smaller than the possible control range will also simplify this problem.

The minimum value for frequency compensation capacitance is given in the data book as follows:

Generator resistances	> 10 kΩ
Stray capacitances	< 5 pF at the summing point
Loads	< 100 pF

In other cases it may be necessary to use a stronger frequency compensation and/or a forward compensation from the input to the output (see TAA 762, test circuit 2 and **figure 1**).

For precision applications or open-loop operations, we recommend that both inputs on the PC board be protected by a guard ring and that the leads running to the inputs be manufactured with a shielded litz wire.

Shields of this kind are also recommended for applications with low input currents (or extremely high feedback resistance).

They prevent parasitic currents from occurring on the PC board – a phenomenon which might arise owing to soiled surfaces, for example.

Figure 1

Improving the stability at high capacitive loads ≥ 100 pF by limiting the surge currents with *R*

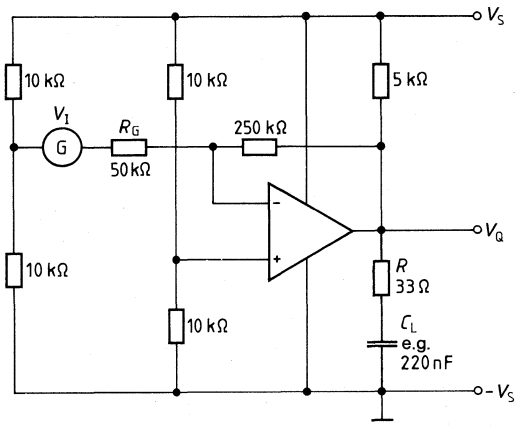


Figure 2

Compensation by means of approx. 220 Ω and 10 nF at input when no compensation point in the op amp is available, e.g. with gain 1, integrators and high capacitive loads.

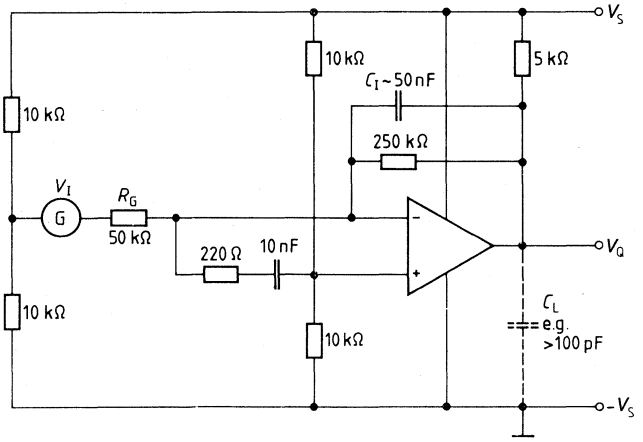
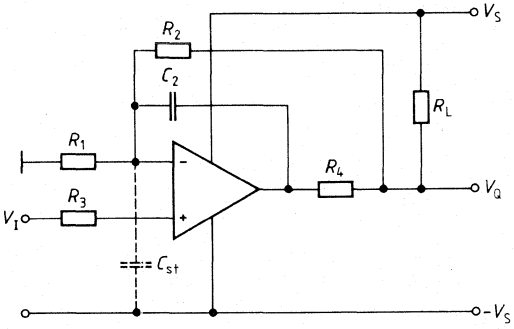


Figure 3

Protecting the inputs and outputs and compensation of the stray capacitance C_{st}



Gain

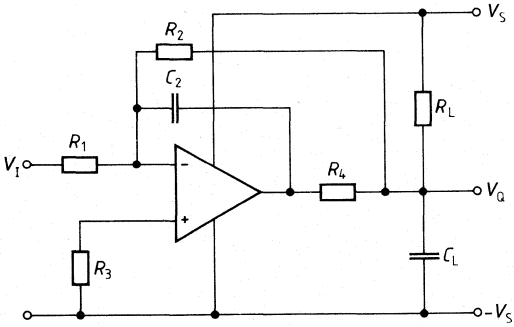
$$G = \frac{R_1 + R_2}{R_1}$$

Compensation

$$C_2 \approx \frac{R_1}{R_2} C_{st}$$

Figure 4

Wiring in the case of large capacitive loads



Gain

$$G = \frac{R_2}{R_1}$$

In figure 4 and 5:

R_3: Input protection

R_4: Output protection

R_L: Collector resistance (always required for op amps with open collector output).

Operational Amplifiers

Selector Guide

Type	Package	Operating range			Electrical characteristics $V_S = \pm 15$ V, $T_A = 25$ °C		
		Supply voltage V_S V	Operating temperature T_A °C	Output current I_Q mA max.	Input offset voltage ($R_G = 50\ \Omega$) V_{IO} mV min./max.	Input current I_I µA typ.	Slew rate ($R_L = 2$ kΩ) SR V/µs typ.
Single Operational Amplifiers with NPN Input and Open Collector Output							
TAA 762 A	P-DIP-6	±1.5 to ±18	-55 to 125	70	±4	0.3	18
TAA 762 G	similar to P-DSO-6	±1.5 to ±18	-55 to 125	70	±4	0.3	18
TAA 765 A	P-DIP-6	±1.5 to ±18	-25 to 85	70	±5.5	0.5	18
TAA 765 G	similar to P-DSO-6	±1.5 to ±18	-25 to 85	70	±5.5	0.5	18
Dual Operational Amplifiers with NPN Input and Open Collector Output							
TAA 2762 A	P-DIP-8	±2 to ±15	-55 to 125	70	±4	0.3	0.5
TAA 2765 A	P-DIP-8	±2 to ±15	-25 to 85	70	±5.5	0.5	0.5
Quad Operational Amplifiers with NPN Input and Open Collector Output							
TAA 4762 A	P-DIP-14	±2 to ±15	-55 to 125	70	±4	0.3	0.5
TAA 4765 A	P-DIP-14	±2 to ±15	-25 to 85	70	±5.5	0.5	0.5
Single Operational Amplifiers with Darlington Input and Open Collector Output							
TCA 332 A	P-DIP-6	±2 to ±15	-55 to 125	70	±10	5	9
TCA 332 G	similar to P-DSO-6	±2 to ±15	-55 to 125	70	±10	5	9
TCA 335 A	P-DIP-6	±2 to ±15	-25 to 85	70	±15	5	9
TCA 335 G	similar to P-DSO-6	±2 to ±15	-25 to 85	70	±15	5	9
Dual Operational Amplifiers with Darlington Input and Open Collector Output							
TBC 2332 B	P-DIP-8	±2 to ±15	-55 to 125	70	±10	5	0.5
TBE 2335 B	P-DIP-8	±2 to ±15	-25 to 85	70	±15	5	0.5
Quad Operational Amplifiers with Darlington Input and Open Collector Output							
TBC 4332 A	P-DIP-14	±2 to ±15	-55 to 125	70	±10	5	0.5
TBE 4335 A	P-DIP-14	±2 to ±15	-25 to 85	70	±15	5	0.5

Selector Guide (cont'd)

Type	Package	Operating range			Electrical characteristics $V_S = \pm 15$ V, $T_A = 25$ °C		
		Supply voltage V_S V	Operating temperature T_A °C	Output current I_Q mA	Input offset voltage ($R_G = 50\ \Omega$) V_{IO} mV	Input current I_I µA	Slew rate ($R_L = 2\ k\Omega$) SR V/µs
				max	min/max	typ	typ
Single Operational Amplifiers with PNP Input and Open Collector Output							
TAE 1453 A	P-DIP-6	±1.0 to ±18	-25 to 85	100	±5.5	0.04	20
TAE 1453 G	similar to P-DSO-6	±1.0 to ±18	-25 to 85	100	±5.5	0.04	20
TAF 1453 A	P-DIP-6	±1.0 to ±18	-55 to 125	100	±4	0.04	20
TAF 1453 G	similar to P-DSO-6	±1.0 to ±18	-55 to 125	100	±4	0.04	20
Dual Operational Amplifiers with PNP Input and Open Collector Output							
TAE 2453 A	P-DIP-8	±1.0 to ±18	-25 to 85	100	±5.5	0.04	1
TAE 2453 G	similar to P-DSO-8	±1.0 to ±18	-25 to 85	100	±5.5	0.04	1
TAF 2453 A	P-DIP-8	±1.0 to ±18	-55 to 125	100	±4	0.04	1
TAF 2453 G	similar to P-DSO-8	±1.0 to ±18	-55 to 125	100	±4	0.04	1
Quad Operational Amplifiers with PNP Input and Open Collector Output							
TAE 4453 A	P-DIP-14	±1.0 to ±18	-25 to 85	100	±5.5	0.04	1
TAE 4453 G	P-DSO-14	±1.0 to ±18	-25 to 85	100	±5.5	0.04	1
TAF 4453 A	P-DIP-14	±1.0 to ±18	-55 to 125	100	±4	0.04	1
TAF 4453 G	P-DSO-14	±1.0 to ±18	-55 to 125	100	±4	0.04	1
Single Operational Amplifiers with Push-Pull Output							
TBA 221 B	P-DIP-8	±4 to ±18	0 to 70	±20	±6	0.08	0.5
TBA 222 B/S1	P-DIP-8	±4 to ±22	-55 to 125	±20	±4	0.08	0.5
TBB 0741 G	similar to P-DSO-8	±4 to ±18	0 to 70	±20	±6	0.08	0.5
TBB 0742 G	similar to P-DSO-8	±4 to ±22	-55 to 125	±20	±4	0.08	0.5
Dual Operational Amplifiers with Push-Pull Output							
TBB 1458 B	P-DIP-8	±4 to ±18	0 to 70	±18	±6	0.08	0.5
TBB 1458 G	similar to P-DSO-8	±4 to ±18	0 to 70	±18	±6	0.08	0.5

Type	Ordering Code	Package	Color Code
S TAA 762 A	Q67000-A2271	P-DIP-6	–
TAA 762 G	Q67000-A2273	similar to P-DSO-6 (SMD)	white/yellow
S TAA 765 A	Q67000-A524	P-DIP-6	–
S TAA 765 G	Q67000-A599-G403	similar to P-DSO-6 (SMD)	yellow/yellow

Particularly economic and versatile op amps. Owing to their excellent performance qualities they are well suited for a wide scope of applications, as in control engineering, automotive electronics, AF circuits, analog computers, etc.

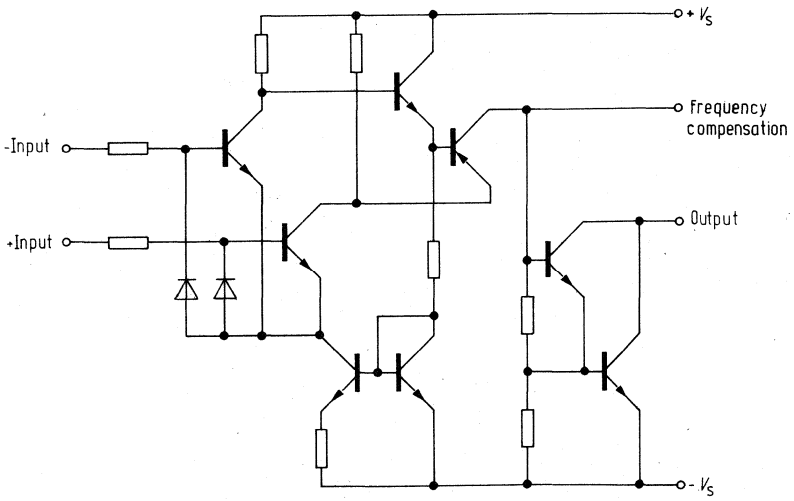
Features

- Wide common-mode range
- Large supply voltage range
- Large control range
- Wide temperature range (TAA 762)
- High output current
- Simple frequency compensation
- Open collector output

Applications

- Amplifier
- Comparator
- Level converter
- Driver

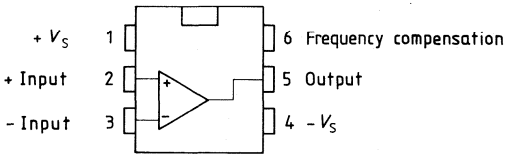
Circuit Diagram



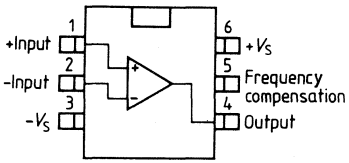
Pin Configurations

(top view)

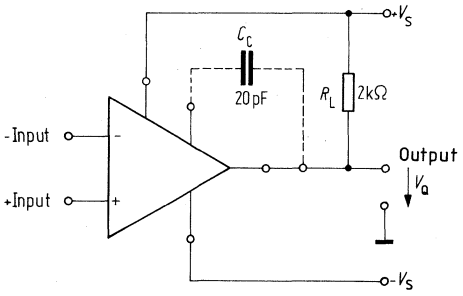
TAA 762 A
TAA 765 A



TAA 762 G
TAA 765 G



Connection Diagram



C_C = output frequency compensation;
R_L = load resistance (collector resistance)

Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	70	mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air TAA 762 A	$R_{th\ SA}$	115	K/W
TAA 762 G	$R_{th\ SA}$	200	K/W

Operating Range

Supply voltage	V_S	± 1.5 to ± 18	V
Ambient temperature	T_A	−55 to 125	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ, unless otherwise specified

		$T_A = 25$ °C			$T_A = -55$ to 125 °C		
Description	Symbol	min	typ	max	min	max	Unit
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}	−100	±50	100	−300	300	nA
Input current	I_I		0.3	0.7		1.0	µA
Control range							
$V_S = \pm 15$ V	$V_{Q\ pp}$	14.9		−14	14.8	−14	V
$R_L = 620\ \Omega$, $V_S = \pm 15$ V	$V_{Q\ pp}$	14.9		−12.5	14.8	−12	V
$V_S = \pm 15$ V, $f = 100$ kHz	$U_{Q\ pp}$		±10				V
Input impedance $f = 1$ kHz	Z_i		200				kΩ
Open-loop voltage gain							
$f = 1$ kHz	G_{V0}	85	87		80		dB
$R_L = 10$ kΩ, $f = 1$ kHz	G_{V0}		92				dB
$f = 1$ MHz	G_{V0}		43				dB
Output reverse current	I_{QR}			1		5	µA

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ,
unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -55$ to 125 °C min	max	Unit
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_2-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	80	85		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	200		200	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω	α_{VIO}		6	25		25	µV/K
Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{IIO}		0.3	1.5		1.5	nA/K
Slew rate of V_q for non-inverting operation[1] (test circuit 1)	SR		9				V/µs
Slew rate of V_q for inverting operation[1] (test circuit 2)	SR		18				V/µs
Noise voltage (in acc. with DIN 45405; referred to input; $R_S = 2.5$ kΩ	V_n		3				µV

Characteristics

$V_S = \pm 2$ V; $R_L = 2$ kΩ

Input offset voltage $R_G = 50$ Ω)	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}	−70		70	−200	200	nA
Input current	I_I		0.2	0.5		0.8	µA
Open-loop voltage gain $f = 1$ kHz	G_{V0}	80			75		dB

[1] For the relationship between power bandwidth and slew rate refer to **"General information"**

Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	±18	V
Output current	I_Q	70	mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air TAA 765 A	$R_{th\ SA}$	115	K/W
TAA 765 G	$R_{th\ SA}$	200	K/W

Operating Range

Supply voltage	V_S	±1.5 to ±18	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ, unless otherwise specified

		$T_A = 25$ °C			$T_A = -25$ to 85 °C		
Description	Symbol	min	typ	max	min	max	Unit
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current	I_{IO}	−200	±80	200	−300	300	nA
Input current	I_I		0.5	0.8		1.0	µA
Control range							
$V_S = \pm 15$ V	$V_{Q\ pp}$	14.9		−14	14.8	−14	V
$R_L = 620\ \Omega$, $V_S = \pm 15$ V	$V_{Q\ pp}$	14.9		−12.5	14.8	−12	V
$V_S = \pm 15$ V, $f = 100$ kHz	$U_{Q\ pp}$		±10				V
Input impedance $f = 1$ kHz	Z_i		200				kΩ
Open-loop voltage gain							
$f = 1$ kHz	G_{V0}	80	85		80		dB
$R_L = 10$ kΩ, $f = 1$ kHz	G_{V0}		90				dB
$f = 1$ MHz	G_{V0}		43				dB
Output reverse current	I_{QR}			10		20	µA

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ,
unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -25$ to 85 °C min	max	Unit
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	75	83		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	200		200	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω	α_{VIO}		6	25		25	µV/K
Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{IIO}		0.3	1.5		1.5	nA/K
Slew rate of V_q for non-inverting operation[1] (test circuit 1)	SR		9				V/µs
Slew rate of V_q for inverting operation[1] (test circuit 2)	SR		18				V/µs
Noise voltage (in acc. with DIN 45405; referred to input; $R_S = 2.5$ kΩ)	V_n		3				µV

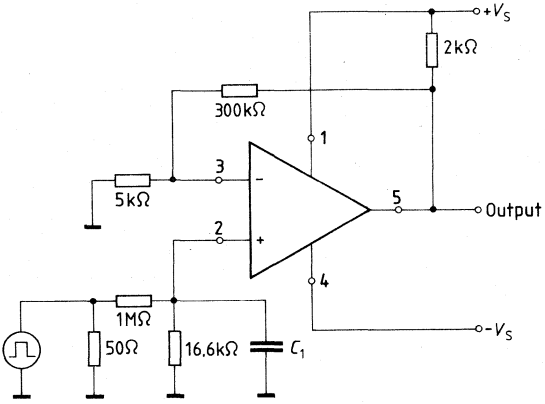
Characteristics

$V_S = \pm 2$ V, $R_L = 2$ kΩ

Input offset voltage $R_G = 30$ Ω	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current	I_{IO}	−150		150	−200	200	nA
Input current	I_I		0.2	0.6		0.8	µA
Open-loop voltage gain $f = 1$ kHz	G_{V0}	75			75		dB

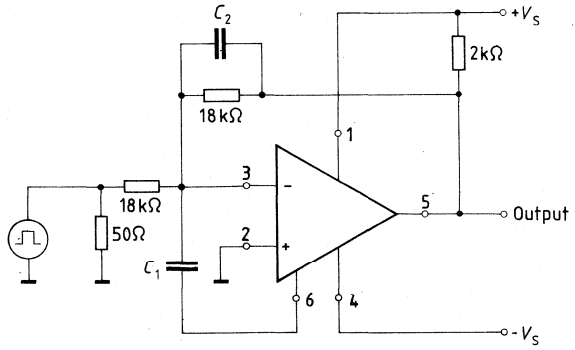
[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

Test Circuit 1 for Slew Rate (non-inverting operation)



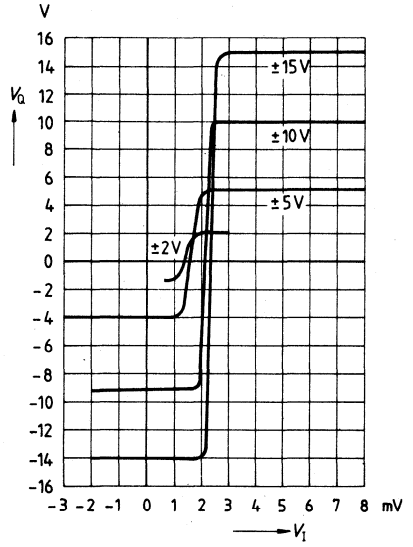
C_1 for min. overshoot (approx. 22 pF)

Test Circuit 2 for Slew Rate (inverting operation)

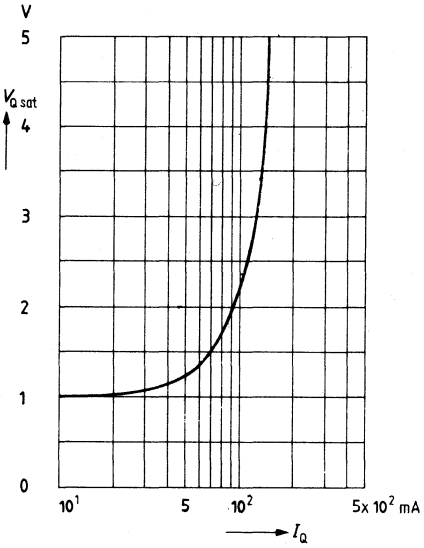


C_2 causes a frequency-dependent compensation to reduce rise times (approx. 390 pF)
C_1 for min. overshoot (approx. 3.9 pF)

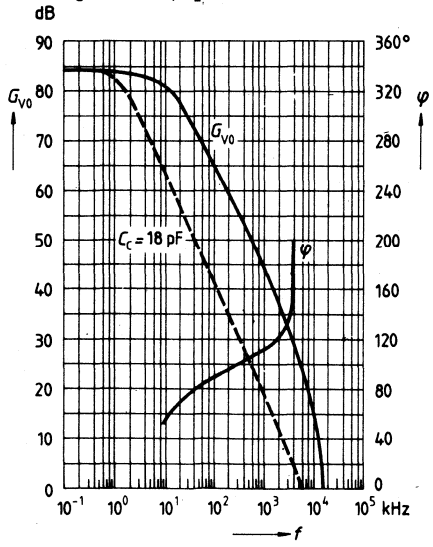
Transfer characteristic
Output voltage versus input voltage
V_S = parameter, R_L = 2 kΩ



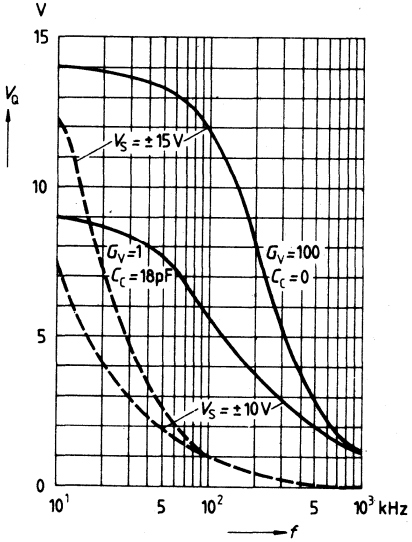
Saturation voltage versus output current
T_A = 25 °C



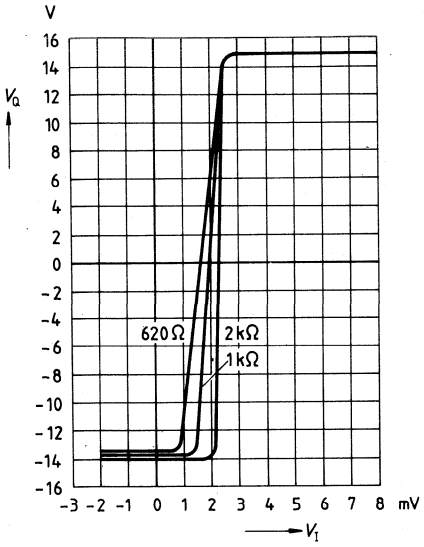
Open-loop voltage gain and phase versus frequency
V_S = ± 15 V; R_L = 2 kΩ



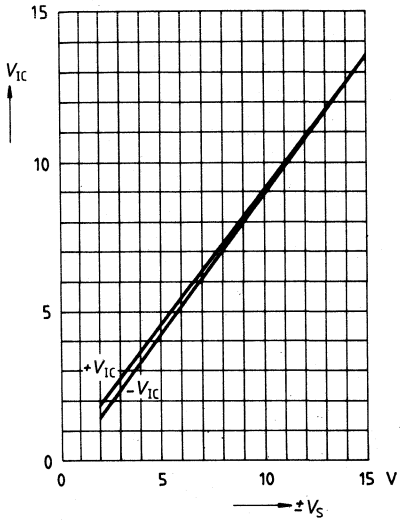
Frequency dependence of large signal modulation
Output voltage versus frequency



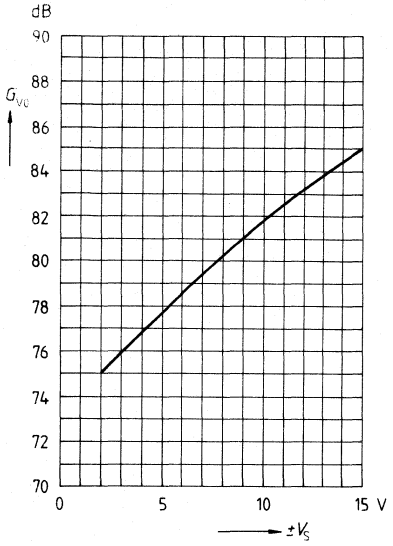
Transfer characteristic
Output voltage versus input voltage
$V_S = \pm$ 15 V; R_L = parameter



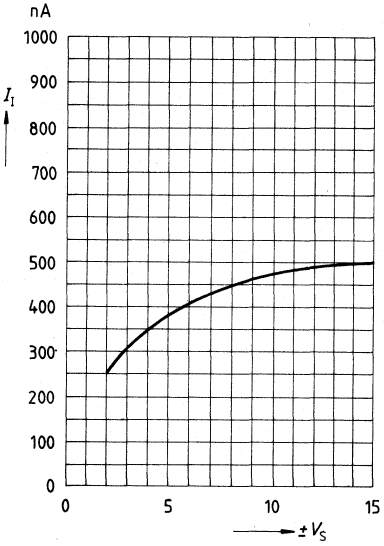
Common-mode voltage range
Common-mode input
voltage versus supply voltage



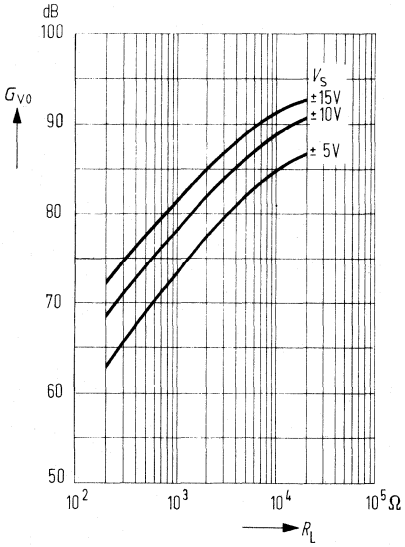
Open-loop voltage gain versus supply voltage
$T_A = 25\,°C$; $R_L = 2\,k\Omega$



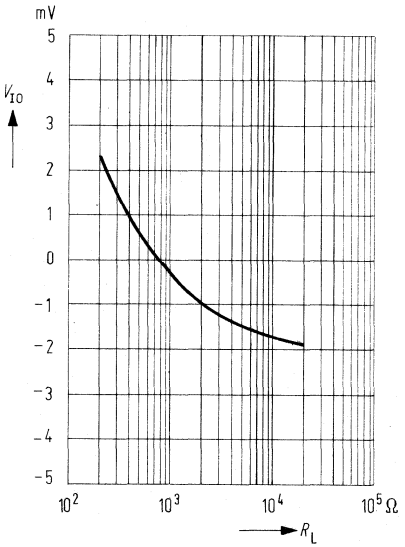
Input current versus supply voltage



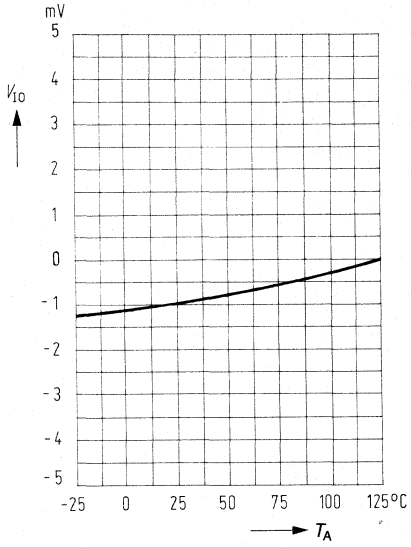
Open-loop voltage gain versus load resistance
$T_A = 25\,°C$



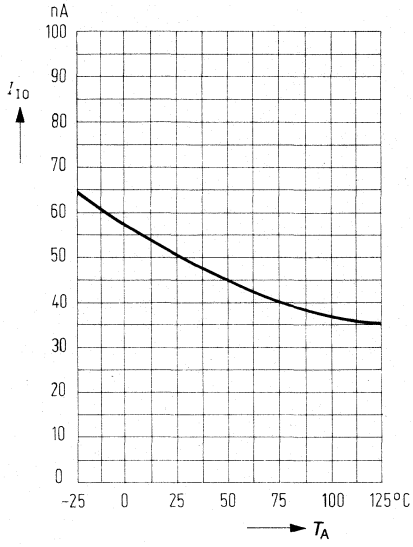
Input offset voltage versus load resistance
$V_S = \pm 15\,V$



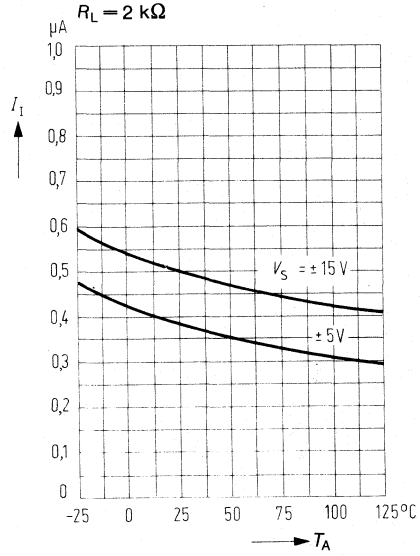
Input offset voltage versus ambient temperature
$R_L = 2\ k\Omega$, $V_S = \pm 15\ V$



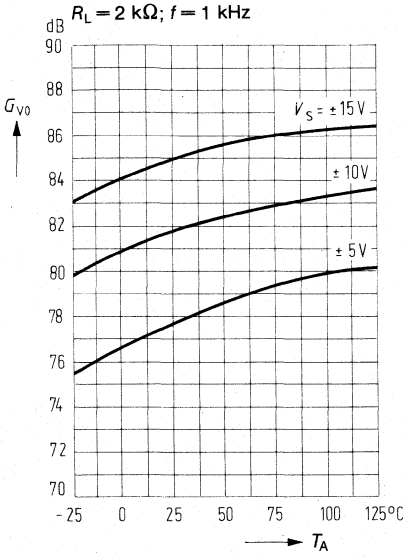
Input offset current versus ambient temperature
$R_L = 2\ k\Omega$, $V_S = \pm 15\ V$



Input current versus ambient temperature
$R_L = 2\ k\Omega$



Open-loop voltage gain versus ambient temperature
$R_L = 2\ k\Omega$; $f = 1$ kHz



Type	Ordering Code	Package	Color Code
TCA 332 A	Q67000-A2272	P-DIP-6	–
TCA 332 G	Q67000-A2270	similar to P-DSO 6 (SMD)	orange/yellow
TCA 335 A	Q67000-A563	P-DIP-6	–
TCA 335 G	Q67000-A1018-G403	similar to P-DSO-6 (SMD)	blue/yellow

For TCA 315 A, G; TCA 325 A, G see **chapter "Comparators".**

These op amps are particularly economic and versatile. Owing to their excellent performance characteristics they are well suited for a wide scope of applications, such as measuring and control engineering, automotive electronics, AF circuits, analog computers, etc. The low input current of these amplifiers is particularly advantageous for application in measuring and control systems.

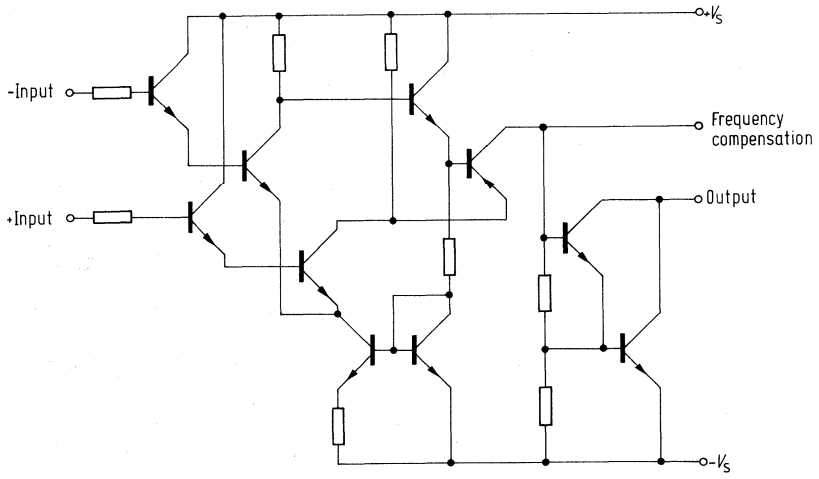
Features

- High input impedance
- Wide common-mode range
- Large supply-voltage range
- Large control range
- High output current
- Simple frequency compensation
- Wide temperature range (TCA 332)
- NPN Darlington input
- Open collector output

Applications

- Amplifier
- Comparator
- Level converter
- Impedance converter
- Driver

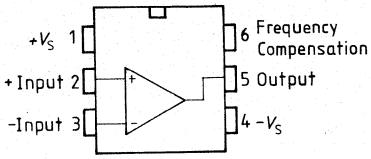
Circuit Diagram



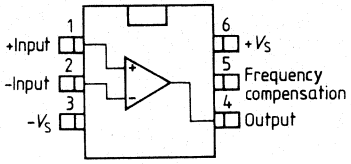
Pin Configurations

(top view)

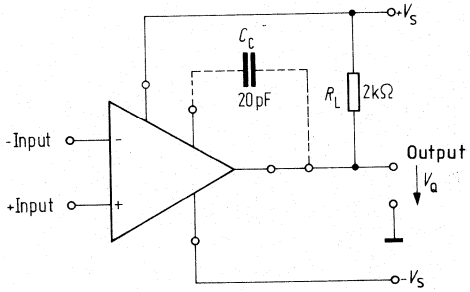
TCA 332 A
TCA 335 A



TCA 332 G
TCA 335 G



Connection Diagram



C_C = output frequency compensation
R_L = load resistance (collector resistance)

Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	± 15	V
Output current	I_Q	70	mA
Differential input voltage: V_S = 13 to 15 V Differential input voltage: V_S = 2 to 13 V	V_{ID} V_{ID}	± 13 ± V_S	V V
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air TCA 332 A TCA 332 G	 $R_{th\,SA}$ $R_{th\,SA}$	 115 200	 K/W K/W

Operating Range

Supply voltage	V_S	± 2 to ± 15	V
Ambient temperature	T_A	−55 to 125	°C

Characteristics

V_S = ± 5 V to ± 15 V
R_L = 2 kΩ, unless otherwise specified

		T_A = 25 °C			T_A = −55 to 125 °C		
Description	Symbol	min	typ	max	min	max	Unit
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage R_G = 50 Ω	V_{IO}	−10		10	−15	15	mV
Input offset current Input current Input current V_{ID} = ± 13 V	I_{IO} I_I I_I	−5	 5 	5 15 200	−10	10 25 	nA nA nA
Control range V_S = ± 15 V R_L = 620 Ω, V_S = ± 15 V V_S = ± 15 V, f = 100 kHz	$V_{Q\,pp}$ $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9	 ± 10	 −14.0 −12.5	 14.8 14.8	 −14.0 −12.0	 V V V

Characteristics
$V_S = \pm 5$ V to ± 15 V
$R_L = 2$ kΩ, unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -55$ to 125 °C min	max	Unit
Input impedance $f = 1$ kHz	Z_i		3				MΩ
Open-loop voltage gain $f = 1$ kHz $R_L = 10$ kΩ, $f = 1$ kHz $f = 1$ MHz	 G_{V0} G_{V0} G_{V0}	 80	 83 88 43		 75		 dB dB dB
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection $R_L = 2$ kΩ	k_{CMR}	75	80		70		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	200		200	μV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		12 50	50		50	μV/K pA/K
Slew rate of V_q for non-inverting operation[1] (see TAA 765, test circuit 1) Slew rate of V_q for inverting operation[1] (see TAA 765, test circuit 2)	SR SR		9 18				V/μs V/μs
Output saturation voltage $I_Q = 10$ mA	V_{Qsat}			1			V
Output reverse current	I_{QR}			1		5	μA

Characteristics
$V_S = \pm 2$ V, $R_L = 2$ kΩ

Input offset voltage $R_G = 50$ Ω	V_{IO}	−10		10	−15	15	mV
Input offset current Input current	I_{IO} I_I	−5	 5	5 15	−10	10 25	nA nA
Open-loop voltage gain $f = 1$ kHz	G_{V0}	75			70		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	± 15	V
Output current	I_Q	70	mA
Differential input voltage: V_S = 13 to 15 V Differential input voltage: V_S = 2 to 13 V	V_{ID} V_{ID}	± 13 ± V_S	V V
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air TCA 335 A TCA 335 G	 $R_{th\ SA}$ $R_{th\ SA}$	 115 200	 K/W K/W

Operating Range

Supply voltage	V_S	± 2 to ± 15	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

V_S = ± 5 V to ± 15 V
R_L = 2 kΩ, unless otherwise specified

		T_A = 25 °C			T_A = −25 to 85 °C		
Description	Symbol	min	typ	max	min	max	Unit
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage R_G = 50 Ω	V_{IO}	−15		15	−18	18	mV
Input offset current Input current Input current V_{ID} = ± 13 V	I_{IO} I_I I_I	−10	 5 	10 25 200	−20	20 35 	nA nA nA
Control range V_S = ± 15 V R_L = 620 Ω, V_S = ± 15 V V_S = ± 15 V, f = 100 kHz	 $V_{Q\ pp}$ $V_{Q\ pp}$ $V_{Q\ pp}$	 14.9 14.9 	 ± 10	 −14.0 −12.5 	 14.8 14.8 	 −14.0 −12.0 	 V V V

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ,
unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -25$ to 85 °C min	max	Unit
Input impedance $f = 1$ kHz	Z_i		3				MΩ
Open-loop voltage gain $f = 1$ kHz $R_L = 10$ kΩ, $f = 1$ kHz $f = 1$ MHz	 G_{V0} G_{V0} G_{V0}	 75	 80 85 43		 75		 dB dB dB
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	70	78		70		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	200		200	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		12 50	50		50	µV/K pA/K
Slew rate of V_q for non-inverting operation[1]) (see TAA 765, test circuit 1) Slew rate of V_q for inverting operation[1]) (see TAA 765, test circuit 2)	SR SR		9 18				V/µs V/µs
Output saturation voltage $I_Q = 10$ mA	V_{Qsat}			1			V
Output reverse current	I_{QR}			10		20	µA

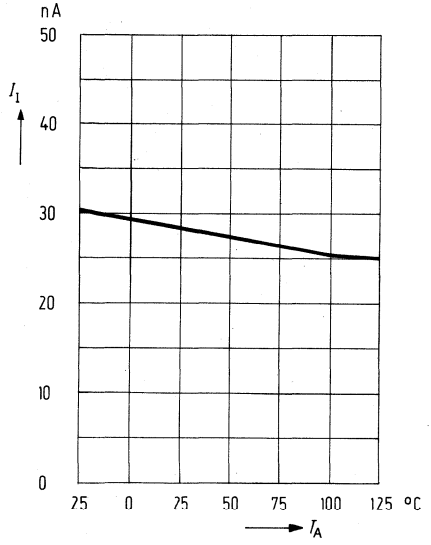
Characteristics

$V_S = \pm 2$ V, $R_L = 2$ kΩ

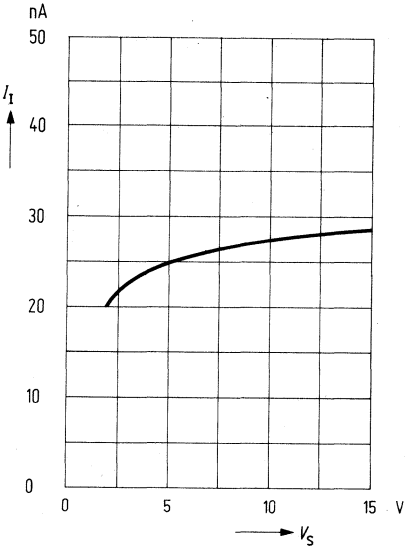
Input offset voltage $R_G = 50$ Ω	V_{IO}	−17		17	−20	20	mV
Input offset current Input current	I_{IO} I_I	−10	 5	10 25	−20	20 35	nA nA
Open-loop voltage gain $f = 1$ kHz	G_{V0}	70			70		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

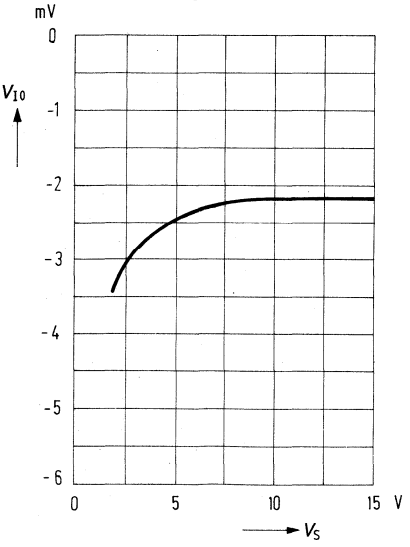
Input current versus ambient temperature
$R_L = 2\ k\Omega$



Input current versus supply voltage
$T_A = 25\,°C$; $R_L = 2\ k\Omega$



Input offset voltage versus supply voltage



Type	Ordering Code	Package	Color Code
TAE 1453 A	Q67000-A2017	P-DIP-6	–
TAE 1453 G	Q67000-A2106	similar to P-DSO-6 (SMD)	blue/white
TAF 1453 A	Q67000-A2269	P-DIP-6	–
TAF 1453 G	Q67000-A2209	similar to P-DSO-6 (SMD)	red/red

These operational amplifiers are circuits for universal applications having a PNP input differential stage and an open collector output. Apart from one resistor, only active components are used. The integrated regulator provides for all parameters a large degree of independence from the supply voltage.

Features

- Supply voltage range between 2 V (1.8 V) and 36 V
- Low current consumption, 0.25 mA typ.
- Extremely large control range
- Low output saturation voltage, almost independent of load current
- Output current up to 70 mA (100 mA max.)
- Wide common-mode range
- Wide operating temperature range (TAF 1453A, TAF 1453G)
- Pin-compatible to TAA 765

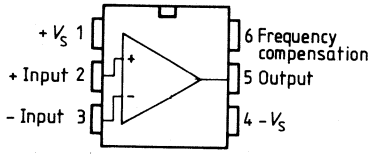
Applications

- Amplifier
- Level converter
- Driver
- Zero voltage switch
- Comparator

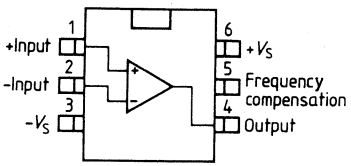
Pin Configurations

(top view)

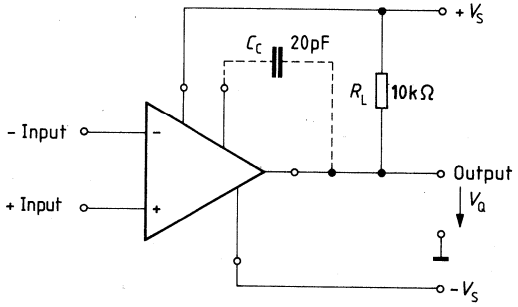
TAE 1453 A,
TAF 1453 A



TAE 1453 G,
TAF 1453 G

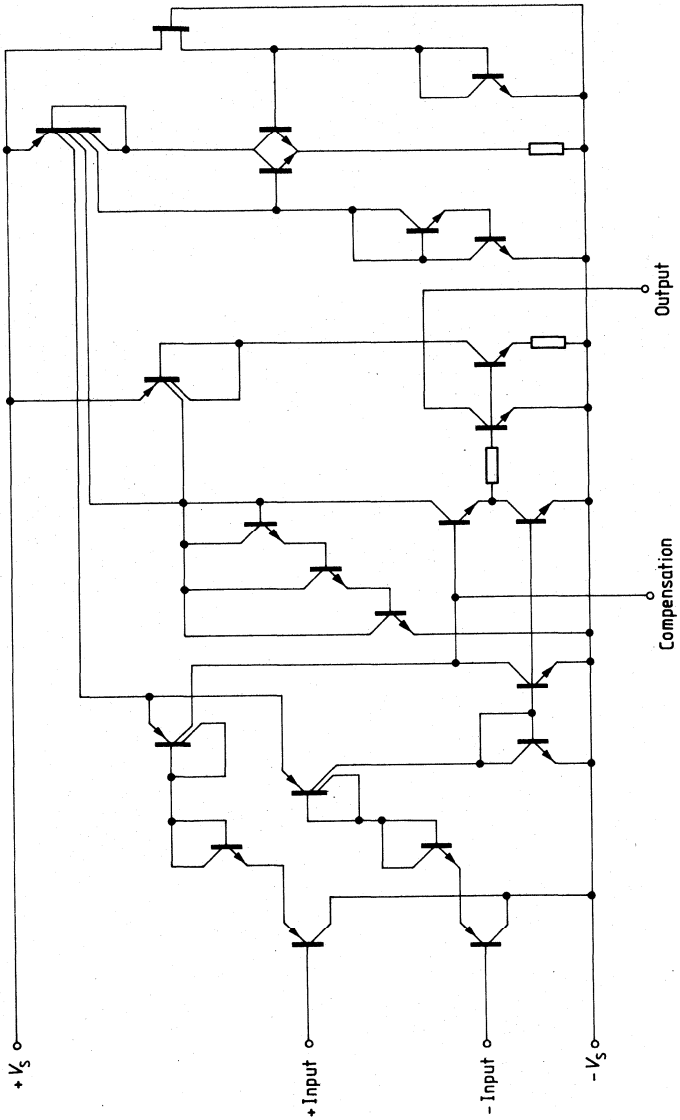


Connection Diagram



C_C = output frequency compensation (if required);
R_L = load resistance (collector resistance)

Circuit Diagram



Maximum Ratings

Description		Symbol	Ratings	Unit
Supply voltage		V_S	± 18	V
Output current		I_Q	100	mA
Differential input voltage		V_{ID}	± V_S	V
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C
Thermal resistance system – air	TAE 1453 A	$R_{th\ SA}$	135	K/W
	TAE 1453 G	$R_{th\ SA}$	200	K/W

Operating Range

Supply voltage	V_S	± 1.0 to ± 18 (± 0.9 V with slightly increased offset voltage)	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 10$ kΩ,
unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -25$ to 85 °C min	max	Unit
Open-loop current consumption	I_S		0.25	0.4		0.45	mA
Input offset voltage $R_G = 50$ Ω	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current Input current	I_{IO} I_I	−15	 40	15 150	−100	100 200	nA nA
Control range $R_L = 2$ kΩ, $V_S = \pm 15$ V $R_L = 620$ Ω, $V_S = \pm 15$ V $R_L = 2$ kΩ, $V_S = \pm 15$ V, $f = 100$ kHz	 $V_{Q\,pp}$ $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9 10		 −14.7 −14.5 −10	 14.9 14.9	 −14.7 −14.4	 V V V
Input impedance $f = 1$ kHz	Z_i		200				kΩ
Open-loop voltage gain	G_{V0}	78	85		78		dB
Output reverse current	I_{QR}			10		20	μA
Common-mode input voltage range	V_{IC}	$-V_S-0.2$		$V_S-1.8$	$-V_S$	$V_S-2.0$	V
Common-mode rejection	k_{CMR}	75	80		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		120	μV/V
Temperature coefficient of I_{IO} $R_G = 50$ Ω Temperature coefficient of V_{IO} $R_G = 50$ Ω	α_{IIO} α_{VIO}		0.1 6				nA/K μV/K
Slew rate for non-inverting operation[1]) Slew rate for inverting operation[1])	SR SR		20 30				V/μs V/μs

Characteristics

$V_S = \pm 2$ V, $R_L = 10$ kΩ

Input offset voltage $R_G = 50$ Ω	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current Input current	I_{IO} I_I	−15	 40	15 150	−100	100 200	nA nA
Open-loop voltage gain	G_{V0}	70			70		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	100	mA
Differential input voltage	V_{ID}	± V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 150	°C
Thermal resistance system – air TAF 1453 A	$R_{th\ SA}$	135	K/W
TAF 1453 G	$R_{th\ SA}$	200	K/W

Operating Range

Supply voltage	V_S	± 1.0 to ± 18 (± 0.9 with slightly increased offset voltage)	V
Ambient temperature	T_A	−55 to 125	°C

Characteristics

$U_S = \pm 5$ V to ± 15 V
$R_L = 10$ kΩ, unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -55$ to 125 °C min	max	Unit
Open-loop current consumption (Output in H state)	I_S		0.25	0.35		0.45	mA
Input offset voltage $R_G = 50$ Ω	V_{IO}	−4		4	−6	6	mV
Input offset voltage Input current	I_{IO} I_I	−10	 40	10 100	−75	75 150	nA nA
Control range $R_L = 2$ kΩ, $V_S = \pm 15$ V $R_L = 620$ Ω, $V_S = \pm 15$ V $R_L = 2$ kΩ, $V_S = 15$ V, $f = 100$ kHz	 $V_{Q\,pp}$ $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9 10		 −14.7 −14.5 −10	 14.9 14.9	 −14.7 −14.4	 V V V
Input impedance $f = 1$ kHz	Z_i		200				kΩ
Open-loop voltage gain	G_{V0}	80	85		80		dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range	V_{IC}	$-V_S$−0.3		V_S−1.5	$-V_S$	V_S−1.8	V
Common-mode rejection	k_{CMR}	80	85		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of I_{IO} $R_G = 50$ Ω Temperature coefficient of V_{IO} $R_G = 50$ Ω	α_{IIO} α_{VIO}		0.1 6	0.8 25			nA/K µV/K
Slew rate for non-inverting operation[1] Slew rate for inverting operation[1]	SR SR		20 30				V/µs V/µs

Characteristics

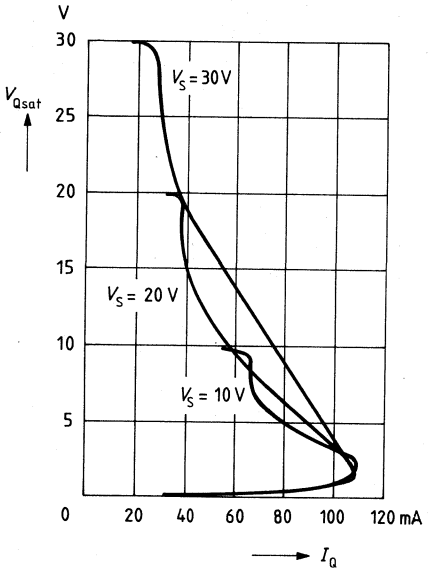
$V_S = \pm 2$ V, $R_l = 10$ kΩ

Input offset voltage $R_G = 50$ Ω	V_{IO}	−4		4	−6	6	mV
Input offset current Input current	I_{IO} I_I	−10	 40	50 100	10	75 150	nA nA
Open-loop voltage gain	G_{V0}	75			70		dB

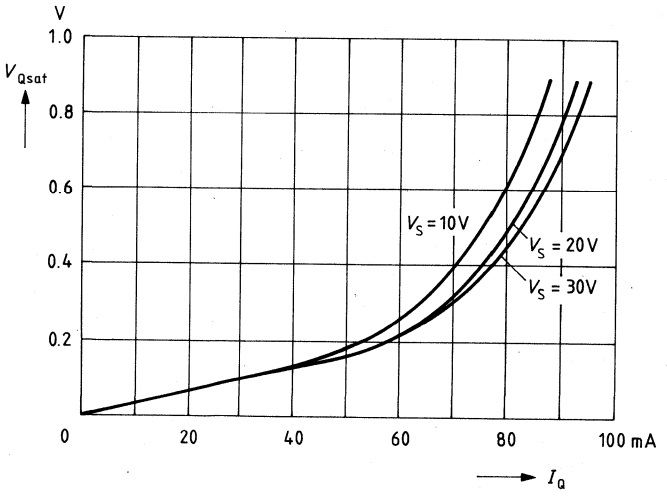
[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

Typical Characteristics of Electrical Parameters

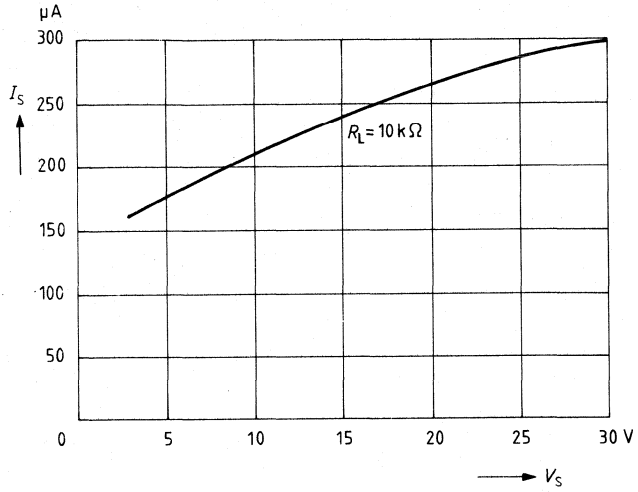
Load characteristics
Output saturation voltage versus output current



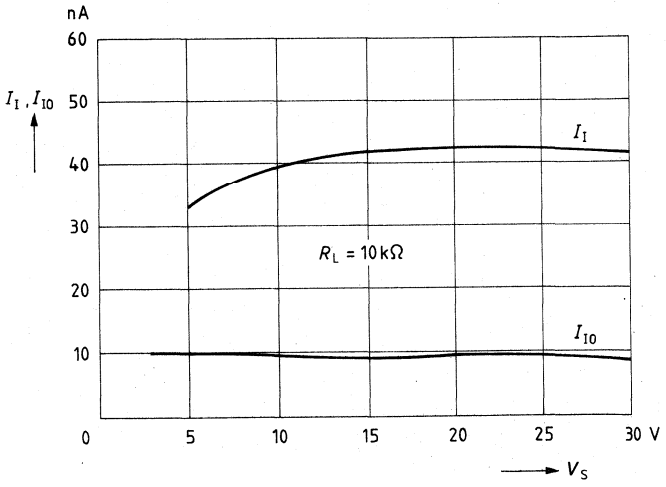
Output saturation voltage versus output current



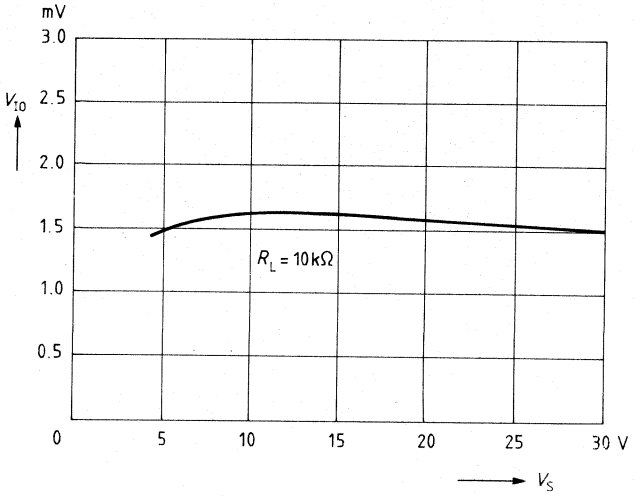
Supply current versus supply voltage



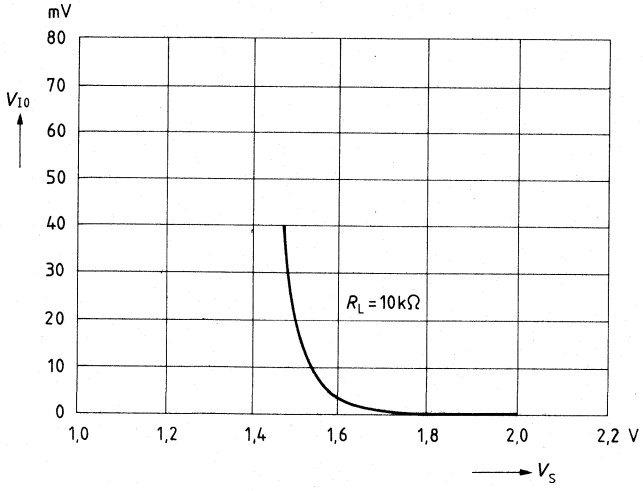
Input current and input offset current versus supply voltage



Input offset voltage versus supply voltage



V_{IO} behavior at low operating voltages
Input offset voltage versus supply voltage



Bipolar IC

Type	Ordering Code	Package	Color Code
TBA 221 B	Q67000-A281	P-DIP-8	–
TBA 222 B	Q67000-A2280	P-DIP-8	–
TBA 222 B S1	Q67000-A8057	P-DIP-8	–
S TBB 0741 G	Q67000-A1498	similar to P-DSO-8 (SMD)	blue/brown
TBB 0742 G	Q67000-A2395-G403	similar to P-DSO-8 (SMD)	red/green

These op amps are short-circuit proof to $+V_S$, $-V_S$. The input offset voltage can be very easily compensated. Very few external components are required due to the internal frequency compensation. The gain reduction by 6 dB/octave yields a very good stability.

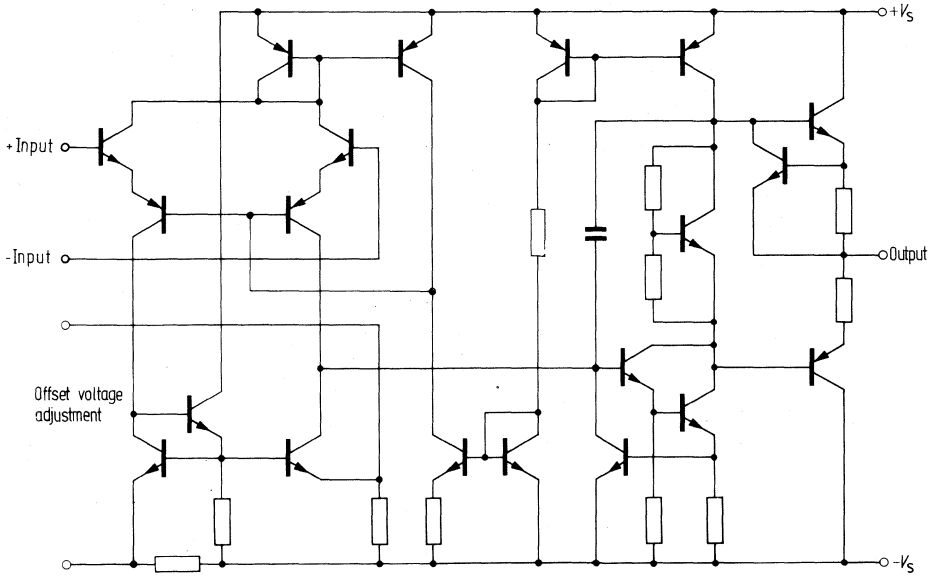
Features

- NPN input
- High differential input voltage
- Short-circuit proof
- High voltage gain
- High supply voltage, 44 V
- Wide temperature range (TBA 222, TBB 0742)
- Push-pull output
- B S1-version for high quality

Applications

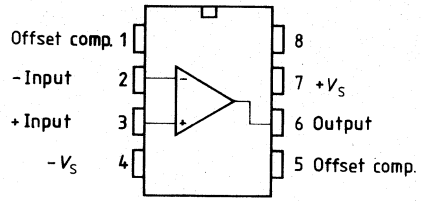
- Amplifier
- Comparator

Circuit Diagram

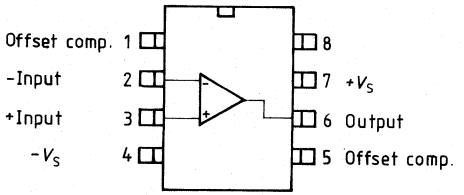


Pin Configurations
(top view)

TBA 221 B
TBA 222 B
TBA 222 B S1



TBB 0741 G
TBB 0742 G



Maximum Ratings

Description	Symbol	TBA 221 TBB 0741	TBA 222 TBB 0742	Unit
Supply voltage	V_S	±18	±22	V
Input voltage: $V_S = \pm 4$ to ± 15 V $V_S \geq 15$ V	V_I V_I	$\pm V_S$ ±15	$\pm V_S$ ±15	V V
Differential input voltage	V_{ID}	±30	±30	V
Output short-circuit duration[1])	t_{QSC}	∞	∞	
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	150 −65 to 150	°C °C
Thermal resistance system – air TBA 221B/222B; BS1 TBB 0741 G/0742 G	 $R_{th\ SA}$ $R_{th\ SA}$	 100 200	 100 200	 K/W K/W

Operating Range

Supply voltage	V_S	±4 to ±18	±4 to ±22	V
Ambient temperature	T_A	0 to 70	−55 to 125	°C

[1]) Short circuit may be to $+V_S$, $-V_S$, or 0, whereby maximum ratings like T_j must not be exceeded.

Characteristics

$V_S = \pm 15$ V

Description	Symbol	$T_A = 25$ °C min	$T_A = 25$ °C typ	$T_A = 25$ °C max	$T_A = 0$ °C to 70 °C min	$T_A = 0$ °C to 70 °C max	Unit
Input offset voltage $R_G \leq 10$ kΩ	V_{IO}	−6		6	−7.5	7.5	mV
Setting range of V_{IO}	V_{IO}	6	±15	−6			mV
Input offset current	I_{IO}	−200	±20	200	−300	300	nA
Input current	I_I		80	500		800	nA
Supply current	I_S		1.7	2.8		2.8	mA
Pos. output short-circuit current	I_{QSC+}	15	20	25			mA
Neg. output short-circuit current	I_{QSC-}	−25	−20	−15			mA
Input resistance	R_I	300	2000				kΩ
Input capacitance	C_I		1.4				pF
Output resistance	R_Q		75				Ω
Control range $R_G \geq 10$ kΩ $R_L \geq 2$ kΩ	 $V_{Q\,pp}$ $V_{Q\,pp}$	 13 11	 ±14 ±13	 −12.5 −11			 V V
Common-mode input voltage range	V_{IC}	$-V_S+3$		V_S-3			V
Open-loop voltage gain $V_{Q\,pp} = \pm 10$ V, $R_L \geq 2$ kΩ	G_{V0}	86	100		84		dB
Common-mode rejection ($R_G \leq 10$ kΩ)	k_{CMR}	70	90				dB
Supply voltage rejection	k_{SVR}		30	150			μV/V
Transient response of output voltage at $G_V = 1$: Rise time, $V_I = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF	t_r		0.3				μs
Overshoot			5				%
Slew rate[1] $R_L \leq 2$ kΩ	SR		0.5				V/μs
Temperature coefficient of V_{IO}	α_{VIO}		3				μV/K
Temperature coefficient of I_{IO}	α_{IIO}		0.4				nA/K

[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

Characteristics

$V_S = \pm 15$ V

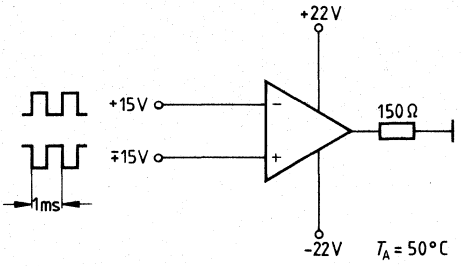
Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -55$ to 125 °C min	max	Unit
Input offset voltage $R_G \leq 10$ kΩ	V_{IO}	−4		4	−5.5	5.5	mV
Setting range of V_{IO}	V_{IO}	6	±15	−6			mV
Input offset current	I_{IO}	−100	±20	100	−400	400	nA
Input current	I_I		80	350		1200	nA
Supply current	I_S		1.7	2.8		2.8	mA
Pos. output short-circuit current	I_{QSC+}	15	20	25			mA
Neg. output short-circuit current	I_{QSC-}	−25	−20	−15			mA
Input resistance	R_I	300	2000				kΩ
Input capacitance	C_I		1.4				pF
Output resistance	R_Q		75				Ω
Control range $R_L \geq 10$ kΩ	$V_{Q\,pp}$	13	±14	−12.5			V
$R_L \geq 2$ kΩ	$V_{Q\,pp}$	11	±13	−11			V
Common-mode input voltage range	V_{IC}	$-V_S+3$		V_S-3			V
Open-loop voltage gain $V_{Q\,pp} = \pm 10$ V, $R_L \geq 2$ kΩ	G_{V0}	94	106		88		dB
Common-mode rejection $R_G \leq 10$ kΩ	k_{CMR}	80	90				dB
Supply voltage rejection	k_{SVR}		30	100			μV/V
Transient response of output voltage at $G_V = 1$: Rise time, $V_I = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF	t_r		0.3				μs
Overshoot			5				%
Slew rate[1] $R_L \leq 2$ kΩ	SR		0.5				V/μs
Temperature coefficient of V_{IO}	α_{VIO}		3				μV/K
Temperature coefficient of I_{IO}	α_{IIO}		0.4				nA/K

[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

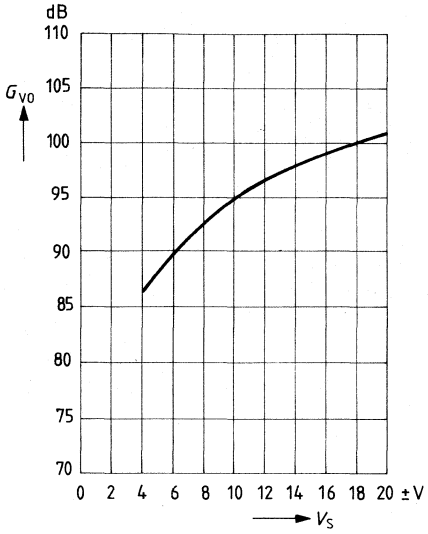
TBA 222 B S1 similar to TBA 222 B, however, with special quality features.

1. 72 hours electrically preaged at $T_A = 50\,°C$, $V_S \pm 22$ V corresponding to the circuit shown below
2. Noise < 5 µVs in accordance with DIN 45405

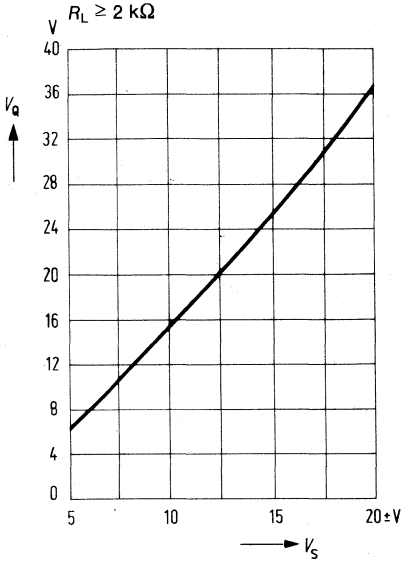
Circuit, Preageing for TBA 222 BS1



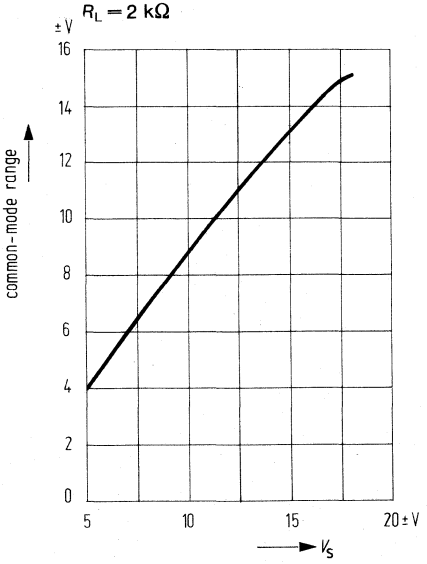
Open-loop voltage gain versus supply voltage



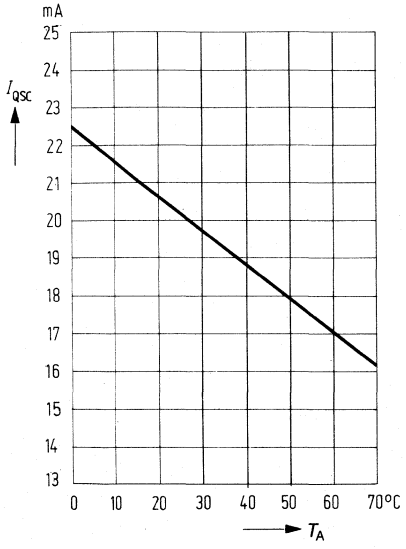
Output voltage versus supply voltage
$R_L \geq 2$ kΩ



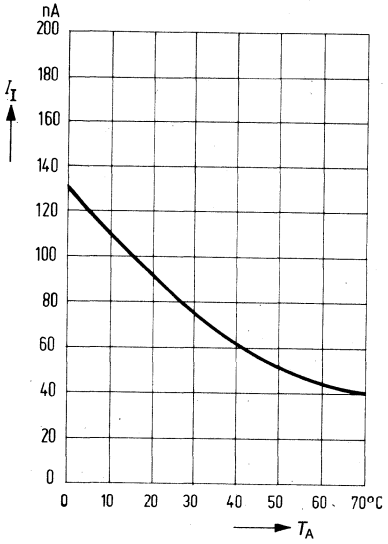
Common-mode range versus supply voltage
$R_L = 2$ kΩ



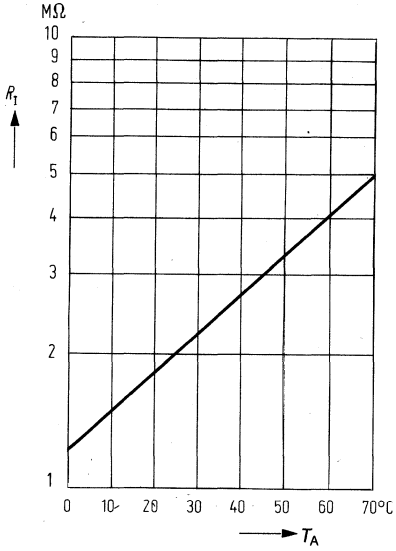
Output short-circuit current versus ambient temperature



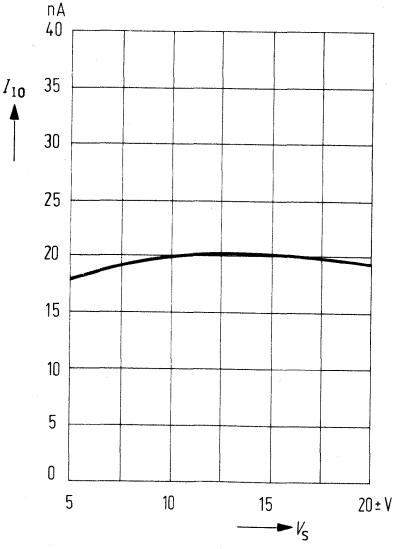
Input current versus ambient temperature
$V_S = \pm 15$ V



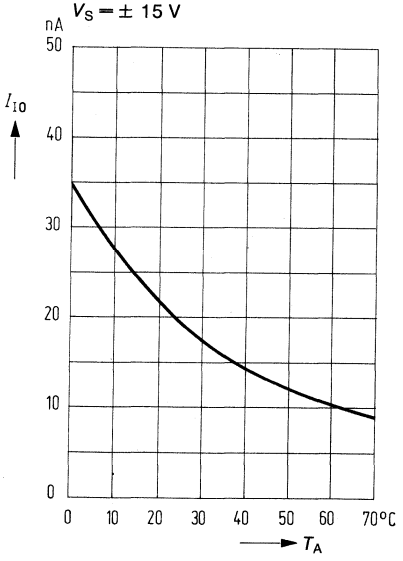
Input resistance versus ambient temperature
$V_S = \pm 15$ V



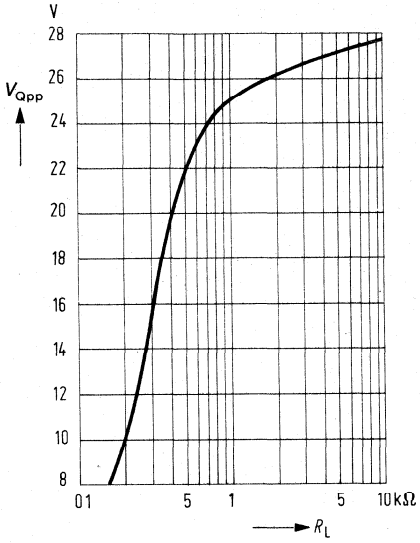
Input offset current versus supply voltage



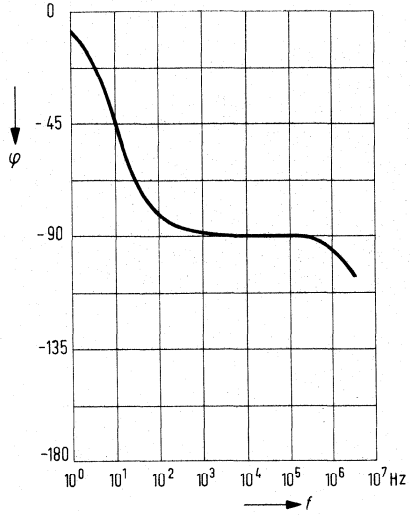
Input offset current versus ambient temperature
$V_S = \pm 15$ V



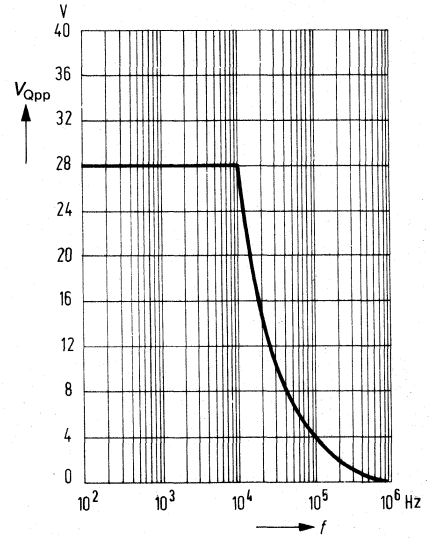
Output voltage versus load resistance
$V_S = \pm 15$ V



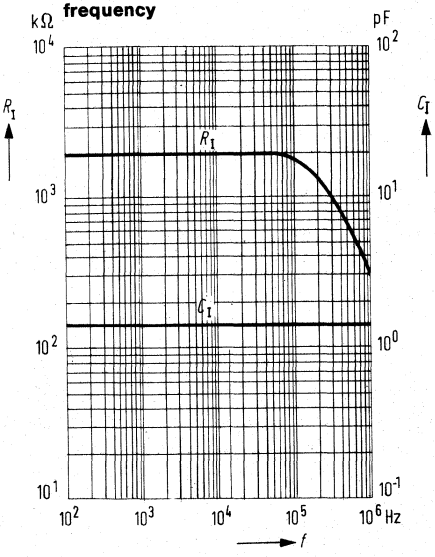
Phase response of open-loop voltage gain
Phase versus frequency
$V_S = \pm 15$ V



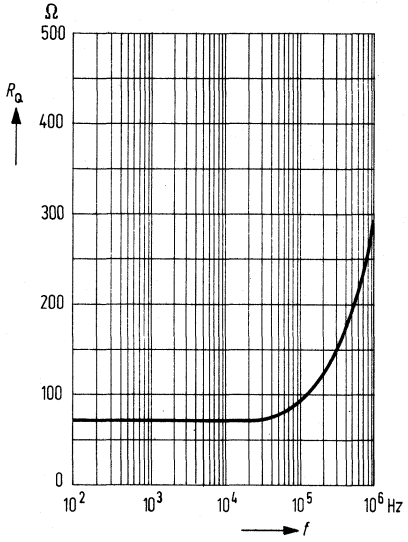
Output voltage versus frequency
$V_S = \pm 15$ V; $R_L = 10$ kΩ



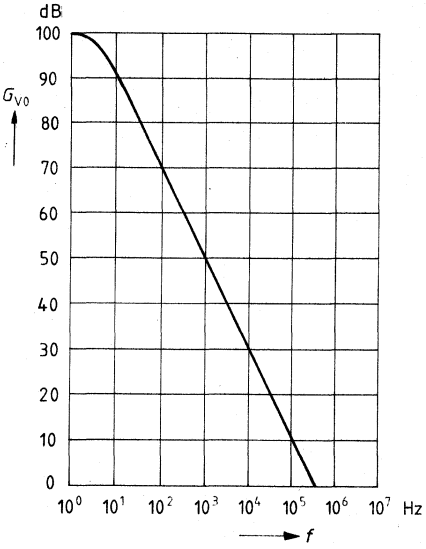
Input resistance and input capacitance versus frequency



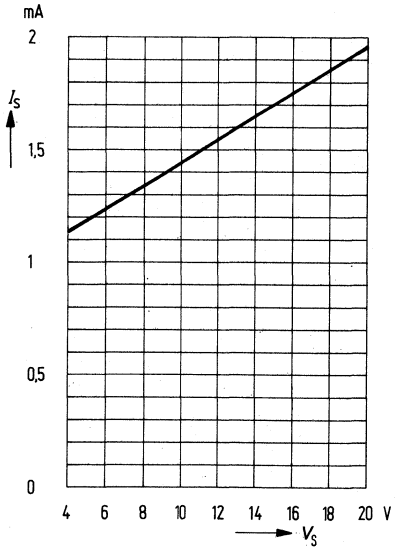
Output resistance versus frequency



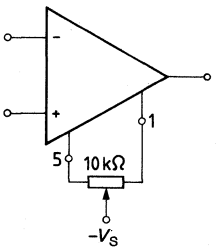
Open-loop voltage gain versus frequency



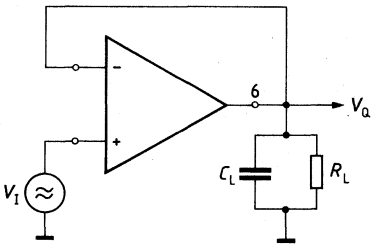
Supply current versus supply voltage



Offset voltage adjustment circuit



Transient response



Type	Ordering Code	Package
TAA 2762 A	Q67000-A2499	P-DIP-8
TAA 2765 A	Q67000-A1031	P-DIP-8

These op amps are particularly economic and versatile. Owing to their excellent performance qualities they are well suited for a wide scope of applications, as in control engineering, automotive electronics, AF circuits, analog computers, etc.

Features

- Wide common-mode range
- Large supply voltage range
- Wide temperature range (TAA 2762 A)
- High output current
- Large control range
- Internally frequency-compensated
- NPN inpute with protection diodes
- Open collector output

Applications

- Amplifier
- Comparator
- Level converter
- Driver

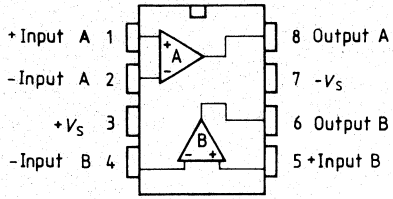
Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	±15	V
Output current	I_Q	70	mA
Differential input voltage	V_{ID}	$\pm V_S$	
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air TAA 2762 A/2765 A	$R_{th\ SA}$	100	K/W

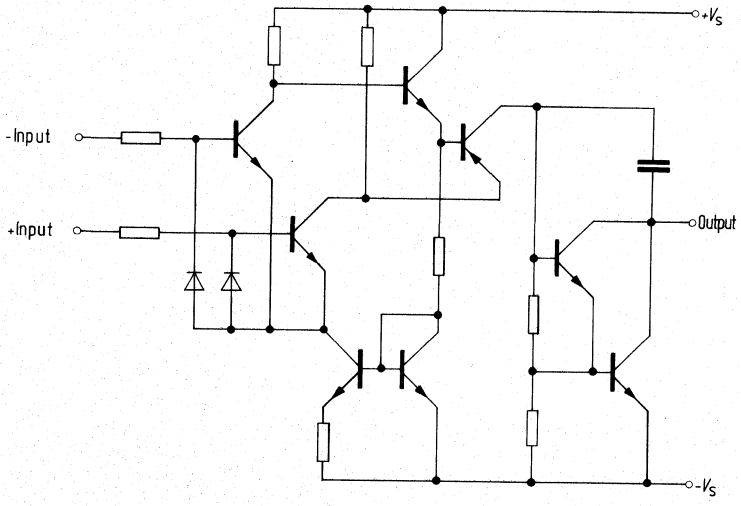
Operating Range

Supply voltage	V_S	±2 to ±15	V
Ambient temperature TAA 2762 A	T_A	−55 to 125	°C
Ambient temperature TAA 2765 A	T_A	−25 to 85	°C

Pin Configuration
(top view)



Circuit Diagram of a Single Op Amp



Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ,
unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -55$ to 125 °C min	max	Unit
Open-loop supply current consumption, total	I_S		0.5	1.5		1.5	mA
Input offset voltage, $R_G = 50$ Ω	V_{IO}	−4		4	−6	6	mV
Input offset current Input current	I_{IO} I_I	−100	±50 0.3	100 0.7	−300	300 1.0	nA µA
Control range $V_S = \pm 15$ V $R_L = 620$ Ω, $V_S = \pm 15$ V	 $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9		 −14 −12.5	 14.8 14.8	 −14 −12	 V V
Input impedance, $f = 1$ kHz	Z_i		200				kΩ
Open-loop voltage gain $f = 100$ kHz $R_L = 10$ kΩ, $f = 100$ Hz	 G_{V0} G_{V0}	 85	 87 92		 80		 dB dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	80	85			75	dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		1 0.3	15 1.5		25 1.5	µV/K nA/K
Noise voltage (in acc. with DIN 45405; referred to input; $R_S = 2.5$ kΩ)	V_n		3				µV
Output saturation voltage $I_Q = 10$ mA	V_{Qsat}			1			V
Slew rate for non-inverting operation[1] Slew rate for inverting operation[1]	SR SR		0.5 0.5				V/µs V/µs

Characteristics

$V_S = \pm 2$ V, $R_L = 2$ kΩ

Input offset voltage, $R_G = 50$ Ω	V_{IO}	−4		4	−6	6	mV
Input offset current Input current	I_{IO} I_I	−70	 0.2	70 0.5	−200	200 0.8	nA µA
Open-loop voltage gain $f = 100$ Hz	G_{V0}	80			75		dB

[1]) For the relationship between bandwidth and slew rate refer to **"General information"**

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ,
unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -25$ to 85 °C min	max	Unit
Open-loop supply currrent consumption, total	I_S		0.5	1.5		1.5	mA
Input offset voltage, $R_G = 50$ Ω	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current Input current	I_{IO} I_I	−200	±80 0.5	200 0.8	−300	300 1.0	nA µA
Control range $V_S = \pm 15$ V $R_L = 620$ Ω, $V_S = \pm 15$ V	 $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9		 −14 −12.5	 14.8 14.8	 −14 −12	 V V
Input impedance, $f = 1$ kHz	Z_i		200				kΩ
Open-loop voltage gain $f = 100$ Hz $R_L = 10$ kΩ, $f = 100$ Hz	 G_{V0} G_{V0}	 80	 85 90		 80		 dB dB
Output reverse current	I_{QR}			10		20	µA
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	75	83		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		1 0.3	15		25 1.5	µV/K nA/K
Noise voltage (in acc. with DIN 45405; referred to input; $R_S = 2.5$ kΩ)	V_n		3				µV
Output saturation voltage $I_Q = 10$ mA	V_{Qsat}			1			V
Slew rate for non-inverting operation[1] Slew-rate for inverting operation[1]	SR SR		0.5 0.5				V/µs V/µs

Characteristics

$V_S = \pm 2$ V, $R_L = 2$ kΩ

Input offset voltage, $R_G = 50$ Ω	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current Input current	I_{IO} I_I	−150	 0.2	150 0.6	−200	200 0.8	nA µA
Open-loop voltage gain $f = 100$ Hz	G_{V0}	75			75		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

Type	Ordering Code	Package
TBC 2332 B	Q67000-A2500	P-DIP-8
TBE 2335 B	Q67000-A1165	P-DIP-8

These op amps are economic and versatile. Owing to their excellent performance qualities, they are well suited for a wide scope of applications, as in measurement and control engineering, automotive electronics, AF circuits, analog computers, etc. The low input current of these amplifiers is particularly advantageous for measurement and control systems.

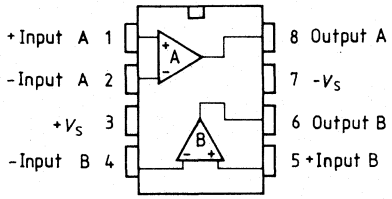
Features

- High input impedance
- Wide common-mode range
- Large supply voltage range
- Large control range
- High output current
- Wide temperature range (TBC 2332 B)
- Open collector output
- NPN Darlington input
- Low input current
- Internally frequency-compensated

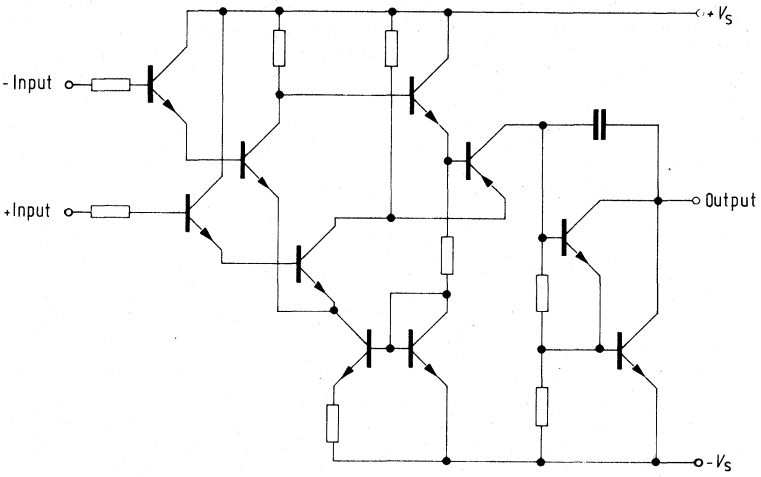
Applications

- Amplifier
- Comparator
- Level converter
- Impedance converter
- Driver

Pin Configuration
(top view)



Circuit Diagram of a Single Op Amp



Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	±15	V
Output current	I_Q	70	mA
Differential input voltage $V_S = \pm 13$ to ± 15 V $V_S = \pm$ 2 to ± 13 V	 V_{ID} V_{ID}	 ±13 $\pm V_S$	V
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air	$R_{th\ SA}$	100	K/W

Operating Range

Supply voltage	V_S	±2 to ±15	V
Ambient temperature	T_A	−55 to 125	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V

		$T_A = 25$ °C			$T_A = -55$ to 125 °C		
Description	Symbol	min	typ	max	min	max	Unit
Open-loop supply current consumption, total	I_S		0.5	1.5		1.5	mA
Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−10		10	−15	15	mV
Input offset current Input current	I_{IO} I_I	−5	 5	5 15	−10	10 25	nA nA
Control range $R_L = 2$ kΩ, $V_S = \pm 15$ V $R_L = 620\ \Omega$, $V_S = \pm 15$ V	 $V_{Q\ pp}$ $V_{Q\ pp}$	 14.9 14.9		 −14 −12.5	 14.8 14.8	 −14 −12	 V V

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ, unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -55$ to 125 °C min	max	Unit
Input impedance $f = 1$ kHz	Z_i		3				MΩ
Open-loop voltage gain $f = 100$ Hz $R_L = 10$ kΩ, $f = 100$ Hz	 G_{V0} G_{V0}	 80	 83 88	 	 75	 	 dB dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range	V_{IC}	V_S		$-V_S+2.0$	V_S	$-V_S+3$	V
Common-mode rejection	k_{CMR}	75	80		70		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		4 50	25		50	µV/K pA/K
Output saturation voltage $I_Q = 10$ mA	$V_{Q\,sat}$			1			V
Slew rate for non-inverting operation[1] Slew rate for inverting operation[1]	SR SR		0.5 0.5				V/µs V/µs
Characteristis $V_S = \pm 2$ V, $R_L = 2$ kΩ							
Input offset voltage $R_G = 50$ Ω	V_{IO}	−10		10	−15	15	mV
Input offset current Input current	I_{IO} I_I	−5	 5	5 15	−10	10 25	nA nA
Open-loop voltage gain $f = 100$ Hz	G_{V0}	75			70		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	±15	V
Output current	I_Q	70	mA
Differential input voltage $V_S = \pm 13$ to ± 15 V $V_S = \pm 2$ to ± 13 V	 V_{ID} V_{ID}	 ±13 $\pm V_S$	V
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air	$R_{th\ SA}$	100	K/W

Operating Range

Supply voltage	V_S	±2 to ±15	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V, $R_L = 2$ kΩ

		$T_A = 25$ °C			$T_A = -25$ to 85 °C		
Description	Symbol	min	typ	max	min	max	Unit
Open-loop supply current consumption, total	I_S		0.5	1.5		1.5	mA
Input offset voltage $R_G = 50$ Ω	V_{IO}	−15		15	−18	18	mV
Input offset current Input current	I_{IO} I_I	−10	 5	10 25	−20	20 35	nA nA
Control range $V_S = \pm 15$ V $R_L = 620$ Ω, $V_S = \pm 15$ V	 $V_{Q\ pp}$ $V_{Q\ pp}$	 14.9 14.9		 −14 −12.5	 14.8 14.8	 −14 −12	 V V

Characteristics
$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ,
unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -25$ to 85 °C min	max	Unit
Input impedance $f = 1$ kHz	Z_i		3				MΩ
Open-loop voltage gain $f = 100$ Hz $R_L = 10$ kΩ, $f = 100$ Hz	 G_{V0} G_{V0}	 75	 80 85	 	 75	 	 dB dB
Output reverse current	I_{QR}			10		20	μA
Common-mode input voltage range	V_{IC}	$-V_S+2.0$		$V_S-0.5$	$-V_S+3$	$-V_S-0.8$	V
Common-mode rejection	k_{CMR}	70	78		70		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	μV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		4 50	25		50	μV/K pA/K
Output saturation voltage $I_Q = 10$ mA	$V_{Q\,sat}$			1			V
Slew rate for non-inverting operation[1]) Slew rate for inverting operation[1])	SR SR		0.5 0.5				V/μs V/μs

Characteristics
$V_S = \pm 2$ V, $R_L = 2$ kΩ

Input offset voltage $R_G = 50$ Ω	V_{IO}	−17		17	−20	20	mV
Input offset current Input current	I_{IO} I_i	−10	 5	10 25	−20	20 35	nA nA
Open-loop voltage gain $f = 100$ Hz	G_{V0}	70			70		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

Type	Ordering Code	Package	Color Code
S TAE 2453 A	Q67000-A2107	P-DIP 8	–
S TAE 2453 G	Q67000-A2108	similar to P-DSO-8 (SMD)	white
S TAF 2453 A	Q67000-A2210	P-DIP 8	–
TAF 2453 G	Q67000-A2211	similar to P-DSO-8 (SMD)	green

The TAF 2453/TAE 2453 consists of two independent, frequency-compensated op amps, each having a PNP input differential stage and an open collector output. The integrated regulator provides for all parameters a large degree of independence of the supply voltage.

Features

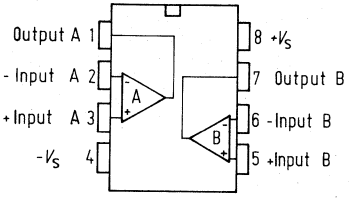
- Supply voltage range between 2 V (1.8 V) and 36 V
- Low current consumption, 0.8 mA typ.
- Extremely large control range
- Low output saturation voltage, almost independent of load current
- Output current up to 70 mA (max. 100 mA)
- Output virtually short-circuit proof
- Wide common-mode voltage range
- Wide operating temperature range (TAF 2453 A; G)
- Pin-compatible to TBB 1458 B
- The characteristic curves of the electric parameters correspond to those of type TAE 1453 A; G

Applications

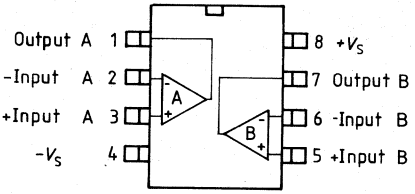
- Amplifier
- Level converter
- Driver
- Zero voltage switch
- Comparator

Pin Configurations
(top view)

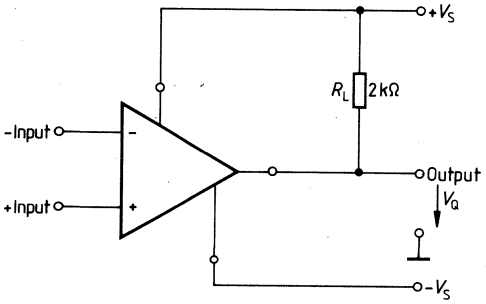
**TAE 2453 A;
TAF 2453 A**



**TAE 2453 G;
TAF 2453 G**

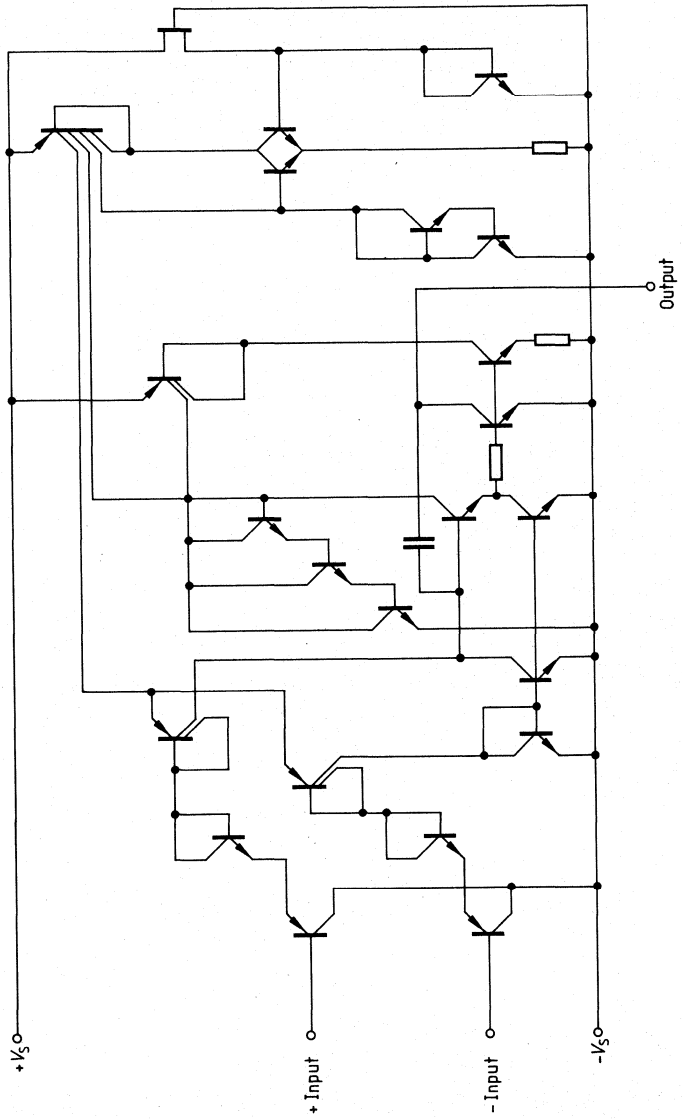


Connection Diagram



R_L = load resistance (collector resistance)

Circuit Diagram



Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	100	mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature	T_j	150	°C
Storage temperature raange	T_{stg}	−55 to 150	°C
Thermal resistance system – air TAE 2453 A	$R_{th\ SA}$	100	K/W
TAE 2453 G	$R_{th\ SA}$	170	K/W

Operating Range

Supply voltage	V_S	± 1.0 to ± 18 (± 0.9 V with slightly increased offset voltage)	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 10$ kΩ,
unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -25$ to 85 °C min	max	Unit
Open-loop supply current consumption, total	I_S		0.8	1.5		1.8	mA
Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current Input current	I_{IO} I_I	−15	 40	15 150	−100	100 200	nA nA
Control range $R_L = 2$ kΩ, $V_S = \pm 15$ V $R_L = 620\ \Omega$, $V_S = \pm 15$ V	 $V_{Q\ pp}$ $V_{Q\ pp}$	 14.9 14.9		 −14.7 −14.5	 14.9 14.9	 −14.7 −14.4	 V V
Input impedance $f = 1$ kHz	Z_i		200				kΩ
Open-loop voltage gain $R_L = 2$ kΩ	G_{V0}	80	85		80		dB
Output reverse current	I_{QR}			10		20	μA
Common-mode input voltage range $R_L = 2$ kΩ	V_{IC}	$-V_S$-0.2		V_S-1.8	$-V_S$	V_S-2.0	V
Common-mode rejection $R_L = 2$ kΩ	k_{CMR}	75	80		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	μV/V
Temperature coefficient of I_{IO} $R_G = 50\ \Omega$	α_{IIO}		0.1				nA/K
Temperature coefficient of V_{IO} $R_G = 50\ \Omega$	α_{VIO}		6				μV/K
Slew rate for non-inverting operation[1] Slew rate for inverting operation[1]	SR SR		1 1				V/μs V/μs

Characteristics $V_S = \pm 2$ V, $R_L = 10$ kΩ

Input offset voltage $R_G = 50\ \Omega$	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current Input current	I_{IO} I_I	−75	 40	75 150	−100	100 200	nA nA
Open-loop voltage gain	G_{V0}	70			70		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	100	mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 150	°C
Thermal resistance system – air TAF 2453 A	$R_{th\ SA}$	100	K/W
TAF 2453 G	$R_{th\ SA}$	170	K/W

Operating Range

Supply voltage	V_S	± 1.0 to ± 18 (± 0.9 with sligthly increased offset voltage)	V
Ambient temperature	T_A	−55 to 125	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 10$ kΩ;
unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -55$ to 125 °C min	max	Unit
Open-loop supply current consumption total	I_S		0.8	1.5		1.8	mA
Input offset voltage $R_G = 50$ Ω	V_{IO}	−4		4	−6	6	mV
Input offset current Input current	I_{IO} I_I	−10	 40	10 100	−75	75 150	nA nA
Control range $R_L = 2$ kΩ, $V_S = \pm 15$ V $R_L = 620$ Ω, $V_S = \pm 15$ V	 $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9		 −14.7 −14.5	 14.8 14.8	 −14.7 −14.4	 V V
Input impedance $f = 1$ kHz	Z_i		200				kΩ
Open-loop voltage gain $R_L = 2$ kΩ	G_{V0}	85	87		80		dB
Output reverse current	I_{QR}			1		5	μA
Common-mode input voltage range	V_{IC}	$-V_S$−0.3		V_S−1.5	$-V_S$	V_S−1.8	V
Common-mode rejection $R_L = 2$ kΩ	k_{CMR}	80	85		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	μV/V
Temperature coefficient of I_{IO} $R_G = 50$ Ω Temperature coefficient of V_{IO} $R_G = 50$ Ω	α_{IIO} α_{VIO}		0.1 6	0.8 25		0.8 25	nA/K μV/K
Slew rate for non-inverting operation[1]) Slew rate for inverting operation[1])	SR SR		1 1				V/μs V/μs

Characteristics

$V_S = \pm 2$ V

Input offset voltage $R_G = 50$ Ω	V_{IO}	−4		4	−6	6	mV
Input offset current Input current	I_{IO} I_I	−50	 40	50 100	−75	75 150	nA nA
Open-loop voltage gain $R_L = 2$ kΩ	G_{V0}	75			70		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

Bipolar IC

Type	Ordering Code	Package	Color Code
TBB 1458 B	Q67000-A1036	P-DIP-8	–
TBB 1458 G	Q67000-A1458	similar to P-DSO-8 (SMD)	orange/orange

The op amp TBB 1458 is outstanding for its large common-mode and differential input voltage range, as well as its short-circuit strength. No external components are required for frequency compensation.

For single amplifier performance refer to the TBA 221 op amp.

Features

- NPN input
- High differential input voltage
- Short-circuit proof
- Push-pull output
- Fully compatible with industrial standard type TBB 1458

Applications

- Amplifier
- Comparator

Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	±18	V
Input voltage[1])	V_I	±15	V
Differential input voltage[2])	V_{ID}	±30	V
Output short-circuit duration[3])	t_{QSC}	∞	
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air TBB 1458 B	$R_{th\ SA}$	100	K/W
TBB 1458 G	$R_{th\ SA}$	170	K/W

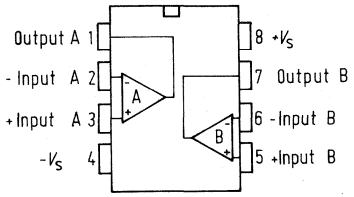
Operating Range

Supply voltage	V_S	±4 to ±18	V
Ambient temperature	T_A	0 to 70	°C

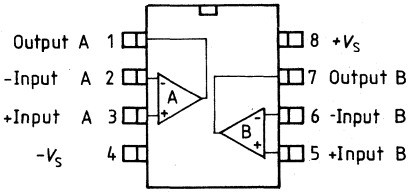
[1]) For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
[2]) For supply voltages less than ±15 V, the maximum differential input voltage is equal to ± (V_S + I V_S- I).
[3]) Short circuit may be to ground or to the supply voltage ± V_S, whereby the maximum ratings must not be exceeded.

Pin Configurations
(top view)

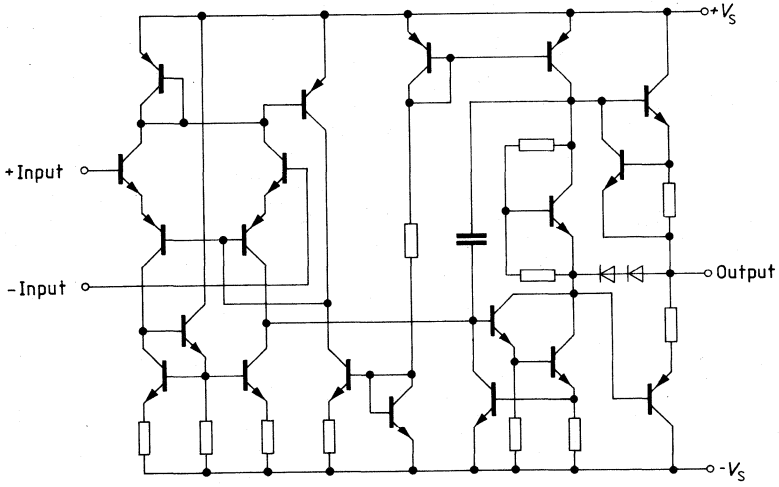
TBB 1458 B



TBB 1458 G



Circuit Diagram of a Single Op Amp



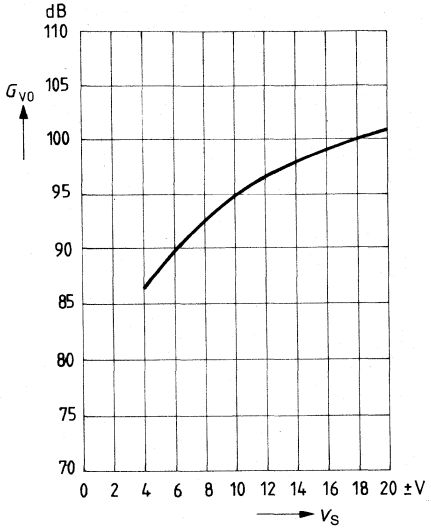
Characteristics

$V_S = \pm 15$ V

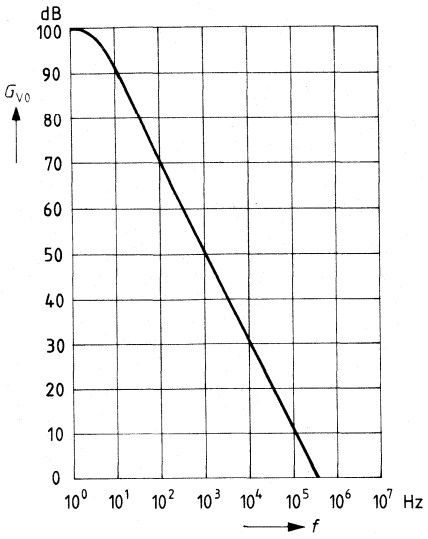
Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = 0$ °C to 70 °C min	max	Unit
Input offset voltage $R_G \leq 10$ kΩ	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current Input current Open-loop supply current consumption, total Output short-circuit current	I_{IO} I_I I_S I_{QSC}	−200	±20 80 2 ±18	200 500 3	−300	300 800 3	nA nA mA mA
Input resistance	R_I	0.3	1				MΩ
Input capacitance	C_I		6				pF
Output resistance	R_Q		75				Ω
Control range $R_L \geq 10$ kΩ $R_L \geq 2$ kΩ	$V_{Q\,pp}$ $V_{Q\,pp}$	13 11	±14 ±13	−13 −11			V V
Common-mode input voltage range	V_{IC}	$-V_S+3$		V_S-3			V
Voltage gain $V_{Q\,pp} = \pm 10$ V, $R_L = 2$ kΩ	G_V	86	100		84		dB
Common-mode rejection $R_G \leq 10$ kΩ	k_{CMR}	70	90				dB
Supply voltage rejection	k_{SCR}		30	150		150	µV/V
Temperature coefficient of V_{IO} Temperature coefficient of I_{IO}	α_{VIO} α_{IIO}		3 0.4				µV/K nA/K
Slew rate[1] $G_V = 1$, $R_L \geq 2$ kΩ	SR		0.5				V/µs

[1] For the relationship between power bandwidth and slew rate refer to **"General information"**

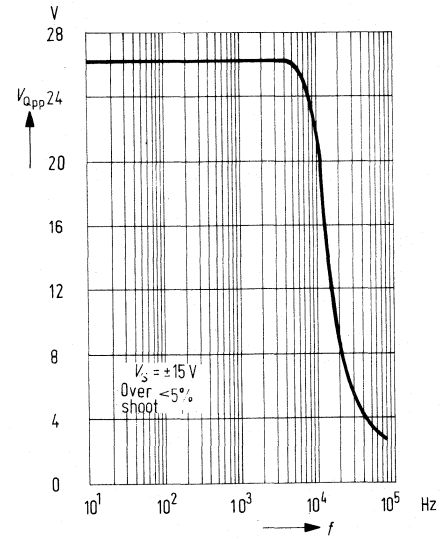
Open-loop voltage gain versus supply voltage



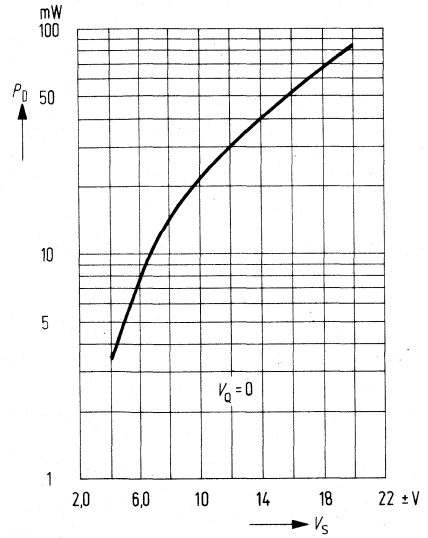
Open-loop voltage gain versus frequency



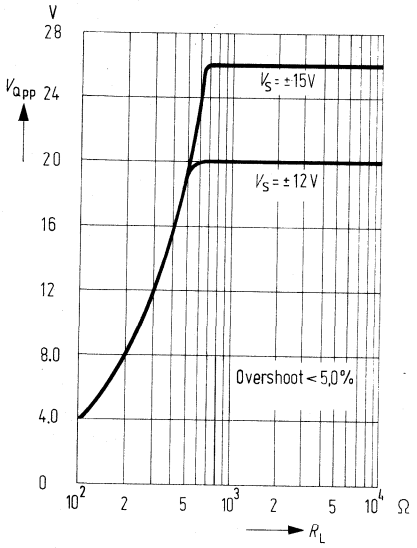
Power bandwidth
Output voltage versus frequency

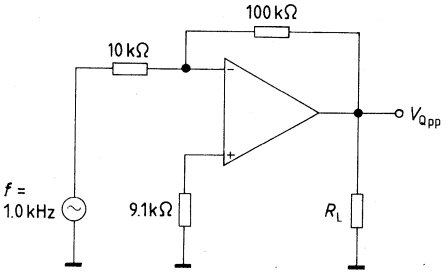


Power dissipation versus supply voltage

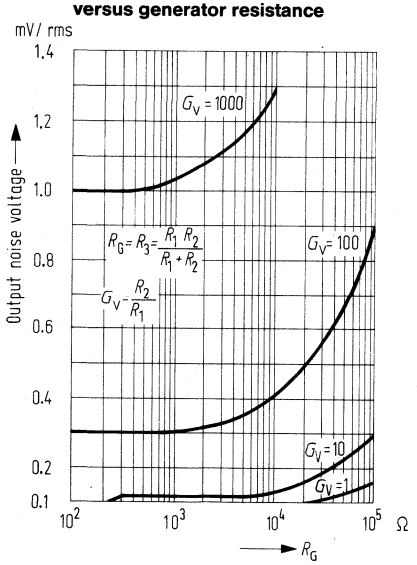


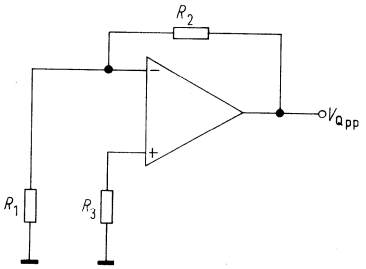
Output voltage versus load resistance





Output noise voltage versus generator resistance





For further characteristic curves refer to TBA 221.

Type	Ordering Code	Package
TAA 4762 A	Q67000-A2502	P-DIP-14
TAA 4765 A	Q67000-A1033	

These op amps are particularly economic and versatile. Owing to their excellent performance qualities, they are well suited for a wide scope of applications, as in control engineering, automotive electronics, AF circuits, analog computers, etc.

Features

- Wide common-mode range
- Large supply voltage range
- Comprehensive protection against destruction
- High output current
- Large control range
- Internal frequency compensation
- Wide temperature range (TAA 4762 A)
- Open collector output

Applications

- Amplifier
- Comparator
- Level converter
- Driver

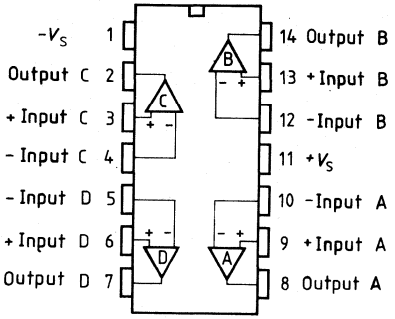
Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	±15	V
Output current	I_Q	70	mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air	$R_{th\ SA}$	80	K/W

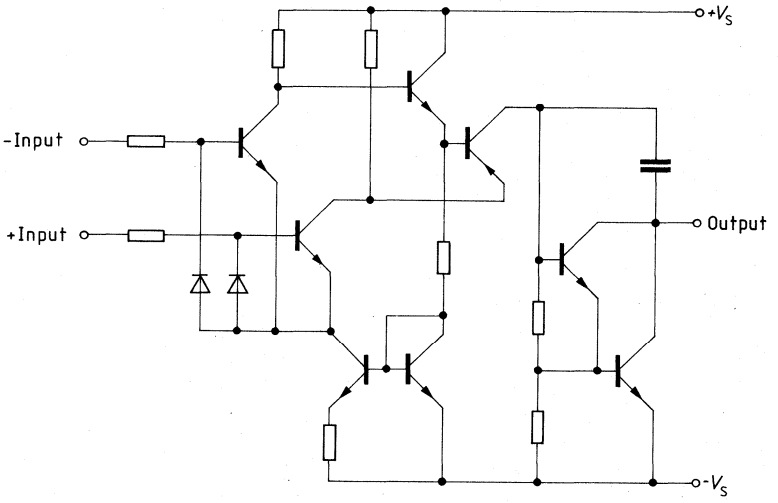
Operating Range

Supply voltage		V_S	±2 to ±15	V
Ambient temperature	TAA 4762 A	T_A	−55 to 125	°C
	TAA 4765 A	T_A	−25 to 85	°C

Pin Configuration
(top view)



Circuit Diagram of a Single Op Amp



Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ,
unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -55$ to 125 °C min	max	Unit
Open-loop supply current consumption, total	I_S		1	3		3	mA
Input offset voltage, $R_G = 50$ Ω	V_{IO}	−4			−6	6	mV
Input offset current Input current	I_{IO} I_I	−100	±50 0.3	100 0.7	−300	300 1.0	nA µA
Control range $V_S = \pm 15$ V $R_L = 620$ Ω, $V_S = \pm 15$ V	 $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9		 −14 −12.5	 14.8 14.8	 −14 −12	 V V
Input impedance, $f = 1$ kHz	Z_I		200				kΩ
Open-loop voltage gain $f = 100$ Hz $R_L = 10$ Ω, $f = 100$ Hz	 G_{V0} G_{V0}	 85	 87 92		 80		 dB dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range	V_{IC}	$-V_2+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	80	85		75		dB
Supply voltage rejection, $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		1 0.3	15 1.5		25 1.5	µV/K nA/K
Noise voltage (in acc. with DIN 45405, referred to input $R_S = 2.5$ Ω)	V_n		3				µV
Output saturation voltage $I_Q = 10$ mA	V_{Qsat}			1			V
Slew rate for non-inverting operation[1]) Slew rate for inverting operation[1])	SR SR		0.5 0.5				V/µs V/µs

Characteristics

$V_S = \pm 2$ V, $R_L = 2$ kΩ

Input offset voltage, $R_G = 50$ Ω	V_{IO}	−4		4	−6	6	mV
Input offset current Input current	I_{IO} I_I	−70	 0.2	70 0.5	−200	200 0.8	nA µA
Open-loop voltage gain $f = 100$ Hz	G_{V0}	80			75		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ,
unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -25$ to 85 °C min	max	Unit
Open-loop supply current consumption, total	I_S		1	3		3	mA
Input offset voltage, $R_G = 50$ Ω	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current Input current	I_{IO} I_I	−200	±80 0.5	200 0.8	−300	300 1.0	nA µA
Control range $V_S = \pm 15$ V $R_L = 620$ Ω, $V_S = \pm 15$ V	 $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9		 −14 −12.5	 14.8 14.8	 −14 −12	 V V
Input impedance, $f = 1$ kHz	Z_i		200				kΩ
Open-loop voltage gain $f = 100$ Hz $R_L = 10$ kΩ, $f = 100$ Hz	 G_{V0} G_{V0}	 80	 85 90	 	 80	 	 dB dB
Output reverse current	I_{QR}			10		20	µA
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	75	83		75		dB
Supply voltage rejection, $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		1 0.3	15		25	µV/K nA/K
Noise voltage (in acc. with DIN 45405, referred to input $R_S = 2.5$ Ω)	V_n		3				µV
Output saturation voltage $I_Q = 10$ mA	V_{Qsat}			1			V
Slew rate for non-inverting operation[1]) Slew rate for inverting operation[1])	SR SR		0.5 0.5				V/µs V/µs

Characteristics

$V_S = \pm 2$ V, $R_L = 2$ kΩ

Input offset voltage, $R_G = 50$ Ω	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current Input current	I_{IO} I_I	−150	 0.2	150 0.6	−200	200 0.8	nA µA
Open-loop voltage gain $f = 100$ Hz	G_{V0}	75			75		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

Type	Ordering Code	Package
TBC 4332 A	Q67000-A2503	P-DIP-14
TBE 4335 A	Q67000-A1167	P-DIP-14

These op amps are economic and versatile. Owing to their excellent performance qualities, they are well suited for a wide scope of applications, as in control engineering, automotive electronics, AF circuits, analog computers, etc. The low input current of these amplifiers is particularly advantageous for application in control systems.

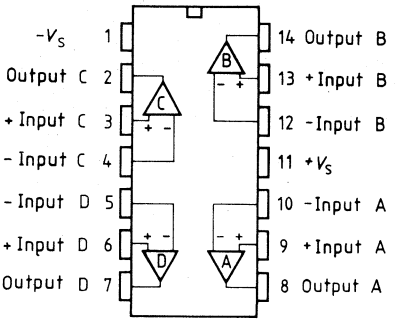
Features

- High input impedance
- Wide common-mode range
- Large supply voltage range
- Large control range
- High output current
- Wide temperature range (TBC 4332A)
- NPN Darlington input
- Open collector output
- Low input current
- Internal frequency compensation

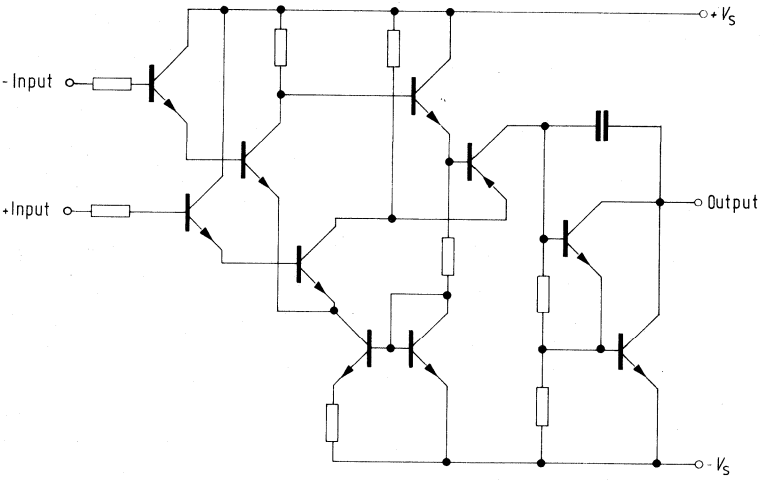
Applications

- Amplifier
- Comparator
- Level converter
- Impedance converter
- Driver

Pin Configuration
(top view)



Circuit Diagram of a Single Op Amp



Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	±15	V
Output current	I_Q	70	mA
Differential input voltage, $V_S = \pm 13$ to ± 15 V Differential input voltage, $V_S = \pm$ 2 to ± 13 V	V_{ID} V_{ID}	±13 $\pm V_S$	V V
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air	$R_{th\ SA}$	80	K/W

Operating Range

Supply voltage	V_S	±2 to ±15	V
Ambient temperature	T_A	−55 to 125	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ,
unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -55$ to 125 °C min	max	Unit
Open-loop supply current consumption, total	I_S		1	3		3	mA
Input offset voltage $R_G = 50$ Ω	V_{IO}	−10		10	−15	15	mV
Input offset current Input current	I_{IO} I_I	−5	 5	5 15	−10	10 25	nA nA
Control range $V_S = \pm 15$ V $R_L = 620$ Ω, $V_S = \pm 15$ V	 $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9		 −14 −12.5	 14.8 14.8	 −14 −12	 V V
Input impedance $f = 1$ kHz	Z_i		3				MΩ
Open-loop voltage gain $f = 100$ Hz $R_L = 10$ kΩ, $f = 100$ Hz	 G_{V0} G_{V0}	 80	 83 88		 75		 dB dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range (comparator operation)	V_{IC}	V_S		$-V_S+2.0$	V_S	$-V_S+3$	V
Common-mode rejection	k_{CMR}	75	80		70		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω	α_{VIO}		−4	25		50	µV/K
Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{IIO}		50				pA/K
Output saturation voltage $I_Q = 10$ mA	V_{Qsat}			1			V
Slew rate for non-inverting operation[1] Slew rate for inverting operation[1]	SR SR		0.5 0.5				V/µs V/µs

Characteristics

$V_S = \pm 2$ V, $R_L = 2$ kΩ

Input offset voltage $R_G = 50$ Ω	V_{IO}	−10		10	−15	15	mV
Input offset current Input current	I_{IO} I_I	−5	 5	5 15	−10	10 25	nA nA
Open-loop voltage gain $f = 100$ Hz	G_{V0}	75			70		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	±15	V
Output current	I_Q	70	mA
Differential input voltage, $V_S = \pm 13$ to ± 15 V Differential input voltage, $V_S = \pm$ 2 to ± 13 V	V_{ID} V_{ID}	±13 $\pm V_S$	V V
Junction temperature Storage tempture range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air	$R_{th\ SA}$	80	K/W

Operating Range

Supply voltage	V_S	±2 to ±15	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 2$ kΩ,
unless otherwise specified

Description	Symbol	$T_A = 25$ C min	typ	max	$T_A = -25$ to 85 °C min	max	Unit
Open-loop supply current consumption, total	I_S		1	3		3	mA
Input offset voltage $R_G = 50$ Ω	V_{IO}	−15		15	−18	18	mV
Input offset current	I_{IO}	−10		10	−20	20	nA
Input current	I_I		5	25		35	nA
Control range							
$V_S = \pm 15$ V	$V_{Q\,pp}$	14.9		−14	14.8	−14	V
$R_L = 620$ Ω, $V_S = \pm 15$ V	$V_{Q\,pp}$	14.9		−12.5	14.8	−12	V
Input impedance $f = 1$ kHz	Z_i		3				MΩ
Open-loop voltage gain $f = 100$ Hz	G_{V0}	75	80		75		dB
$R_L = 10$ kΩ, $f = 100$ Hz	G_{V0}		85				dB
Output reverse current	I_{QR}			10		20	μA
Common-mode input voltage range (comparator operation)	V_{IC}	$+V_S$−0.5		$-V_S$+2.0	$+V_S$−0.8	$-V_S$+3	V
Common-mode rejection	k_{CMR}	70	78		70		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	μV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω	α_{VIO}		4	25		50	μV/K
Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{IIO}		50				pA/K
Output saturation voltage $I_Q = 10$ mA	$V_{Q\,sat}$			1			V
Slew rate for non-inverting operation[1]	SR		0.5				V/μs
Slew rate for inverting operation[1]	SR		0.5				V/μs

Characteristics

$V_S = \pm 2$ V, $R_L = 2$ kΩ

Input offset voltage $R_G = 50$ Ω	V_{IO}	−17		17	−20	20	mV
Input offset current	I_{IO}	−10		10	−20	20	nA
Input current	I_I		5	25		35	nA
Open-loop voltage gain $f = 100$ Hz	G_{V0}	70			70		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

Type	Ordering Code	Package
S TAE 4453 A	Q67000-A2109	P-DIP-14
S TAE 4453 G	Q67000-A2152	P-DSO-14 (SMD)
S TAF 4453 A	Q67000-A2212	P-DIP-14
TAF 4453 G	Q67000-A2213	P-DSO-14 (SMD)

The TAE 4453/TAF 4453 consists of four independent, frequency-compensated op amps, each having a PNP input differential stage and an open collector output. The integrated regulator provides for all parameters a large degree of independence of the supply voltage.

Features

- Supply voltage range between 2 V (1.8 V) and 36 V
- Low current consumption, 1.6 mA typ.
- Extremely large control range
- Low output saturation voltage, almost independent of load current
- Output current up to 70 mA (100 mA max.)
- Output virtually short-circuit proof
- Wide common-mode range
- Wide temperature range (TAF 4453 A; G)
- Pin-compatible to LM 324
- The typical characteristics of the electric parameters correspond to those of the TAE 1453 A; G

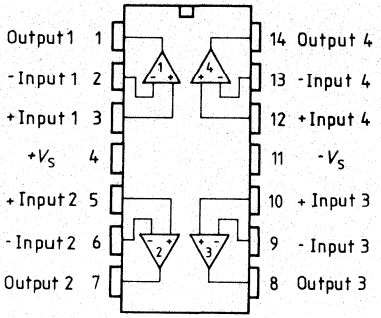
Applications

- Amplifier
- Level converter
- Driver
- Offset voltage switch
- Comparator

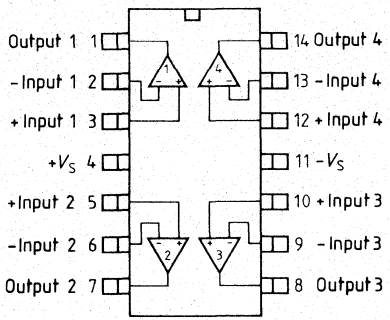
Pin Configurations

(top view)

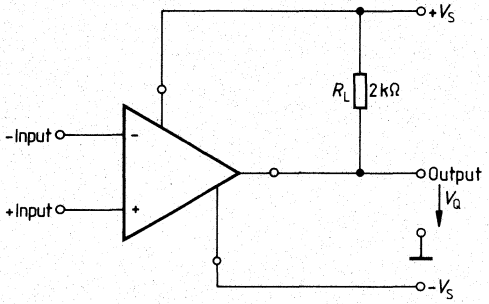
**TAE 4453 A,
TAF 4453 A**



**TAE 4453 G,
TAF 4453 G**

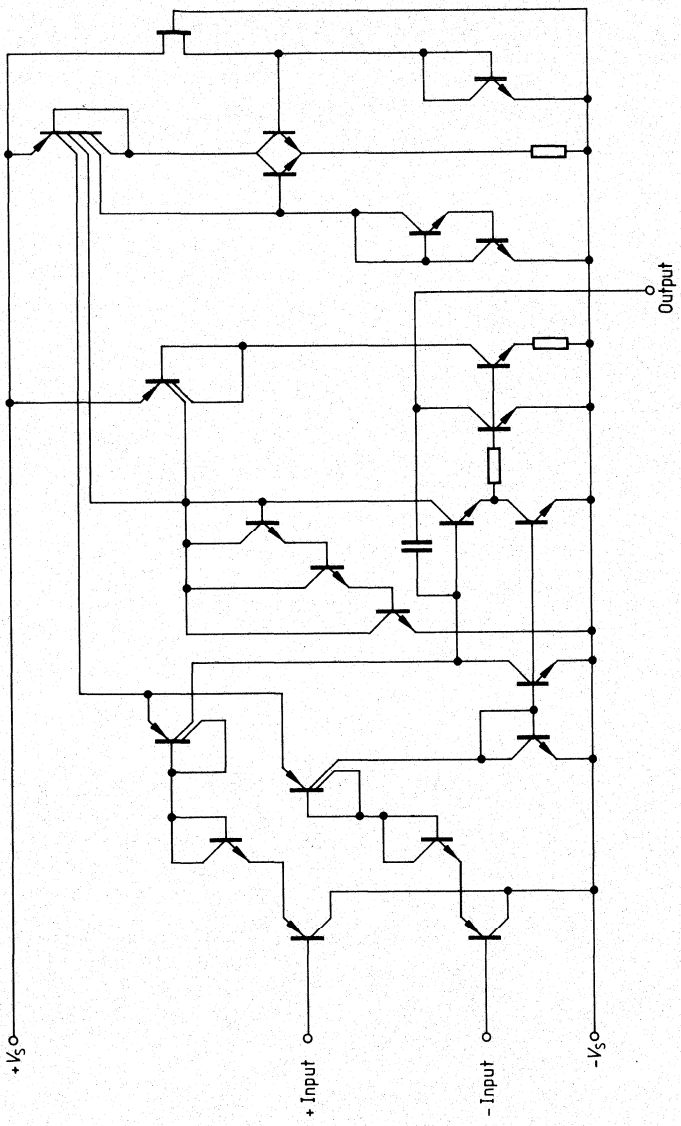


Connection Diagram



R_L = load resistance (collector resistance)

Circuit Diagram



Maximum Ratings

Description		Symbol	Ratings	Unit
Supply voltage		V_S	± 18	V
Output current		I_Q	100	mA
Differential input voltage		V_{ID}	$\pm V_S$	V
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C
Thermal resistance system – air	TAE 4453 A	$R_{th\ SA}$	80	K/W
	TAE 4453 G	$R_{th\ SA}$	120	K/W

Operating Range

Supply voltage	V_S	± 1.0 to ± 18 (± 0.9 V with slightly increased offset voltage)	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 10$ kΩ,
unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -25$ to 85 °C min	max	Unit
Open-loop supply current consumption, total	I_S		1.6	3.0		3.6	mA
Input offset voltage $R_G = 50$ Ω	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current Input current	I_{IO} I_I	15	 40	15 150	−25	25 200	nA nA
Control range $R_L = 2$ kΩ, $V_S = \pm 15$ V $R_L = 620$ Ω, $V_S = \pm 15$ V	 $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9	 	 −14.7 −14.5	 14.9 14.9	 −14.7 −14.4	 V V
Input impedance $f = 1$ kHz	Z_i		200				kΩ
Open-loop voltage gain $R_L = 2$ kΩ	G_{V0}	80	85		80		dB
Output reverse current	I_{QR}			10		20	µA
Common-mode input voltage range $R_L = 2$ kΩ	V_{IC}	$-V_S$−0.2		$+V_S$−1.8	$-V_S$	$+V_S$−2.0	V
Common-mode rejection $R_L = 2$ kΩ	k_{CMR}	75	80		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of I_{IO} $R_G = 50$ Ω Temperature coefficient of V_{IO} $R_G = 50$ Ω	α_{IIO} α_{VIO}		0.1 6				nA/K µV/K
Slew rate for non-inverting operation[1]) Slew rate for inverting operation[1])	SR SR		1 1				V/µs V/µs

Characteristics

$V_S = \pm 2$ V

Input offset voltage $R_G = 50$ Ω	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current Input current	I_{IO} I_I	−75	 40	75 150	−100	100 200	nA nA
Open-loop voltage gain $R_L = 2$ kΩ	G_{V0}	70			70		dB

[1]) For relationship between power bandwidth and slew rate refer to **"General information"**

Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	100	mA
Differential input voltage	V_{ID}	± V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 150	°C
Thermal resistance system – air TAF 4453 A	$R_{th\ SA}$	80	K/W
TAF 4453 G	$R_{th\ SA}$	120	K/W

Operating Range

Supply voltage	V_S	± 1.0 to ± 18 (± 0.9 V with sligthly increased offset voltage)	V
Ambient temperature	T_A	−55 to 125	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R_L = 10$ kΩ,
unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -55$ to 125 °C min	max	Unit
Open-loop supply current consumption, total	I_S		1.6	3.0		3.6	mA
Input offset voltage $R_G = 50$ Ω	V_{IO}	−4		4	−6	6	mV
Input offset current Input current	I_{IO} I_I	−10	 40	10 100	−15	15 150	nA nA
Control range $R_L = 2$ kΩ, $V_S = \pm 15$ V $R_L = 620$ Ω, $V_S = \pm 15$ V	 $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9		 −14.7 −14.5	 14.8 14.8	 −14.7 −14.4	 V V
Input impedance $f = 1$ kHz	Z_i		200				kΩ
Open-loop voltage gain $R_L = 2$ kΩ	G_{V0}	85	87		80		dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range $R_L = 2$ kΩ	V_{IC}	$-V_S$−0.3		$+V_S$−1.5	$-V_S$	$+V_S$−1.8	V
Common-mode rejection $R_L = 2$ kΩ	k_{CMR}	80	85		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of I_{IO} $R_G = 50$ Ω Temperature coefficient of V_{IO} $R_G = 50$ Ω	α_{IIO} α_{VIO}		0.1 6	0.8 25		0.8 25	nA/K µV/K
Slew rate for non-inverting operation[1]) Slew rate for inverting operation[1])	SR SR		1 1				V/µs V/µs

Characteristics

$V_S = \pm 2$ V

Input offset voltage $R_G = 50$ Ω	V_{IO}	−4		4	−6	6	mV
Input offset current Input current	I_{IO} I_I	−50	 40	50 100	−75	75 150	nA nA
Open-loop voltage gain $R_L = 2$ kΩ	G_{V0}	75			70		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

Threshold Switches, Comparators, Current-Monitoring ICs

Selector Guide

Type	Package	Operating range			Electrical characteristics $V_S = \pm 15$ V, $T_A = 25$ °C
		Supply voltage V_S V	Operating temperature T_A °C	Output current I_Q mA max	Input offset voltage ($R_G = 50\ \Omega$) V_{IO} mV min/max
Threshold Switches					
TCA 105	P-DIP-6	30	−25 to 85	50	
TCA 105 B	P-DIP-6	20	−25 to 85	50	
TCA 105 G	similar to P-DSO-6 (SMD)	30	−25 to 85	50	
TCA 345 A	P-DIP-4	10	−25 to 85	70	
TCA 965	P-DIP-14	4.75 to 27	−25 to 85	50	
Comparators with Darlington Input					
TCA 312 A	P-DIP-6	±2 to ±15	−55 to 125	70	±10
TCA 312 G	similar to P-DSO-6 (SMD)	±2 to ±15	−55 to 125	70	±10
TCA 315 A	P-DIP-6	±2 to ±15	−25 to 85	70	±15
TCA 315 G	similar to P-DSO-6 (SMD)	±2 to ±15	−25 to 85	70	±15
Comparators with TTL-compatible Output Voltage, High Output Current					
TCA 322 A	P-DIP-6	±2 to ±15	−55 to 125	70	±4
TCA 322 G	similar to P-DSO-6 (SMD)	±2 to ±15	−55 to 125	70	±4
TCA 325 A	P-DIP-6	±2 to ±15	−25 to 85	70	±5.5
TCA 325 G	similar to P-DSO-6 (SMD)	±2 to ±15	−25 to 85	70	±5.5
Current-Monitoring ICs					
TLE 4951	P-DIP-14	4.5 to 32	−40 to 125	40	
TLE 4951G	P-DSO-14	4.5 to 32	−40 to 125	40	

Bipolar IC

Type	Ordering Code	Package	Color Code
TCA 105	Q67000-A527	P-DIP-6	–
TCA 105 B	Q67000-A587	P-DIP-6	–
TCA 105 G	Q67000-A988	similar to P-DSO-6 (SMD)	orange/white

The TCA 105 contains an oscillator stage, a threshold switch, and two anti-valent output stages. The IC is especially suitable for application in proximity switches, light reflection switches, and other contactless switching applications.

Features

- Wide range of supply voltage, 4.5 to 30 V
- High output current, 50 mA
- TTL-compatible
- Triggerable with dc signal

Maximum Ratings

Description	Symbol	TCA 105; G	TCA 105 B	Unit
Supply voltage	V_S	30	20	V
Output voltage (pin 4, pin 5)	V_Q	30	20	V
Output current	I_Q	50	50	mA
Switching frequency	f_S	40	40	kHz
Input voltage	V_I	≥ 0[1])	≥ 0[1])	V
Junction temperature	T_j	125	125	°C
Storage temperature range	T_{stg}	−55 to 125	−55 to 125	°C
Thermal resistance (system – air)				
TCA 105, TCA 105 B	$R_{th\ SA}$	115	115	K/W
TCA 105 G	$R_{th\ SA}$	200		K/W

Operating Range

Supply voltage	V_S	4.75 to 30	4.75 to 20	V
Ambient temperature	T_A	−25 to 85	−25 to 85	°C
Oscillating frequency	f_{OSC}	1 to 4.5	1 to 4.5	MHz

[1]) Negative input voltages are not permitted

Characteristics

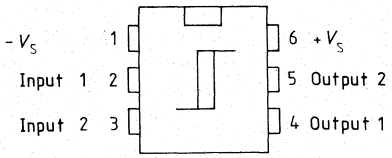
Static measurement, pins 3 and 1 interconnected
$V_S = 12$ V, $T_A = 25$ °C, $R_C = 5.6$ kΩ

Description	Symbol	min	typ	max	Unit
Supply current	I_S		3.4	5	mA
Input threshold voltage with compensation resistor R_C	V_I	300	400	480	mV
Input threshold current	I_I		−60		µA
Hysteresis	V_{hy}	20	35	50	mV
L output voltage $I_Q = 16$ mA	$V_{Q\,L}$		0.25	0.35	V
H output voltage	$V_{Q\,H}$		corresponds to V_S		
Reverse current, $V_S = 30$ V and/or 20 V	$I_{Q\,H}$			60	µA
L output voltage $I_Q = 50$ mA	$V_{Q\,L}$		0.7	1.15	V
Switching time in TTL operation $I_Q = 16$ mA	t		3		µs

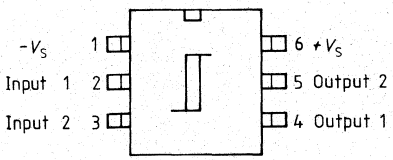
Pin Configurations

(top view)

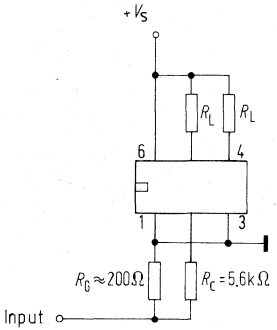
TCA 105, TCA 105 B



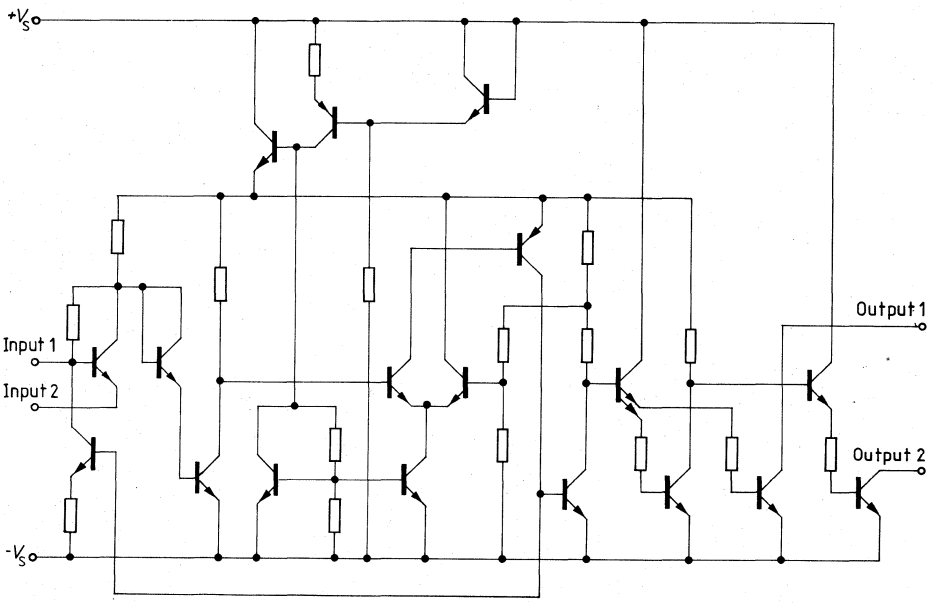
TCA 105 G



Test Circuit

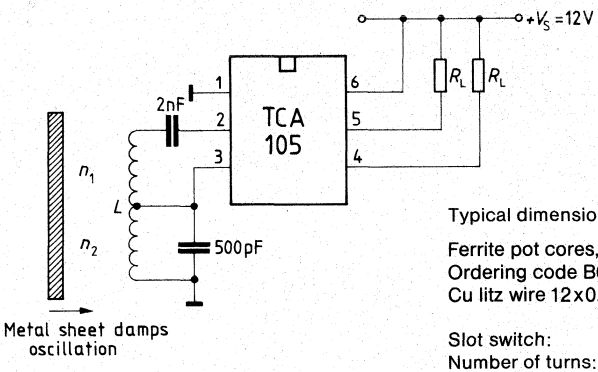


Circuit Diagram



Application Examples

Inductive Slot Switch or Proximity Switch



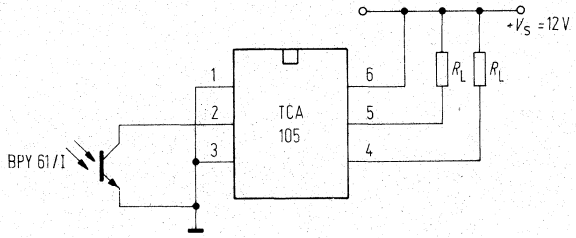
Typical dimensioning values:

Ferrite pot cores, 9 mm dia.
Ordering code B65935-A-X25
Cu litz wire 12x0.04 mm

Slot switch:
Number of turns: $n = 2 \times 25$
Distance between pot core halves:
2.5 to 3.5 mm

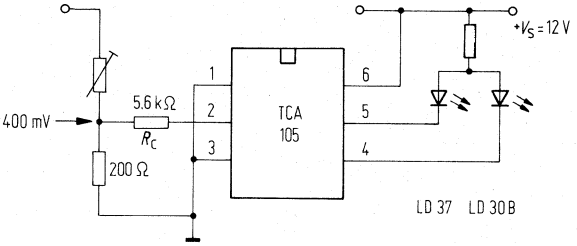
Proximity switch:
Number of turns: $n_1 = 8$, $n_2 = 40$
Distance: 2 to 3 mm

Light-Operated Switch (switching amplifier for phototransistor BPY 61)

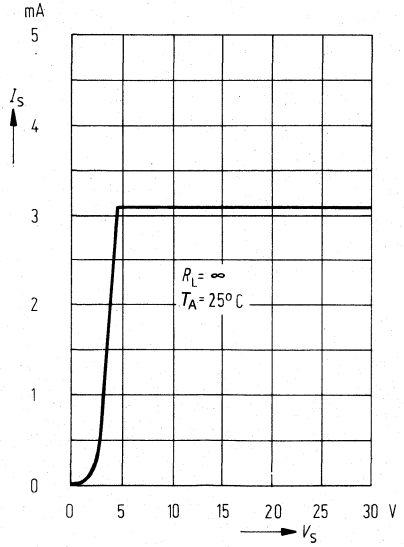


Application Example

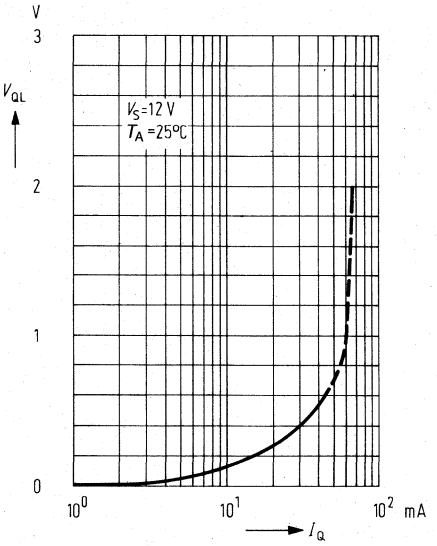
Voltage Monitor



Current consumption
Supply current versus
supply voltage
$T_A = 25\,°C$; $R_L = \infty$

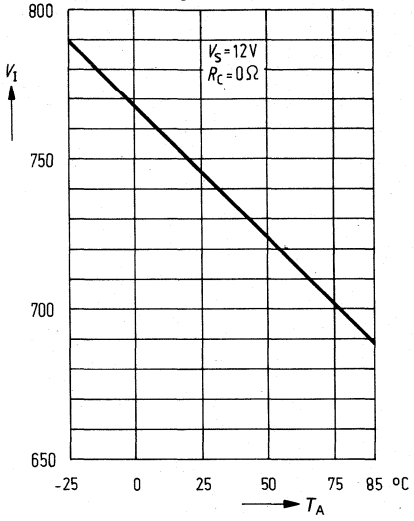


L output voltage versus
output current
$T_A = 25\,°C$; $V_S = 12$ V



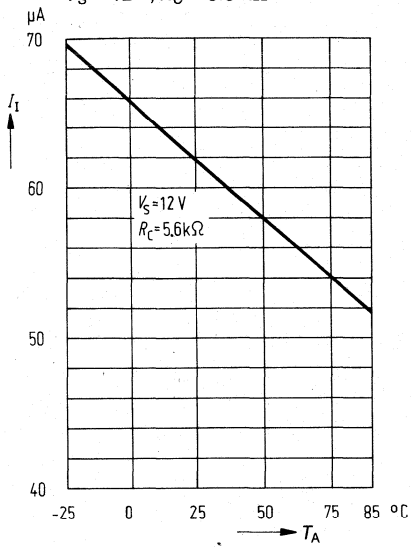
Switching threshold Input voltage versus ambient temperature

$V_S = 12$ V; $R_C = 0$

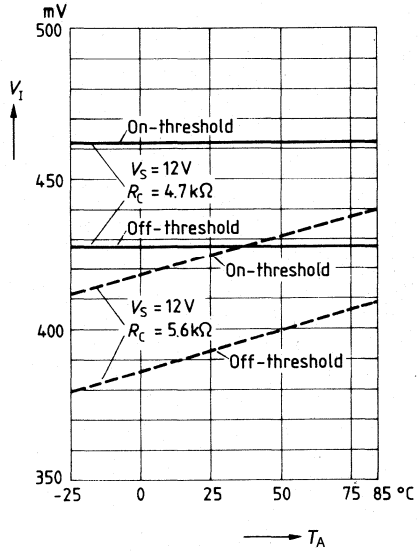


Input current versus ambient temperature

$V_S = 12$ V; $R_C = 5.6$ kΩ

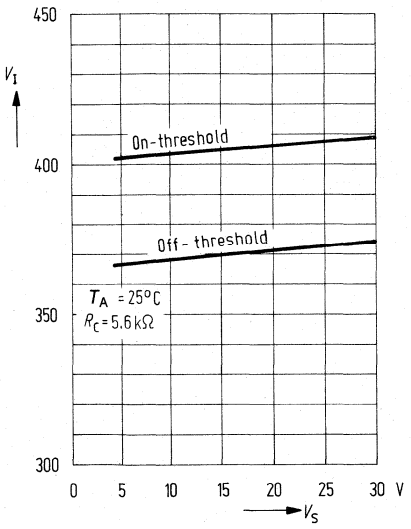


Switching threshold Input voltage versus ambient temperature



Switching threshold Input voltage versus supply voltage

$T_A = 25$ °C; $R_C = 5.6$ kΩ



Type	Ordering Code	Package	Color Code
S TCA 312 A	Q67000-A2048	P-DIP-6	–
TCA 312 G	Q67000-A2509	similar to P-DSO-6 (SMD)	red
S TCA 315 A	Q67000-A561	P-DIP-6	–
S TCA 315 G	Q67000-A1005	similar to P-DSO-6 (SMD)	red/yellow

TCA 312 and TCA 315 are suitable for use as Schmitt trigger or comparator in control engineering and automotive electronics. The output has been designed to control TTL circuits directly.

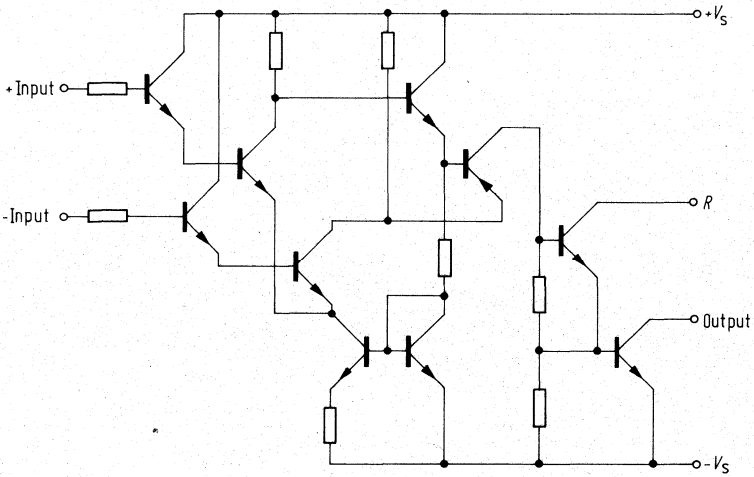
Features

- Very high input resistance
- Large control range
- High output current
- Low output saturation voltage
- Wide temperature range (TCA 312 A; G)
- NPN input
- Open collector output
- High slew rate

Applications

- Comparator
- Level converter
- Driver

Circuit Diagram



Type	Ordering Code	Package	Color Code
S TCA 322 A	Q67000-A2501	P-DIP-6	–
TCA 322 G	Q67000-A2508	similar to P-DSO-6 (SMD)	brown
S TCA 325 A	Q67000-A562	P-DIP-6	–
S TCA 325 G	Q67000-A1012	similar to P-DSO-6 (SMD)	green/yellow

TCA 322 and TCA 325 are suitable for use as Schmitt trigger or comparator in control engineering and automotive electronics. The output has been designed to control TTL circuits directly.

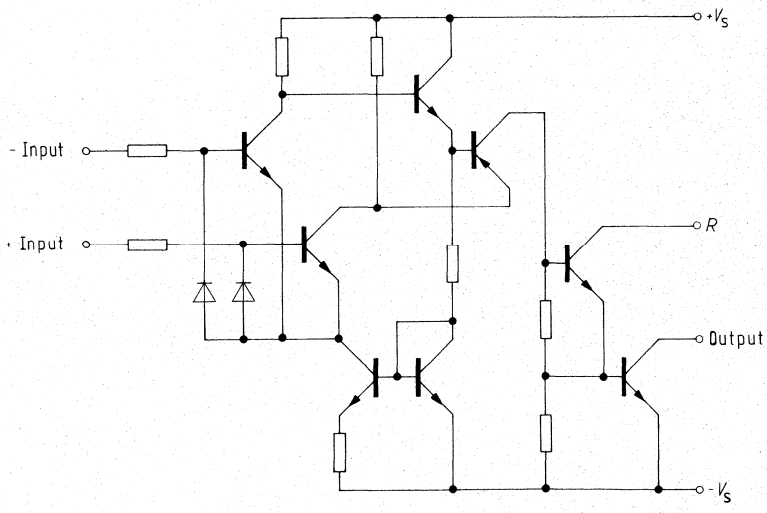
Features

- Wide common-mode range
- Large supply voltage range
- Large control range
- High output current
- Low output saturation voltage
- Wide temperature range (TCA 322 A; G)
- NPN input
- Open collector output
- High slew rate

Applications

- Comparator
- Level converter
- Impedance converter
- Driver

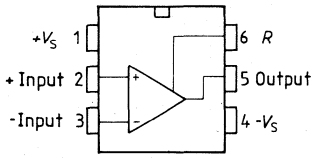
Circuit Diagram



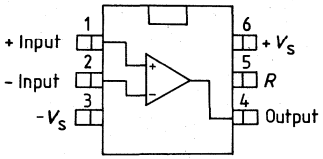
Pin Configurations

(top view)

TCA 312 A; TCA 322 A
TCA 315 A; TCA 325 A

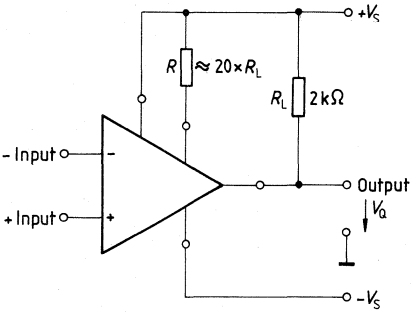


TCA 312 G; TCA 322 G
TCA 315 G; TCA 325 G



Connection Diagram

R_L = load resistance (collector resistance)



Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	±15	V
Output current Driver current	I_Q I_{dr}	70 10	mA mA
Differential input voltage V_S = 13 to 15 V Differential input voltage V_S = 2 to 13 V	V_{ID} V_{ID}	±13 $\pm V_S$	V V
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air TCA 312 A TCA 312 G	 $R_{th\ SA}$ $R_{th\ SA}$	 115 200	 K/W

Operating Range

Supply voltage	V_S	±2 to ±15	V
Ambient temperature	T_A	−55 to 125	°C

Characteristics

V_S = ±5 V to ±15 V; R = 6.8 kΩ
R_L = 2 kΩ,
unless otherwise specified

Description	Symbol	T_A = 25 °C min	typ	max	T_A = −55 to 125 °C min	max	Unit
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage R_G = 50 Ω	V_{IO}	−10		10	−15	15	mV
Input offset current Input current Input current V_{ID} = ±13 V	I_{IO} I_I I_I	−5	 5 	5 15 200	−10	10 25 	nA nA nA
Control range V_S = ±15 V R_L = 620 Ω, V_S = ±15 V V_S = ±15 V, f = 100 kHz	 $V_{Q\ pp}$ $V_{Q\ pp}$ $V_{Q\ pp}$	 14.9 14.9	 ±10	 −14.8 −14.0	 14.8 14.8	 −14.6 −13.5	 V V V

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R = 6.8$ kΩ,
$R_L = 2$ kΩ,
unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -55$ to 125 °C min	max	Unit
Input impedance $f = 1$ kHz	Z_i		3				MΩ
Open-loop voltage gain $f = 1$ kHz $R_L = 10$ kΩ, $f = 1$ kHz $f = 1$ MHz	 G_{V0} G_{V0} G_{V0}	 80	 83 88 60		 75		 dB dB dB
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	75	80		70		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	200		200	μV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		12 50	50			μV/K pA/K
Slew rate of V_q for non-inverting operation[1]) (see TAA 765, test circuit 1)	SR		30				V/μs
Output saturation voltage $I_Q = 10$ mA	V_{Qsat}			200		400	mV
Output reverse current	I_{QR}			1		5	μA

Characteristics

$V_S = \pm 2$ V; $R = 6.8$ kΩ, $R_L = 2$ kΩ

Input offset voltage $R_G = 50$ Ω	V_{IO}	−10		10	−15	15	mV
Input offset current Input current	I_{IO} I_I	−5	 5	5 15	−10	10 25	nA nA
Open-loop voltage gain $f = 1$ kHz	G_{V0}	75			70		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	±15	V
Output current	I_Q	70	mA
Driver current	I_{dr}	10	mA
Differential input voltage V_S = 13 to 15 V	V_{ID}	±13	V
Differential input voltage V_S = 2 to 13 V	V_{ID}	$\pm V_S$	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air TCA 315 A	$R_{th\ SA}$	115	K/W
TCA 315 G	$R_{th\ SA}$	200	K/W

Operating Range

Supply voltage	V_S	±2 to ±15	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

V_S = ±5 V to ±15 V
R = 6.8 kΩ, R_L = 2 kΩ,
unless otherwise specified

		T_A = 25 °C			T_A = −25 to 85 °C		
Description	Symbol	min	typ	max	min	max	Unit
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage R_G = 50 Ω	V_{IO}	−15		15	−18	18	mV
Input offset current	I_{IO}	−10		10	−20	20	nA
Input current	I_I		5	25		35	nA
Input current V_{ID} = ±13 V	I_I			200			nA
Control range							
V_S = ±15 V	$V_{Q\ pp}$	14.9		−14.8	14.8	−14.6	V
R_L = 620 Ω; V_S = ±15 V	$V_{Q\ pp}$	14.9		−14.0	14.8	−13.5	V
V_S = ±15 V, f = 100 kHz	$V_{Q\ pp}$		±10				V

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R = 6.8$ kΩ,
$R_L = 2$ kΩ,
unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -25$ to 85 °C min	max	Unit
Input impedance $f = 1$ kHz	Z_i		3				MΩ
Open-loop voltage gain $f = 1$ kHz $R_L = 10$ kΩ, $f = 1$ kHz $f = 1$ MHz	 G_{V0} G_{V0} G_{V0}	 75	 80 85 60		 75		 dB dB dB
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	70	78		70		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	200		200	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		12 50	50			µV/K pA/K
Slew rate of V_q for non-inverting operation[1]) (see TAA 765, test circuit 1)	SR		30				V/µs
Output saturation voltage $I_Q = 10$ mA	V_{Qsat}			200		400	mV
Output reverse current	I_{QR}			10		20	µA

Characteristics

$V_S = \pm 2$ V; $R = 6.8$ kΩ, $R_L = 2$ kΩ

Input offset voltage $R_G = 50$ Ω	V_{IO}	−17		17	−20	20	mV
Input offset current Input current	I_{IO} I_I	−10	 5	10 25	−20	20 35	nA nA
Open-loop voltage gain $f = 1$ kHz	G_{V0}	70			70		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	±15	V
Output current	I_Q	70	mA
Driver current at R	I_{dr}	10	mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air TCA 322 A	$R_{th\ SA}$	115	K/W
TCA 322 G	$R_{th\ SA}$	200	K/W

Operating Range

Supply voltage	V_S	±2 to ±15	V
Ambient temperature	T_A	−55 to 125	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V
$R = 6.8$ kΩ, $R_L = 2$ kΩ,
unless otherwise specified

		$T_A = 25$ °C			$T_A = -55$ to 125 °C		
Description	**Symbol**	**min**	**typ**	**max**	**min**	**max**	**Unit**
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage $R_G = 50$ Ω	V_{IO}	−4		4	−6	6	mV
Input offset current	I_{IO}	−100	±50	100	−300	300	nA
Input current	I_I		0.3	0.7		1.0	µA
Control range							
$V_S = \pm 15$ V	$V_{Q\ pp}$	14.9		−14.8	14.8	−14.6	V
$R_L = 620$ Ω, $V_S = \pm 15$ V	$V_{Q\ pp}$	14.9		−14.0	14.8	−13.5	V
$V_S = \pm 15$ V, $f = 100$ kHz	$V_{Q\ pp}$		±10				V

Characteristics
$V_S = \pm 5$ V to ± 15 V
$R = 6.8$ kΩ, $R_L = 2$ kΩ,
unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	$T_A = -55$ to 125 °C min	max	Unit
Input impedance $f = 1$ kHz	Z_i		200				kΩ
Open-loop voltage gain $f = 1$ kHz $R_L = 10$ kΩ, $f = 1$ kHz $f = 1$ MHz	 G_{V0} G_{V0} G_{V0}	 85	 87 92 60		 80		 dB dB dB
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	80	85		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	200		200	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		6 0.3	25 1.5			µV/K nA/K
Slew rate of V_q for non-inverting operation[1]) (see TAA 765, test circuit 1)	SR		50				V/µs
Output saturation voltage $I_Q = 10$ mA	$V_{Q\,sat}$			200		400	mV
Output reverse current	I_{QR}			1		5	µA

Characteristics
$V_S = \pm 2$ V; $R = 6.8$ kΩ, $R_L = 2$ kΩ,
unless otherwise specified

Input offset voltage $R_G = 50$ Ω	V_{IO}	−4		4	−6	6	mV
Input offset current Input current	I_{IO} I_I	−70	 0.2	70 0.5	−200	200 0.8	nA µA
Open-loop voltage gain $f = 1$ kHz	G_{V0}	80			75		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	±15	V
Output current Driver current at R	I_Q I_{dr}	70 10	mA mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Thermal resistance system – air TCA 325 A TCA 325 G	 $R_{th\ SA}$ $R_{th\ SA}$	 115 200	 K/W K/W

Operating Range

Supply voltage	V_S	±2 to ±15	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = \pm 5$ V to ± 15 V
$R = 6.8$ kΩ, $R_L = 2$ kΩ,
unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	$T_A = 25$ °C typ	$T_A = 25$ °C max	$T_A = -25$ to 85 °C min	$T_A = -25$ to 85 °C max	Unit
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage $R_G = 50$ Ω	V_{IO}	−5.5		5.5	−7	7	mV
Input offset current Input current	I_{IO} I_I	−200	±80 0.5	200 0.8	−300	300 1.0	nA µA
Control range $V_S = \pm 15$ V $R_L = 620$ Ω, $V_S = \pm 15$ V $V_S = \pm 15$ V, $f = 100$ kHz	 $V_{Q\ pp}$ $V_{Q\ pp}$ $V_{Q\ pp}$	 14.9 14.9	 ±10	 −14.8 −14.0	 14.8 14.8	 −14.6 −13.5	 V V V

Characteristics

$V_S = \pm 5$ V to ± 15 V; $R = 6.8$ kΩ, $R_L = 2$ kΩ,
unless otherwise specified

Description	Symbol	$T_A = 25$ °C min	typ	max	T_A −25 to 85 °C min	max	Unit
Input impedance $f = 1$ kHz	Z_I		200				kΩ
Open-loop voltage gain $f = 1$ kHz $R_L = 10$ kΩ, $f = 1$ kHz $f = 1$ MHz	 G_{V0} G_{V0} G_{V0}	 80	 85 90 60		 80		 dB dB dB
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	75	83		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	200		200	µV/V
Temperature coefficient of V_{IO} $R_G = 50$ Ω Temperature coefficient of I_{IO} $R_G = 50$ Ω	α_{VIO} α_{IIO}		6 0.3				µV/K nA/K
Slew rate of V_q for non-inverting operation[1]) (see TAA 765, test circuit 1)	SR		50				V/µs
Output saturation voltage $I_Q = 10$ mA	$V_{Q\,sat}$			200		400	mV
Output reverse current	I_{QR}			10		20	µA

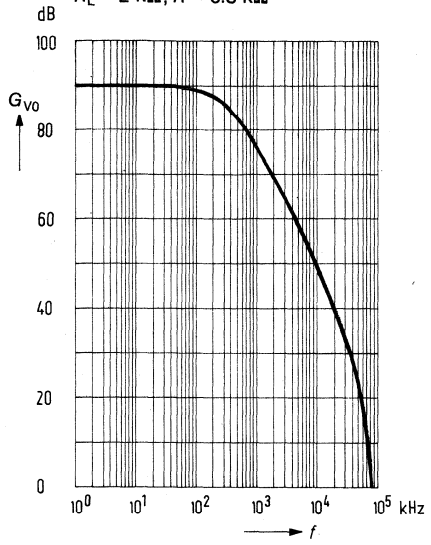
Characteristics

$V_S = \pm 2$ V; $R = 6.8$ kΩ, $R_L = 2$ kΩ

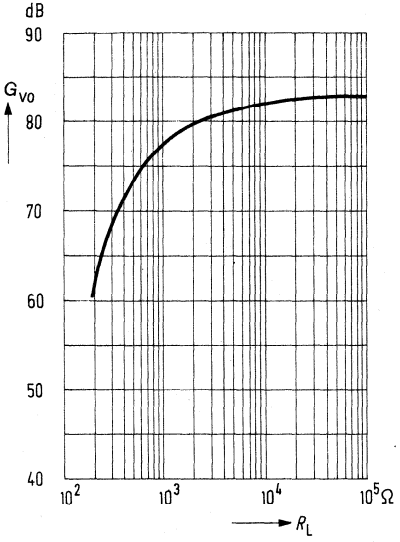
Input offset voltage $R_G = 50$ Ω	V_{IO}	−6		6	−7.5	7.5	mV
Input offset current Input current	I_{IO} I_I	−150	 0.2	150 0.6	−200	200 0.8	nA µA
Open-loop voltage gain $f = 1$ kHz	G_{V0}	75			75		dB

[1]) For the relationship between power bandwidth and slew rate refer to **"General information"**

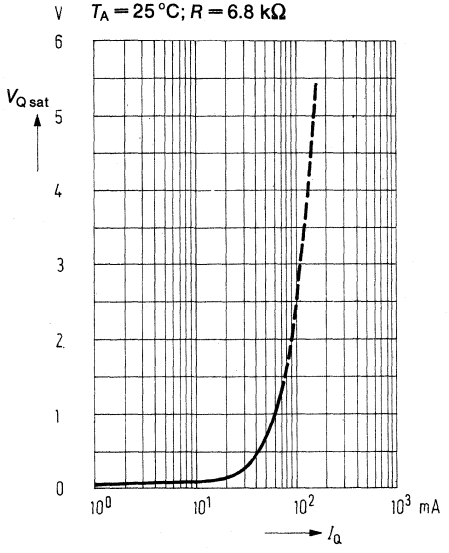
Open-loop voltage gain versus frequency
$R_L = 2\ k\Omega$; $R = 6.8\ k\Omega$



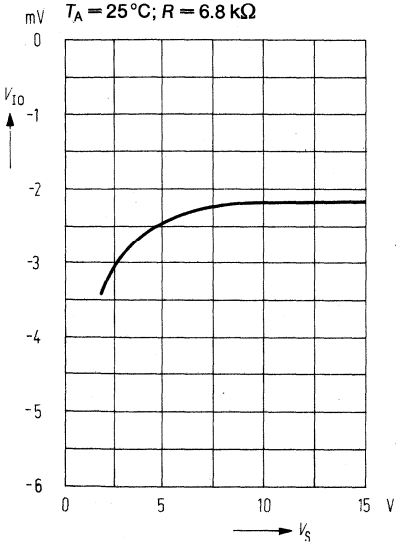
Open-loop voltage gain versus load resistance
$T_A = 25\,°C$; $R = 6.8\ k\Omega$



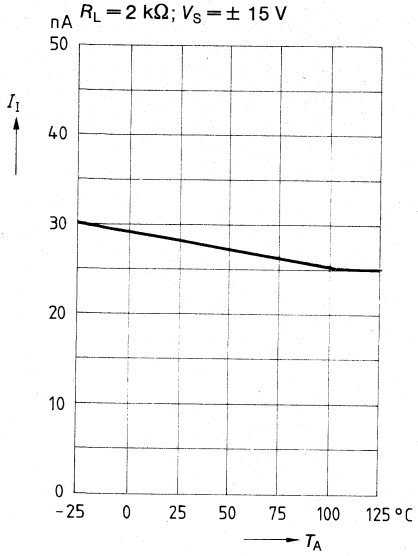
Output saturation voltage versus output current
$T_A = 25\,°C$; $R = 6.8\ k\Omega$



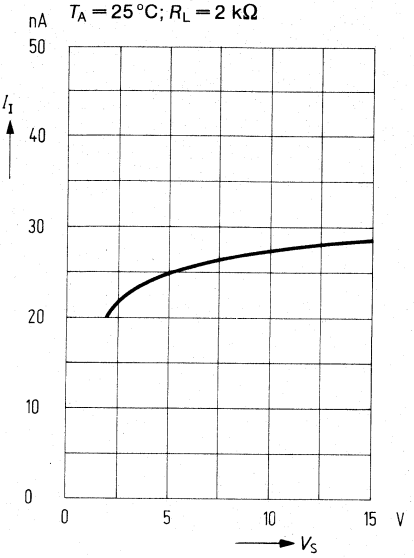
Input offset voltage versus supply voltage
$T_A = 25\,°C$; $R = 6.8\ k\Omega$



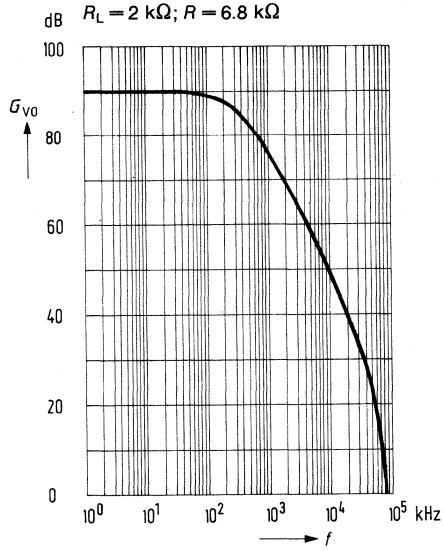
Input current versus ambient temperature
$R_L = 2\ k\Omega$; $V_S = \pm 15\ V$



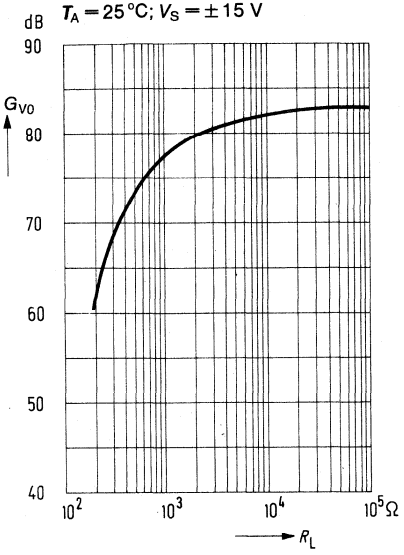
Input current versus supply voltage
$T_A = 25\,°C$; $R_L = 2\ k\Omega$



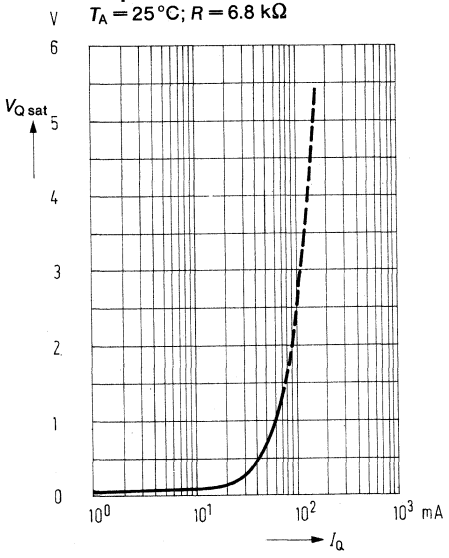
Open-loop voltage gain versus frequency
$R_L = 2\ k\Omega$; $R = 6.8\ k\Omega$



Open-loop voltage gain versus load resistance
$T_A = 25\,°C$; $V_S = \pm 15\ V$



Output saturation voltage versus output current
$T_A = 25\,°C$; $R = 6.8\ k\Omega$



Bipolar IC

Type	Ordering Code	Package
TCA 345 A	Q67000-A564	P-DIP-4

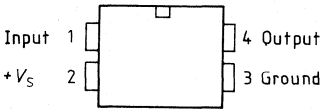
Threshold switches featuring linear, supply voltage-dependent threshold values. Inductive loads may be switched at the output without protective diode.

Features

- TTL-compatible
- High output current
- Very high input impedance
- Good stability due to hysteresis
- Few external components

Pin Configuration

(top view)



Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	10	V
Output current	I_Q	70	mA
Input voltage	V_I	0 to V_S	V
Inductance at the output	L_Q	500	mH
Junction temperature Storage temperature range	T_j T_{stg}	125 −55 to 125	°C °C
Thermal resistance system – air	$R_{th\ SA}$	140	K/W

Operating Range

Supply voltage	V_S	2 to 10	V
Ambient temperature	T_A	−25 to 85	°C

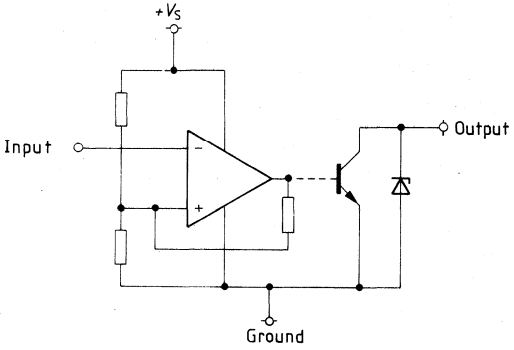
Characteristics

$T_A = +25\,°C$

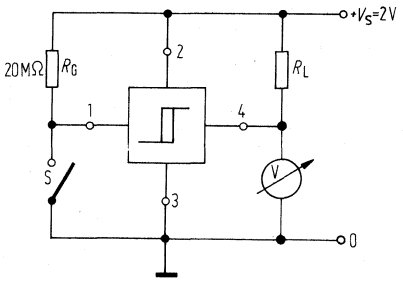
Description	Symbol	min	typ	max	Unit
Current consumption at output current					
I_Q = 0 mA; V_S = 2 V	$I_{S\,H}$		0.55	0.80	mA
= 5 V	$I_{S\,H}$		1.35	2.00	mA
I_Q = 40 mA; V_S = 2 V	$I_{S\,L}$		1.85	3.00	mA
= 5 V	$I_{S\,L}$		7.00	9.00	mA
L output voltage at I_Q = 40 mA V_S = 2 V	$V_{Q\,L}$		150	300	mV
Output reverse current V_Q = 10 V	$I_{Q\,H}$			30	µA
Switching threshold V_S = 2 to 10 V[1])	V_I	0.63 x V_S	0.66 x V_S	0.69 x V_S	V
Linearity error of the switching threshold (referred to V_S = 2 V)				3.0	%
Hysteresis (in % of V_S) V_S = 2 V	ΔV_I	6.0	10	15	%
Hysteresis (in % of V_S) V_S = 5 V	ΔV_I	6.0	20		%
Hysteresis (in % of V_S) V_S = 10 V	ΔV_I	6.0	20		%
Input current	I_I		10	30	nA
Z voltage via output	V	11.0	13.6	15.0	V
Temperature response of switching threshold			30		ppm/K

[1]) measured with increasing input voltage

Circuit Diagram

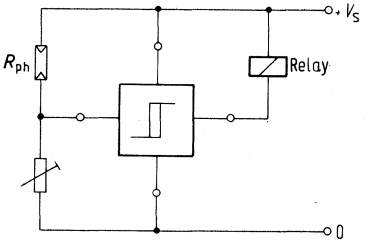


Test Circuit

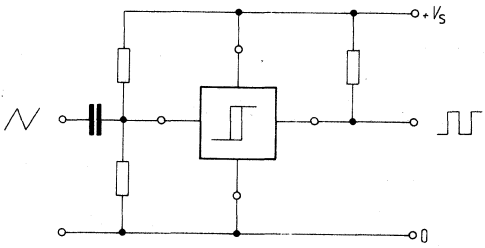


Application Circuits

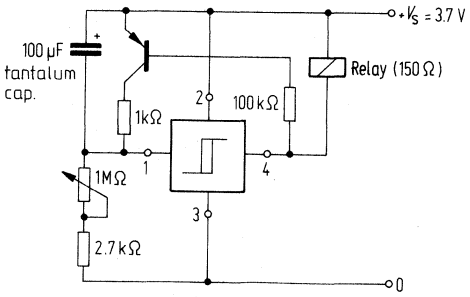
Twilight Switch
(switches on light at nightfall)



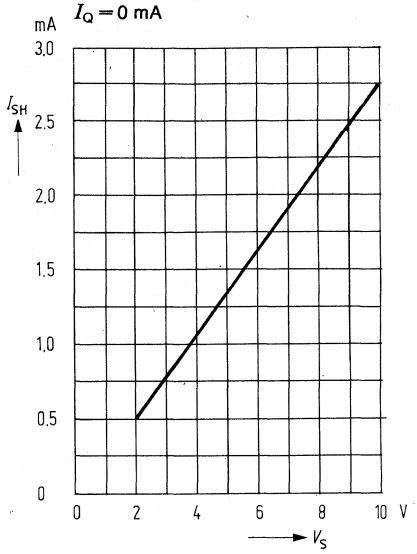
Triangle-square Converter



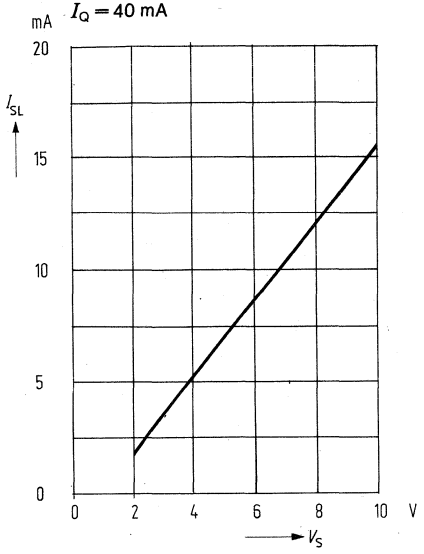
Clock Generator



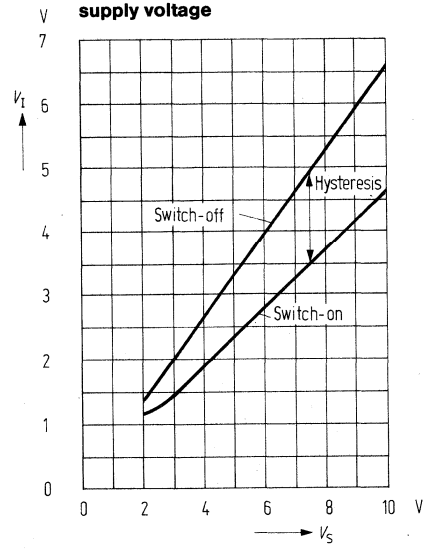
Current consumption I_{SH} versus supply voltage
$I_Q = 0$ mA



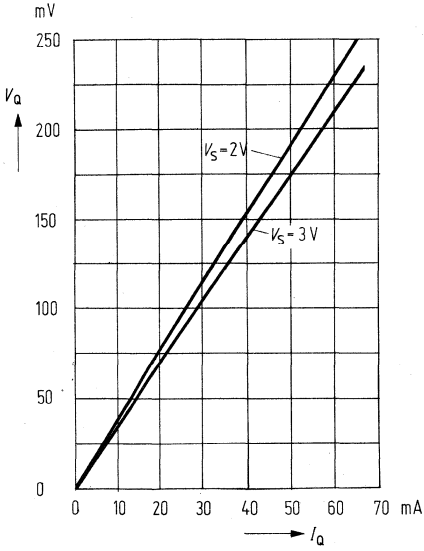
Current consumption I_{SL} versus supply voltage
$I_Q = 40$ mA



Switching threshold Input voltage versus supply voltage



Output voltage versus output current

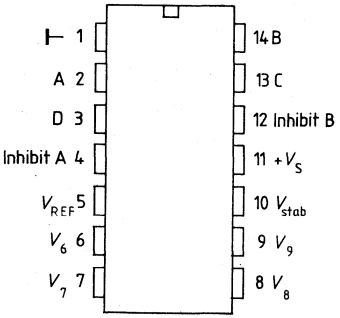


Bipolar IC

Type	Ordering Code	Package
TCA 965	Q67000-A982	P-DIP-14

The TCA 965 window discriminator is particularly suited for control systems as follow-up and adjusting control device with dead space. It can also be used in measuring systems for the selection of elements whose dc values should remain within tolerated deviations from required values. If used as Schmitt-trigger, switching frequencies are possible up to a typical frequency of 200 kHz.

Pin Configuration
(top view)



Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage, output voltages	V_S, V_Q	27	V
Input voltage difference between inputs 6, 7 and 8	V_I	15	V
Input voltage (pin 9)	V_I	30	V
Output current (pin 2, 3, 13, 14)	I_Q	50	mA
Output current of stabilized voltage (pin 10)	I_Q	10	mA
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air	$R_{th\ SA}$	80	K/W
	$R_{th\ SA}$	80	K/W

Operating Range

Supply voltage	V_S	4.75 to 27	V
Ambient temperature	T_A	−25 to 85	°C

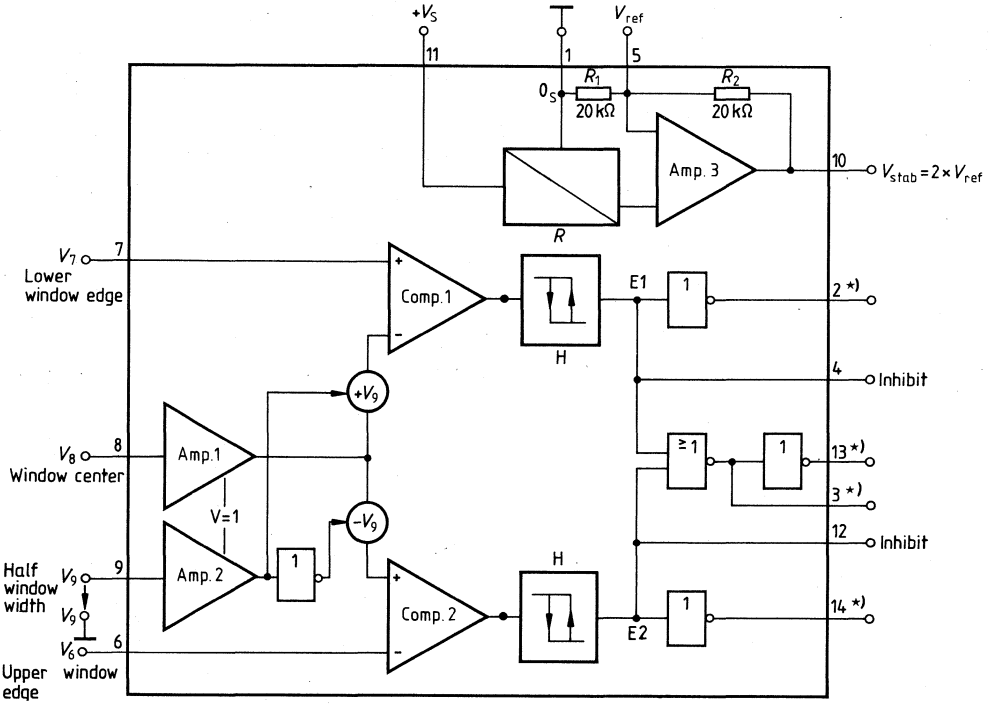
Characteristics

$V_S = 10$ V, $T_A = 25$ °C

Description	Symbol	Test conditions	min	typ	max	Unit
Current consumption	I_S	V_2, $V_{13} = V_{QH}$		5	7	mA
Input current (pin 6, 7, 8)	I_I			20	50	nA
Input current (pin 9)	$-I_I$			400	3000	nA
Input offset voltage (pin 6/8, pin 7/8)	V_{IO}		−20	±10	20	mV
Input voltage range (pin 6, 7, 8)	V_I	$\Delta V_I < 13$ V	1.5		$V_S - 1.0$	V
Input voltage range (pin 9)	V_I		50		$\frac{V_S}{2}$	mV
Differential input voltage	$V_6 - (V_8 - V_9)$				13	V
	$(V_8 + V_9) - V_7$				13	V
Reference voltage	V_5	$I_{REF} = 0$	2.8	3.0	3.2	V
Stabilized voltage	V_{10}	$V_S > 7.9$ V	5.5	6	6.5	V
Temperature coefficient of reference voltage	αV_5			0.5		mV/K
Sensitivity of reference voltage to supply voltage variations	$\frac{\Delta V_5}{\Delta V_S}$			3		mV/V
Output reverse current	I_{QH}				10	µA
Output saturation voltage	V_{QL}	$I_Q = 10$ mA			200	mV
		$I_Q = 40$ mA			800	mV
Hysteresis (window edges)	V_{hy}		18	22	35	mV
Inhibit threshold[1])	$V_{4,12}$			1.5		V
Inhibit current	$I_{4,12}$			−100		µA

[1]) Inhibition occurs if pin 4 and 12 are grounded.

Block Diagram

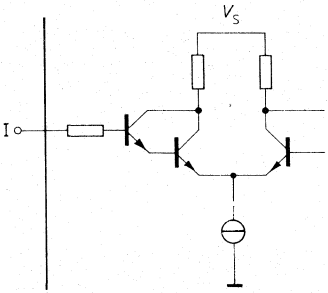


*) Open collector

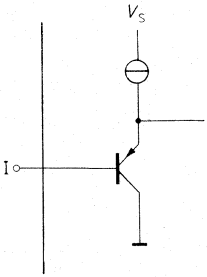
Schematic Circuit Diagrams

Inputs

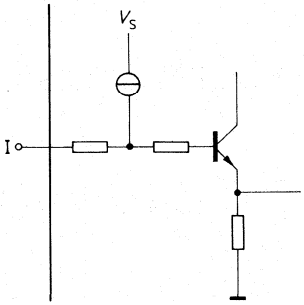
Pin 6, 7, 8



Pin 9

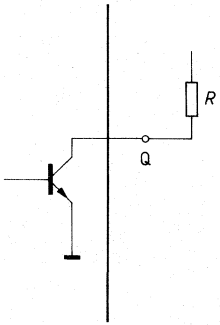


Pin 4, 12

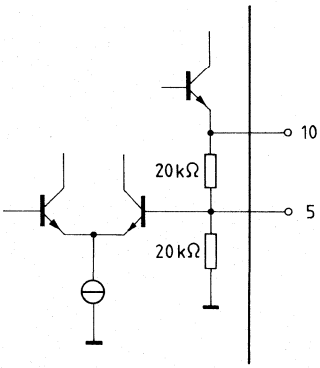


Outputs

Pin 2, 3, 13, 14



Pin 5, 10



Suggestions for Application

The window discriminator analyzes the input voltage with reference to two limits that are input as voltages. The window, within which the circuit reacts »well« can be input either by an upper (V_6) and a lower limit (V_7), or by the window center (V_8) and depending upon that, by a voltage ΔV, (V_9), which corresponds to half window width and is available to ground. A Schmitt trigger characteristic with a small hysteresis is effective at the switching points. Four output signals are available having the following meanings: input signal inside, outside the window (good, bad), too high, too low. All outputs have open collectors that can carry up to 50 mA for the control of small relays, lamps, LEDs. All the usual logic families can be driven directly requiring only few external components.

Additionally, the IC contains a reference voltage source with adjustable amplifier (V_{ref}) for the generation of various reference voltages (V_{stab}) for the inputs. The reference voltage source is, to a large extent, independent of temperature and supply voltage. For stabilization purposes, it requires a capacitor of up to 10 µF (electrolytic capacitor) to ground at pin 10.

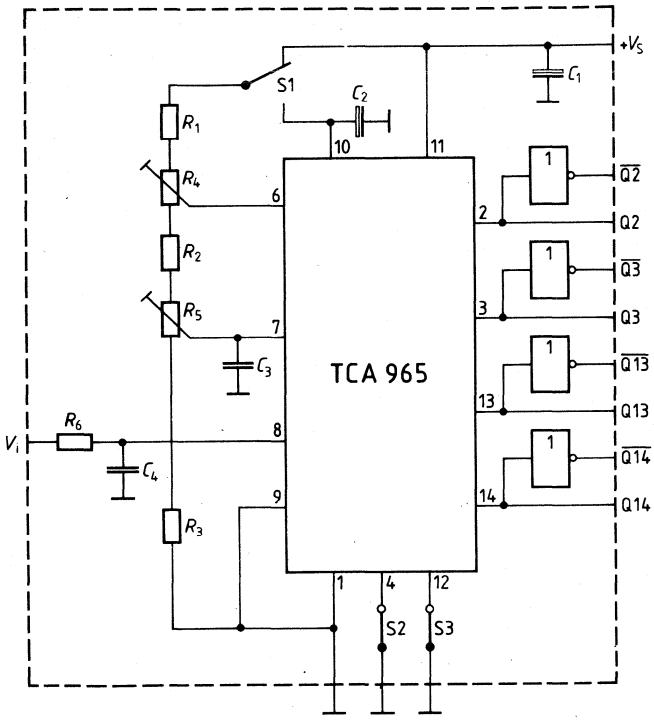
Truth Table (for block diagram in connection with application circuit I and II).

V_I	
Application circuit I $V_I = V_8$	Application circuit II $V_I = V_{6/7}$
$V_8 < (V_7 - V_9)$	$V_{6/7} > (V_8 + V_9)$
$V_8 > (V_6 + V_9)$	$V_{6/7} < (V_8 - V_9)$
$(V_6 + V_9) > V_8 > (V_7 - V_9)$	$(V_8 + V_9) > V_{6/7} > (V_8 - V_9)$
$V_6 + V_9$ – – – upper window edge $V_7 - V_9$ – – – lower window edge $(V_6 + V_9) - (V_7 - V_9)$ – – – – – window width	V_8 – – – window center V_9 – – – half window width (to ground)

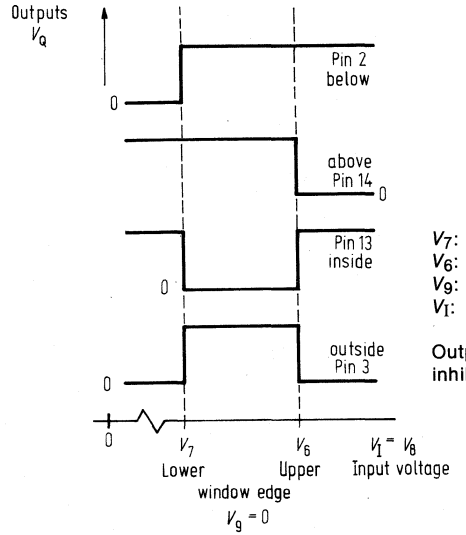
Outputs			
pin 2	14	13	3
L(H)	H(H)	H(L)	L(H)[1]
H(H)	L(H)	H(L)	L(H)[2]
H	H	L	H

Values in brackets refer to external inhibition via pin 4 and pin 12
[1] inhibition pin 4 to ground
[2] inhibition pin 12 to ground

Application Circuit I



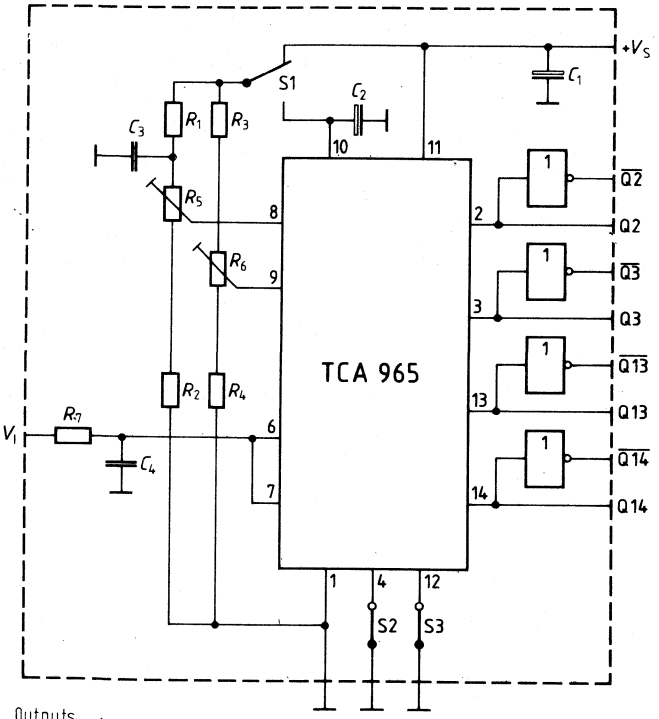
Outputs: pin 2 »below«
pin 3 »outside«
pin 13 »inside«
pin 14 »above«



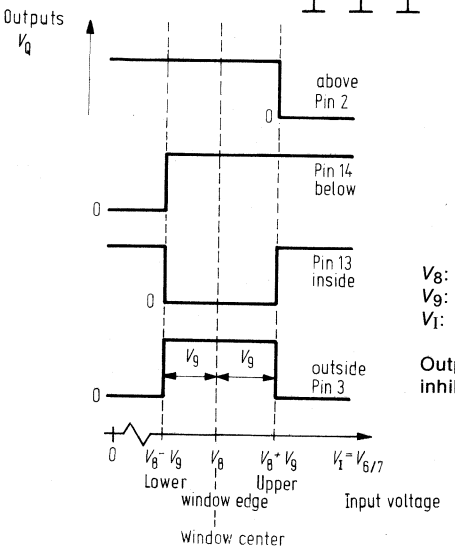
V_7: lower threshold
V_6: upper threshold
V_9: 0 V
V_I: at pin 8

Outputs pin 2 and pin 14 can be inhibited externally and are then H.

Application Circuit II



Outputs: pin 2 »above«
pin 3 »outside«
pin 13 »inside«
pin 14 »below«



V_8: window center
V_9: $\pm 1/2$ window width
V_I: pin 6 and pin 7 connected

Outputs pin 2 and pin 14 can be inhibited externally and are then H.

Examples of Circuit-Board Design for Application Circuits I and II

The inputs of the TCA 965 window discriminator have a Schmitt-trigger characteristic. With an input voltage that crosses the switching threshold very slowly there is nevertheless a risk of the output concerned going into oscillation before it clearly assumes the new switching state. The following circuit boards were designed specially to allow for this factor and offer a maximum possible safeguard against oscillations.

The causes of the undesired response are as follows:

1. **Feedback effect** of the switched load on the window-edge voltage through loading or unloading of the supply voltage.
2. **Hum voltages** that are superimposed on the input signal or the window-edge voltages derived from the supply voltage.
3. Unfavorable **routing of the tracks** on the circuit board with the voltage dividers for the window edges connected to a point of the grounding that alters in potential as a result of load variations. Pin 1 of the TCA 965 can take a load current of 2 x 50 mA to ground.

Remedies for 1

Boundary conditions for non-oscillating operation	
Application circuit I $V_6 = k \cdot V_S$, $V_7 = k' \cdot V_S$	Application circuit II $V_8 = k \cdot V_S$, $V_9 = k' \cdot V_S$
Condition $k \cdot \Delta V_S < V_{hy\,min}$ $k' \cdot \Delta V_S < V_{hy\,min}$	Condition $(k + k') \cdot \Delta V_S < V_{hy\,min}$

If these conditions are not fulfilled, no holding up of the window-edge voltages with capacitors will help. Instead one of the following three measures must be taken:

- use of V_{stab} for deriving the window-edge voltages,
- isolation of the supply voltage V'_S for the load from the supply voltage V_S of the TCA 965,
- increase of the edge hysteresis according to the technical note on the TCA 965.

Remedies for 2

Boundary condition

$V_{hum\ pp}/2 < V_{hy\ min}$

What decides fulfilment of the boundary condition is, depending on the particular application circuit, the sum of the hum voltages affecting the comparator concerned. The following interference suppression measures are suggested:

filtering of the input and window-edge voltage,

increase of the edge hysteresis.

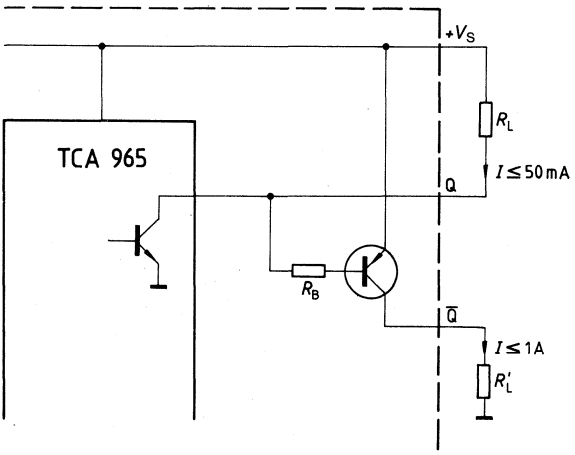
Remedies for 3

The circuit-board suggestions for the two application circuits have optimal grounding to the voltage dividers for the window edges with filtering of the supply voltage directly on the IC.

If several of the above-mentioned causes occur simultaneously, the remedies should be applied in the given sequence.

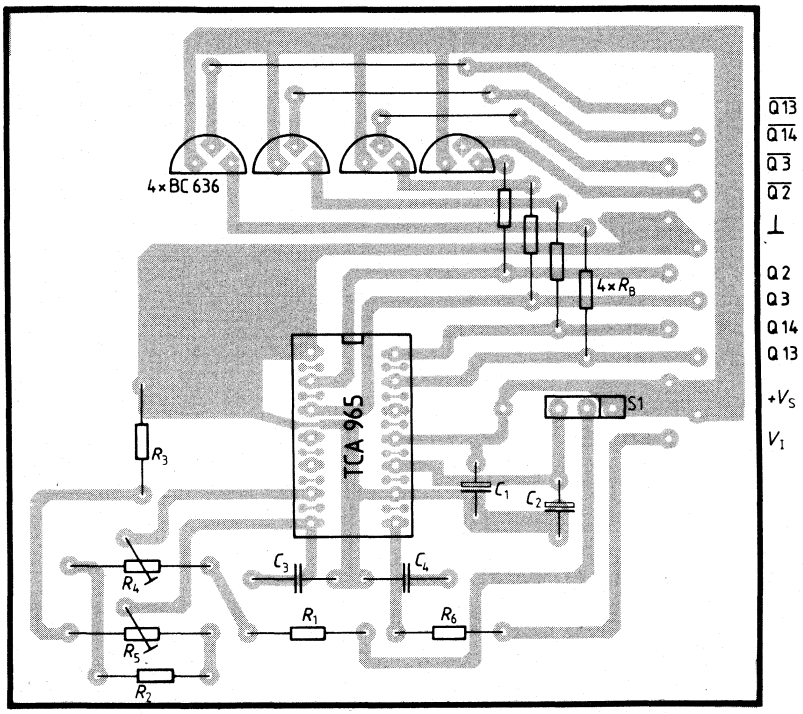
Output Wiring

There are additional driver stages at the outputs of the TCA 965 as shown in the following diagram for switching load currents up to 1 A (outputs $\overline{Q}$)



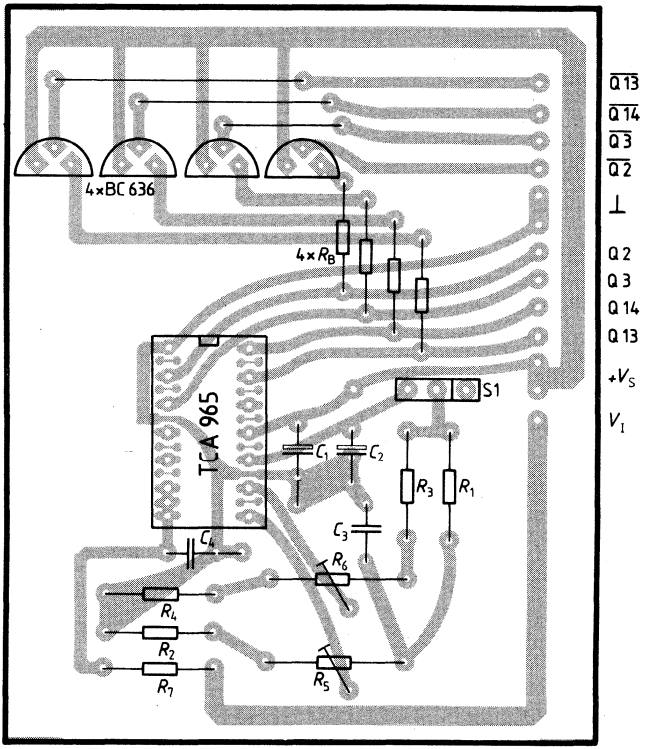
Circuit Board and Component Layout

Application circuit I
(without inhibit switch S2 and S3)



Circuit Board and Component Layout

Application circuit II
(without inhibit switch S2 and S3)



Preliminary Data **Bipolar IC**

Type	Ordering Code	Package
TLE 4951	Q67000-A8266	P-DIP-14
TLE 4951 G	Q67000-A8267	P-DSO-14 (SMD)

The TLE 4951 is designed to monitor the correct function of circuits, in particular those of light bulbs in cars. The IC comprises four identical comparator stages, the logic function of which corresponds to an exclusive-OR gate. With each comparator, pairs of lamps or single lamps can be monitored by means of the voltage drops across shunt resistors (R_{sh}) in the positive supply line (see **application circuits 1 and 2**).

Due to small differential input currents it is possible to connect protective resistors (R_s) in series. This provides a high degree of **protection against destruction** by interfering voltages occurring in cars.

Features

- Input currents max 25 µA, so that protective resistors can be connected in series
- Effective protection against destruction by excessive voltages such as load dump pulses occurring in cars
- Supply voltage range from 4.5 to 32 V
- Input voltage range up to 32 V, independent of supply voltage
- Switching threshold of comparators dependent on supply voltage, corresponding to the characteristic of light bulbs
- Temperature range between −40 °C and 125 °C

Applications

Current monitoring of

- light bulbs
- electric motors
- relays
- glow plugs
- circuits

especially suitable for:

- automotive electronics
- industrial plants

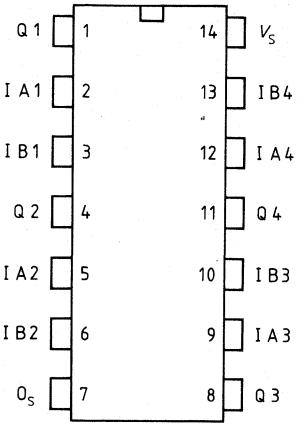
Functional Description

The component incorporates four identical comparator circuits. Each of these functional units has two equivalent inputs and one open-collector output Q. If the voltages differ by more than approx. 15 mV, the switching state changes from H (off-state) to L (on-state).

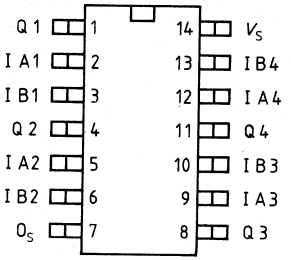
For an input voltage < 4.5 V at both the inputs, the output can switch to H independently of the differential input voltage. For an input voltage < 2.0 V the output is reliably off-state.

Pin Configurations
(top view)

TLE 4951



TLE 4951 G



Pin Description

Pin	Symbol	Function
1	Q1	Output 1
2 3	IA1 IB1	Input A1 Input B1
4	Q2	Output 2
5 6	IA2 IB2	Input A2 Input B2
7 8	0_S Q3	GND Output 3
9 10	IA3 IB3	Input A3 Input B3
11	Q4	Output 4
12 13	IA4 IB4	Input A4 Input B4
14	V_S	Supply voltage

Maximum Ratings

Description	Symbol	min	max	Unit	Notes
Supply voltage	V_S	−0.5	32	V	
Input voltages	$V_{A,B}$	−45	45	V	
Output voltage	V_Q	−0.5	32	V	
Output current	I_Q		40	mA	
Current through protecting structures					
at the supply terminal	I_S	−600	600	mA	$t_d < 2$ ms
at the outputs Q	I_{SQ}	−400	400	mA	$t_d < 2$ ms
Thermal resistance					
system – air TLE 4951	$R_{th\,SA}$		75	K/W	
TLE 4951G	$R_{th\,SA}$		125	K/W[1])	

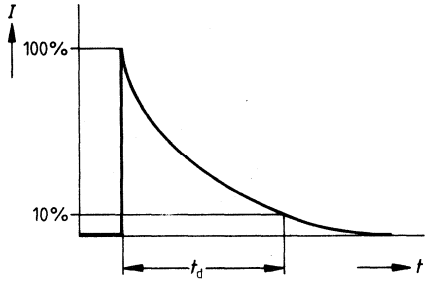
Operating range

Description	Symbol	min	max	Unit
Supply voltage	V_S	4.5	32	V
Ambient temperature	T_A	−40	125	°C
Common-mode input voltage range independent of V_S	V_{IC}	4.5	32	V
Differential input voltage	V_{ID}		100	mV

Permissible short-term overvoltages with series resistors R_S:

$+V_{A,B}$; V_S, Q = $I_{SA,B}$; V_S, Q · $R_{SA,B}$, V_S, Q + 32 V

$-V_{A,B}$; V_S, Q = $-I_{SA,B}$; V_S, Q · $R_{SA,B}$, V_S, Q



[1]) 75 K/W ceramic substrate

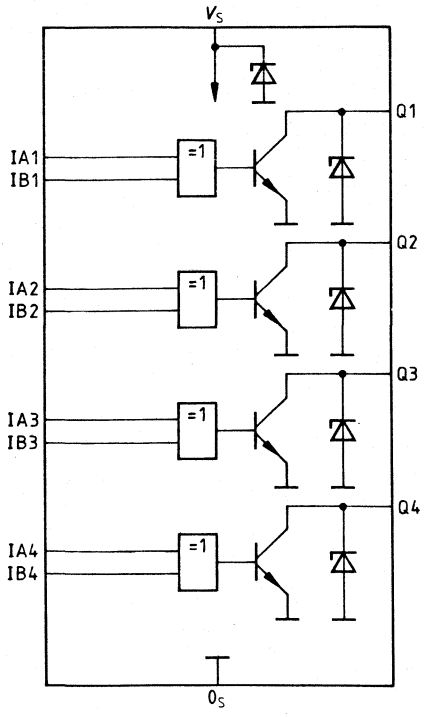
Characteristics

$T_A = -30\,°C$ to $+110\,°C$; $V_S = 10$ to 16 V

Description	Symbol	Measuring conditions	Test circuit	min	typ	max	Unit
Current consumption	I_S	Q1=Q2=Q3=Q4=H	1			3	mA
		Q1=Q2=Q3=Q4=L				8	mA
Switching threshold							
with $R_{SA,B}$	V_{Diff}[1])	$V_S = 13.5$ V, $R_S = 1$ kΩ	2	7	14	20	mV
without $R_{SA,B}$	V_{Diff}[1])	$V_S = 13.5$ V	1	4	8	12	mV
with $R_{SA,B}$	V_{Diff}	4.5 V < V_S < 5.5 V, $R_S = 1$ kΩ	2	2		14	mA
without $R_{SA,B}$	V_{Diff}	4.5 V < V_S < 5.5 V	1	1.5		8	mV
Input current	$I_{A,B}$	$V_A = V_B$	1			25	µA
Output saturation voltage	V_{QL}	$I_Q = 30$ mA	1			0.4	V
Output reverse current	I_{QH}	$V_{QH} = 32$ V	1			10	µA

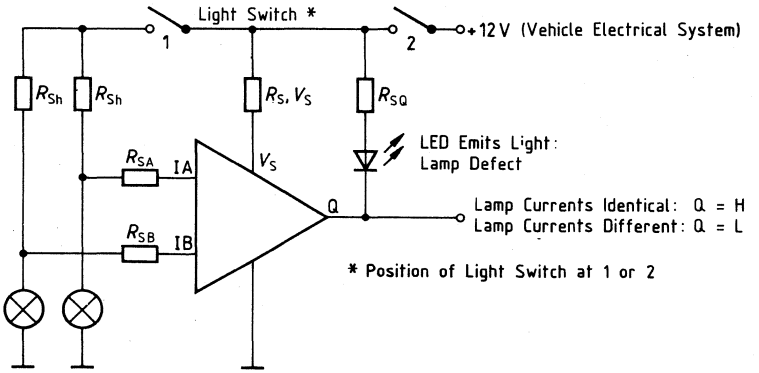
[1]) $V_{Diff} = |V_A - V_B|$

Block Diagram

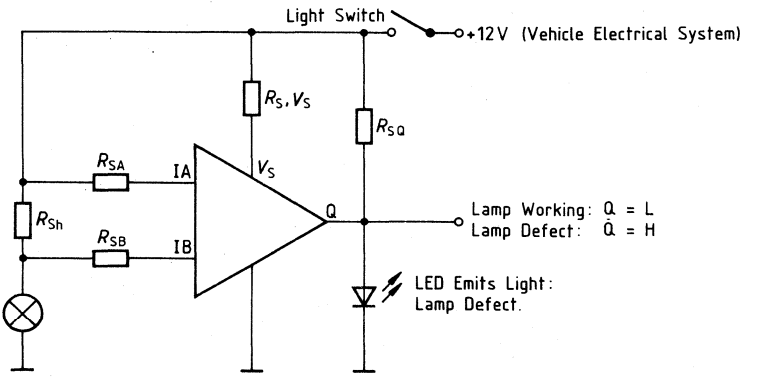


Application Circuits

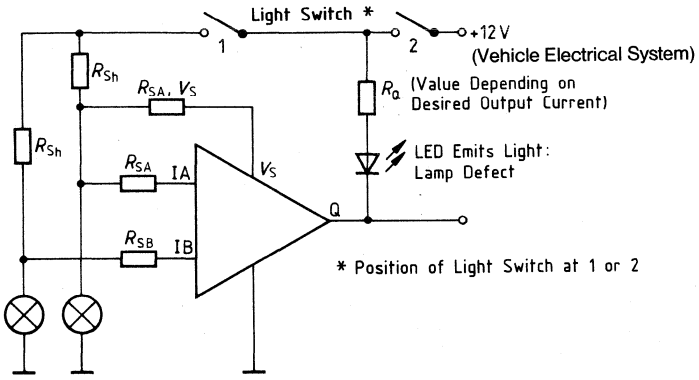
1. Differential measurement



2. Absolute-value measurement

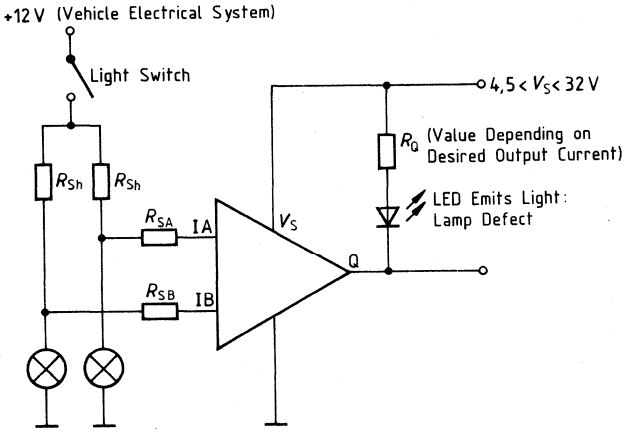


3. Supply from shunt resistor (function as "1": Differential measurement)



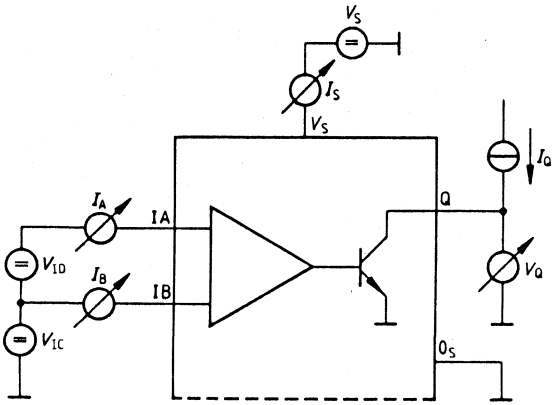
Recommended Protective Resistors: $R_{SA,B} = 1\,k\Omega$
$R_{SA}, V_S = 100\,\Omega$

4. Voltage supply separated from vehicle electrical system (function as "1": Differential measurement)

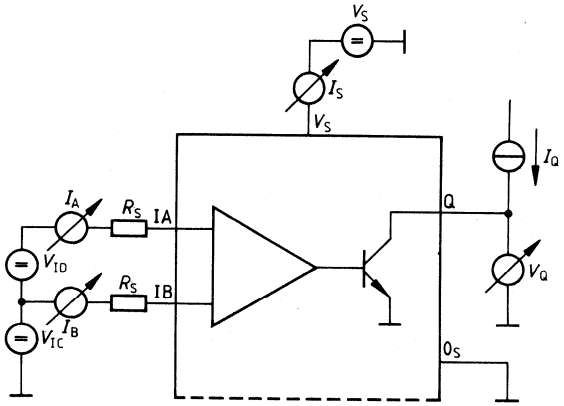


Recommended Protective Resistors : $R_{SA,B} = 1\,k\Omega$

Measuring Circuit 1

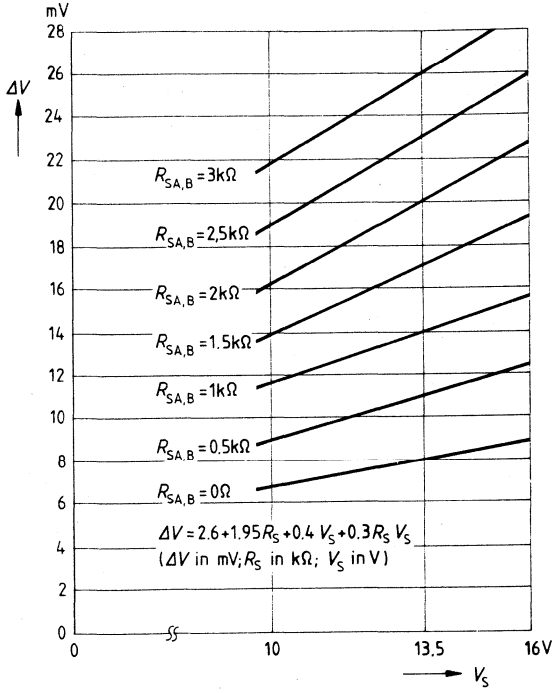


Measuring Circuit 2



Differential switching voltage versus supply voltage

Parameters: protective resistors at the inputs $R_{SA,B}$



ICs for Switch-Mode Power Supplies, Control ICs

Selector Guide

Type	Package	Operating range (V)	Temperature range (°C)	Output voltage (V)	Max. frequency (kHz)	Undervoltage shut-down	Reset signal	Closed-circuit current consumption (mA)	Driver outputs	Max. output current (mA)	Standby	Current limitation
PWM Control ICs												
TDA 4700	C-DIP-24	11 to 30	–25 to 85		100	●		12	2	70		●
TDA 4700 A	C-DIP-24	10.5 to 30	0 to 70		100	●		12	2	70		●
TDA 4718	C-DIP-18	11 to 30	–25 to 85		100	●		12	2	70		●
TDA 4718 A	P-DIP-18	10.5 to 30	0 to 70		100	●		12	2	70		●
TDA 4716 A	P-DIP-16	10.5 to 30	0 to 70		100	●		12	2	70		
TDA 4716 B	P-DIP-16	11 to 30	–25 to 85		100	●		12	2	70		●
TDA 4714 A	P-DIP-14	10.5 to 30	0 to 70		100	●		12	2	70	●	
TDA 4714 B	P-DIP-14	11 to 30	–25 to 85		100	●		12	1	70	●	●
TDA 4814 A	P-DIP-14	9.6 to 14	–25 to 85			●		5	1	$^{+400}_{-300}$	●	●
TDA 4918 A	P-DIP-20	10 to 30	–40 to 85		300	●		12	2	$^{+700}_{-500}$	●	●
TDA 4918 G	P-DSO-20	10 to 30	–40 to 85		300	●		12	2	$^{+700}_{-500}$	●	●
TDA 4919 A	P-DIP-20	10 to 30	–40 to 85		300	●		12	1	$^{+700}_{-500}$	●	●
TDA 4919 G	P-DSO-20	10 to 30	–40 to 85		300	●		12	1	$^{+700}_{-500}$	●	●
Low-Drop Fixed-Voltage Control ICs												
TLE 4258	P-T66-7	6 to 24	–40 to 150	5			●	2	1	750	●	●
TLE 4260	P-T66-5	6 to 28	–40 to 150	5			●	500µA	1	500	●	●

SMD = Surface Mounted Device

Control ICs for Single-Ended and Push-Pull Switch-Mode Power Supplies (SMPS)

The TDA 47xx family of control ICs for SMPS consists of four basic types that, in line with the particular application, will enable optimal adaptation to the SMPS concept that is called for. These devices include all the important basic functions that are expected of a modern SMPS, such as feed-forward control, soft start, dynamic current limitation, error comparators, reference-voltage source, undervoltage shut-down and push-pull open-collector outputs.

The 4714 A; B is the most economic version. TDA 4700 A is the version with the widest range of functions.

Control IC for Single-Ended and Push-Pull Switch-Mode Power Supplies (SMPS)

TDA 4700

Bipolar IC

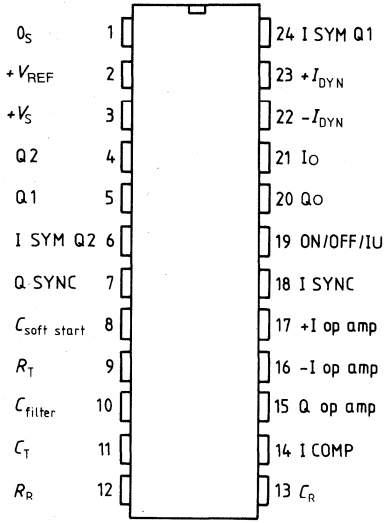
Type	Ordering Code	Package
TDA 4700	Q67000–Y595	C-DIP-24
S TDA 4700 A	Q67000–Y594	P-DIP-24

This versatile SMPS control IC comprises digital and analog functions which are required to design high-quality flyback, single-ended and push-pull converters in normal, half-bridge and full-bridge configurations. The component can also be used in single-ended voltage multipliers and speed-controlled motors. Malfunctions in electrical operation are recognized by the integrated operational amplifiers, which activate protective functions.

In addition to the noticeable reduction in components, our SMPS ICs offer a variety of advantages:

- Feed-forward control (line hum suppression)
- Symmetry inputs for push-pull converter
- Dynamic output current limitation
- Overvoltage protection
- Undervoltage protection
- Soft start
- Double pulse suppression

Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	0_S	Ground 0 V
2	$+V_{REF}$	Reference voltage
3	$+V_S$	Supply voltage
4	Q2	Output Q2
5	Q1	Output Q1
6	I SYM Q2	Symmetry Q2
7	Q SYNC	Sync. output
8	$C_{soft\ start}$	Soft start
9	R_T	VCO R_T
10	C_{filter}	Capacitance
11	C_T	VCO C_T
12	R_R	Ramp generator R_R
13	C_R	Ramp generator C_R
14	I COMP	Comparator input
15	Q op amp	Operational amplifier output
16	$-I_{op\ amp}$	Operational amplifier input (–)
17	$+I_{op\ amp}$	Operational amplifier input (+)
18	I SYNC	Sync. input
19	ON/OFF/IU	ON/OFF, undervoltage
20	QO	Overvoltage output
21	IO	Overvoltage input
22	$-I_{DYN}$	Dynamic current limitation (–)
23	$+I_{DYN}$	Dynamic current limitation (+)
24	I SYM Q1	Symmetry

Circuit Description

Voltage Controlled Oscillator (VCO)

The VCO generates a sawtooth voltage. The duration of the falling edge is determined by the value of C_T. The duration of the rising edge of the waveform and, therefore, approximately the frequency, is determined by the value of R_T. By varying the voltage at C_{filter}, the oscillator frequency can be changed by its rated value. During the fall time, the VCO provides a trigger signal for the ramp generator, as well as an L signal for a number of IC parts to be controlled.

Ramp Generator

The ramp generator is triggered by the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator waveform is to be shorter than the fall time of the VCO. To control the pulse width at the output, the voltage of the rising edge of the ramp generator signal is compared with a dc voltage at comparator K 2. The slope of the rising edge of the ramp generator signal is controlled by the current through R_R. This offers the possibility of an additional, superimposed control of the output duty cycle. This additional control capability, called »feed-forward control«, is utilized to compensate for known interference such as ripple on the input voltage.

Phase Comparator

If the component is operated without external synchronization, the sync input must be connected to the sync output for the phase comparator to set the rated voltage at C_{filter}. The VCO then oscillates with rated frequency. In the case of external synchronization, other components can be synchronized with the sync output. The component can be frequency-synchronized, but not phase-synchronized, with the sync input. The duty cycle of the square-wave voltage at the sync input is arbitrary. The best stability as to small phase and frequency interference deviation is achieved with a duty cycle as offered by the sync output.

Push-pull Flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K 2

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge exceeds the lower of the two plus levels, both outputs are disabled via the pulse turn-off flipflop. The period during which the respective, active output is low can be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Operational Amplifier K1

The K1 op amp is a high-quality amplifier. Fluctuations in the output voltage of the power supply are amplified by K1 and applied to the free + input of comparator K2. Variations in output voltage are, in this way, converted to a corresponding change in output duty cycle. K1 has a common-mode input voltage range between 0 V and +5 V.

Pulse-Turn-Off Flipflop

The pulse turn-off flipflop enables the outputs at the start of each half cycle. If an error signal from comparator K7 or a turn-off signal from K2 is present, the outputs will immediately be switched off.

Comparator K3

Comparator K3 limits the voltage at capacitance $C_{\text{soft start}}$ (and also at K2) to a maximum of +5 V. The voltage at the ramp generator output may, however, rise to 5.5 V. With a corresponding slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value.

Comparator K4

The comparator has its switching threshold at 1.5 V and sets the error flipflop with its output if the voltage at capacitance $C_{\text{soft start}}$ is below 1.5 V. However, the error flipflop accepts the set signal only if no reset pulse (error) is applied. In this way the outputs cannot be turned on again as long as an error signal is present.

Soft Start

The lower one of the two voltages at the plus inputs of K2 is a measure for the duty cycle at the output. At the instant of turning on the component, the voltage at capacitor $C_{\text{soft start}}$ equals 0 V. As long as no error is present, this capacitor is charged with a current of 6 µA to the maximum value of 5 V. In case of an error, $C_{\text{soft start}}$ is discharged with a current of 2 µA. A set signal is pending at the error flipflop below a charge of 1.5 V and the outputs are enabled if no reset signal is pending simultaneously. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually increased slowly and continuously not before the voltage at $C_{\text{soft start}}$ exceeds 1.8 V.

Error Flipflop

Error signals which are routed to input $\overline{R}$ of the error flipflop cause an immediate disabling of the outputs, and after the error has been eliminated, cause the component to switch on again by the soft start.

Comparator K5, K6, K8, V_{REF} Overcurrent Load

These are error detectors which cause immediate disabling of the outputs via the error flipflop when an error occurs. After elimination of the error, the component switches on again using the soft start. The output of K5 can be fed back to the input. This causes the IC output stage to remain disabled even after elimination of the overvoltage. However, it requires high-ohmic overvoltage coupling.

Comparator K 7

K 7 serves to recognize overcurrents. This is the reason why both inputs of the op amp have been brought out. Turning on is resumed after error recovery at the beginning of the next half period but without using the soft start.

The K 7 common-mode range covers 0 V to +4 V. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

Symmetry

In push-pull converters, a saturation of the transformer core must be prevented. The degree of saturation of the transformer can be determined with an external circuit, thus the active periods of the outputs can be decreased unsymmetrically at the symmetry inputs.

Outputs

Both outputs are transistors with open collectors and operate in a push-pull arrangement. They are active low. The time in which only one of the two outputs is conductive can be varied infinitely. The length of the falling edge at VCO is equal to the minimum time during which both outputs are disabled simultaneously. The minimum L voltage is 0.7 V.

Reference Voltage

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be utilized in the external wiring of the op amp, the error comparators, the ramp generator, or other external components.

Maximum Ratings

Description	Symbol	Conditions	min	max	Unit
Supply voltage	V_S		−0.3	33	V
Voltage at Q1, Q2	V_Q	Q1, Q2 high	−0.3	33	V
Current at Q1, Q2	I_Q	Q1, Q2 low		70	mA
Symmetry 1, 2	V_{SYM}		−0.3	33	V
Sync output	$V_{SYNC\ Q}$	SYNC Q high	−0.3	7	V
	$I_{SYNC\ Q}$	SYNC Q low	0	10	mA
Sync input	$V_{SYNC\ I}$		−0.3	33	V
Input C_{filter}	$V_{I\ Cf}$		−0.3	7	V
Input R_T	$V_{I\ RT}$		−0.3	7	V
Input C_T	$V_{I\ CT}$		−0.3	7	V
Input R_R	$V_{I\ RR}$		−0.3	7	V
Input C_R	$I_{I\ CR}$		−10	10	mA
Input comparator K2, K5, K6, K7	$V_{I\ K}$		−0.3	33	V
Output K5	$V_{Q\ K5}$		−0.3	33	V
Input op amp	$V_{I\ Op\ Amp}$		−0.3	33	V
Output op amp	$V_{Q\ Op\ Amp}$		−0.3	V_S-1	V
				max. 7	V
Reference voltage	V_{REF}		−0.3	V_{REF}	V
Input $C_{soft\ start}$	$V_{I\ soft\ start}$		−0.3	7	V
Junction temperature	T_j			125	°C
Storage temperature	T_{stg}		−55	125	°C
Thermal resistance system – air TDA 4700	$R_{th\ SA}$			65	K/W
TDA 4700 A	$R_{th\ SA}$			65	K/W

Operating Range

Supply voltage	V_S		10.5	30	V
Ambient temperature					
TDA 4700	T_A		−25	85	°C
TDA 4700 A	T_A		0	70	°C
VCO frequency	f		40	250 000	Hz
Ramp generator frequency	f_{RG}		40	250 000	Hz

Characteristics

$V_S = 11$ V to 30 V; $T_A = -25$ °C to +85 °C

Description	Symbol	Test conditions	min	typ	max	Unit
Supply current	I_S	$C_T = 1$ nF, $f_{VCO} = 100$ kHz	8		20	mA
Reference						
Reference voltage	V_{REF}	0 mA < I_{REF} < 5 mA	2.35	2.5	2.65	V
Reference voltage change	ΔV_{REF}	14 V ± 20%		8		mV
Reference voltage change	ΔV_{REF}	25 V ± 20%		15		mV
Reference voltage change	ΔV_{REF}	0 mA < I_{REF} < 5 mA			15[1]	mV
Temperature coefficient	TC			0.25	0.4	mV/K
Response threshold of I_{REF} overcurrent	I_{REF}			10		mA
Oscillator (VCO)						
Frequency range	f_{VCO}		40		100 000	Hz
Frequency change	$\Delta f/f_{VCO}$	14 V ± 20%		0.5		%
Frequency change	$\Delta f/f_{VCO}$	25 V ± 20%	−1		1	%
Tolerance	$\Delta f/f_{VCO}$	$\Delta R_T = 0$, $\Delta C_T = 0$	−7		7	%
Fall time sawtooth	t	$C_T =$ 1 nF		1		µs
	t	$C_T = 10$ nF		10		µs
RC combination	C_T		0.82		47	nF
VCO	R_T		5		700	kΩ
Ramp Generator						
Frequency range	f		40		100 000	Hz
Maximum voltage at C_R	V_H			5.5		V
Minimum voltage at C_R	V_L			1.8		V
Input current through R_R	I_{RR}		0		400	µA
Current transformation ratio	I_{RR}/I_{CR}			1/4		
Synchronization						
Sync output	$V_{Q\,H}$	$I_{Q\,H} = -200$ µA	4			V
	$V_{Q\,L}$	$I_{Q\,L} = 1.6$ mA			0.4	V
Sync input	$V_{I\,H}$		2			V
	$V_{I\,L}$				0.8	V
Input current	$-I_I$				5	µA
Comparator K2						
Input current	$-I_{I\,K2}$				2	µA
Turn-off delay[2]	$t_{D\,OFF}$				500	ns
Input voltage	$V_{I\,K2}$	for duty cycle				
		$D = 0$		1.8		V
		$D =$ max.		5		V
Common-mode input voltage range	$V_{I\,C}$		0		5.5	V

[1] At $T_A = 0$ °C to 70 °C, this value falls to max. 5 mV.
[2] At the input: step function $\Delta V = -100$ mV ⇀↽ $\Delta V = +100$ mV

Characteristics

$V_S = 11$ V to 30 V; $T_A = -25\,°C$ to $+85\,°C$

Description	Symbol	Test conditions	min	typ	max	Unit
Soft Start K3, K4						
Charge current for $C_{soft\ start}$	I_{ch}			6		µA
Discharge current for $C_{soft\ start}$	I_{dch}			2		µA
Upper limiting voltage	V_{lim}			5		V
Switching voltage K4	V_{K4}			1.5		V
Operational Amplifier						
Open-loop voltage gain	G_{V0}		60	80		dB
Input offset voltage	V_{IO}		−10		10	mV
Temperature coefficient of V_{IO}	TC		−30		30	µV/K
Input current	$-I_I$				2	µA
Common-mode input voltage range	V_{IC}		0		5	V
Output current	I_Q		−3		1.5	mA
Rise time of output voltage	$\Delta V/\Delta t$			1		V/µs
Transition frequency	f_T			3		MHz
Phase at f_T	φ_T			120		deg.
Output voltage	$V_{Q\,H/L}$	$-3\ mA < I < 1.5\ mA$	1.5		5.5	V
Symmetry						
Input voltage	$V_{I\,H}$		2.0			V
	$V_{I\,L}$				0.8	V
Input current	$-I_I$				2	µA
Output Stages Q1, Q2						
Output voltage	$V_{Q\,H}$				30	V
	$V_{Q\,L}$	$I_Q = 20$ mA			1.1	V
Output leakage current	I_Q	$V_{Q\,H} = 30$ V			2	µA
ON, OFF, Undervoltage K6						
Switching voltage	V		V_{REF}−30mV		V_{REF}+30mV	V
Input current	$-I_I$				2	µA
Turn-off delay time[1])	$t_{D\,OFF}$			250		ns
Error detection time[1])	t			50		ns

[1]) At the input: step function $V_{REF} = -100$ mV ⌐→ $V_{REF} = +100$ mV

Characteristics

V_S = 11 to 30 V; T_A = −25 °C to +85 °C

Description	Symbol	Test conditions	min	typ	max	Unit
Dynamic Current Limitation K7						
Common-mode input voltage range	V_{IC}		0		4	V
Input offset voltage	V_{IO}		−10		10	mV
Input current	$-I_I$				2	µA
Turn-off delay time[2])	$t_{D\ OFF}$			250		ns
Error detection time[2])	t			50		ns
Overvoltage K5						
Switching voltage	V		V_{REF}-30mV		V_{REF}+30mV	V
Input current	$-I_I$				2	µA
Output current	$-I_Q$	V_{QHmin} = 5 V	0		200	µA
Turn-off delay time[1])	$t_{D\ OFF}$			250		ns
Error detection time[1])	t			50		ns
Supply Undervoltage						
Turn-on threshold for V_S rising	V_S	0 °C < T_A < 70 °C	8.8		11	V
					10.5	V
Turn-off threshold for V_S falling	V_S	0 °C < T_A < 70 °C	8.5		10.5	V
					10	V
Input C_{filter}						
Rated voltage for rated frequency	V_R			4		V
Frequency approx. proportional to voltage within the range	V_R		3		5	V
Voltage at open sync input	$V_{c\ filter}$			1.6		V

[1]) At the input: step function V_{REF} = −100 mV → V_{REF} = +100 mV
[2]) At the input: step function ΔV = −100 mV → ΔV = +100 mV

Dimensioning Notes for RC Network

1. Determination of the minimum time during which both outputs must be disabled
   → selection of C_T; selection of $C_R \leq C_T$

2. Determination of the VCO frequency = 2 x output frequency
   → selection of R_T.

3. Determination of the rated slope of the rising ramp generator voltage, which the maximum possible turn-on period per half wave depends on
   → selection of R_R.

4. Duration of the soft start process
   → selection of $C_{soft\ start}$.

5. In the case of a free-running VCO: connect sync output with sync input.

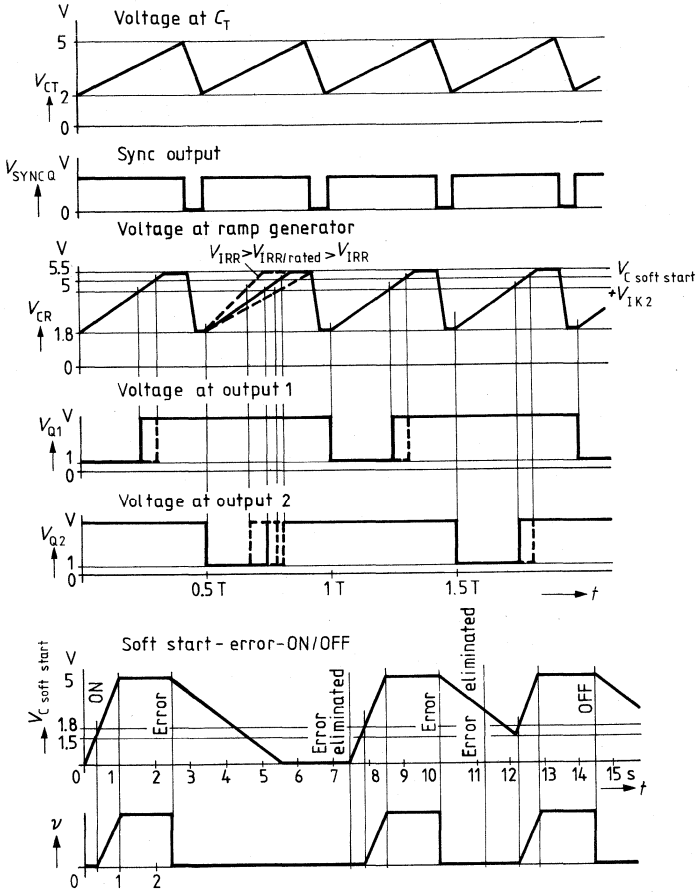
6. Wiring of the op amp according to the dynamic requirements and connection of its output with the free input of K2.

7. Capacitance C_{filter} is not required in the free-running operation (sync input connected with sync output).

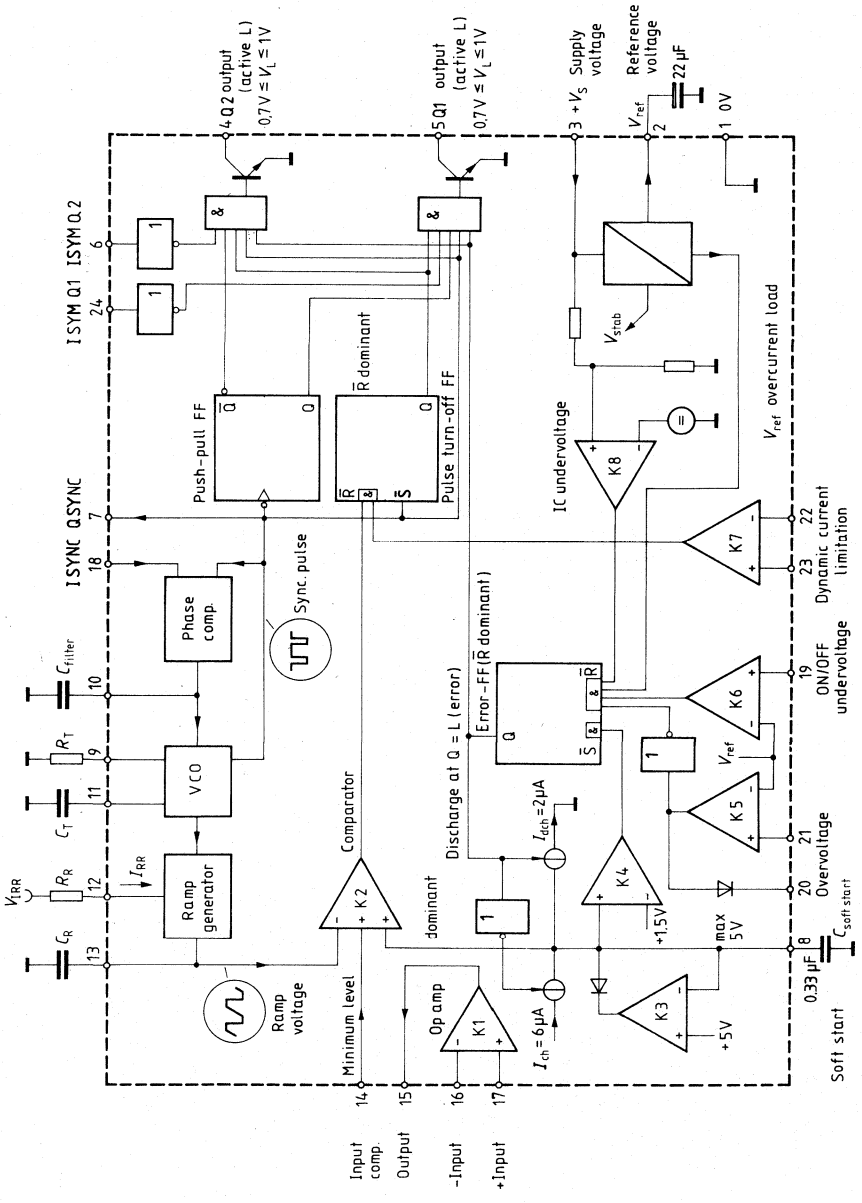
   In the case of external synchronization, that value depends on the selected operating frequency and the required maximum phase interference deviation.

Rated VCO frequency:	100 kHz	50 Hz
C_{filter} favorable:	10 nF	1 µF

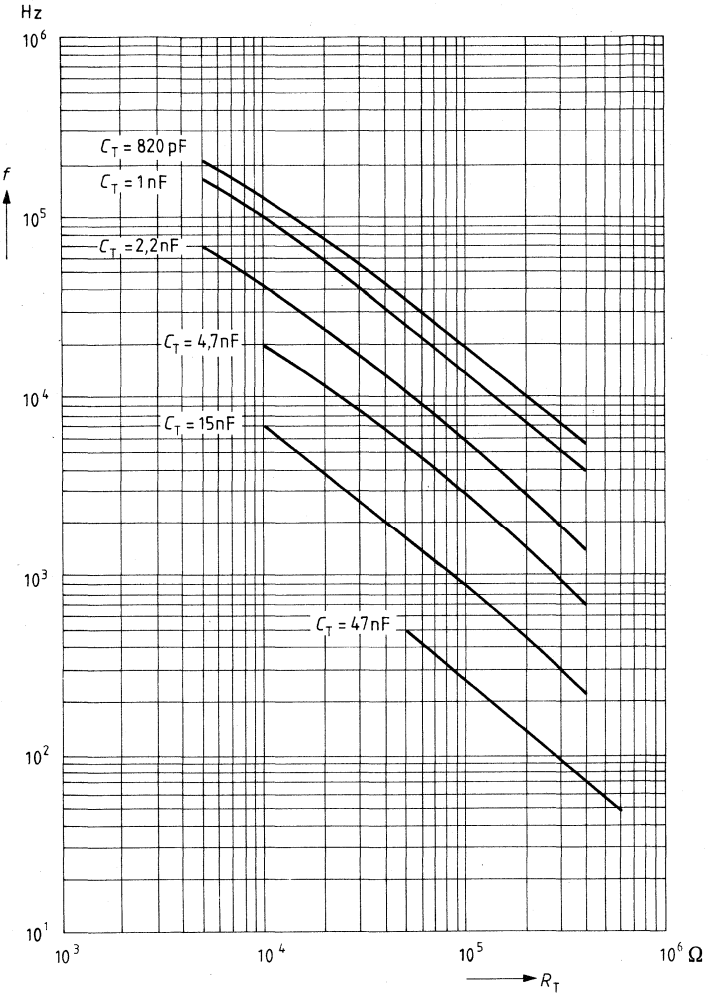
Pulse Diagram



Block Diagram

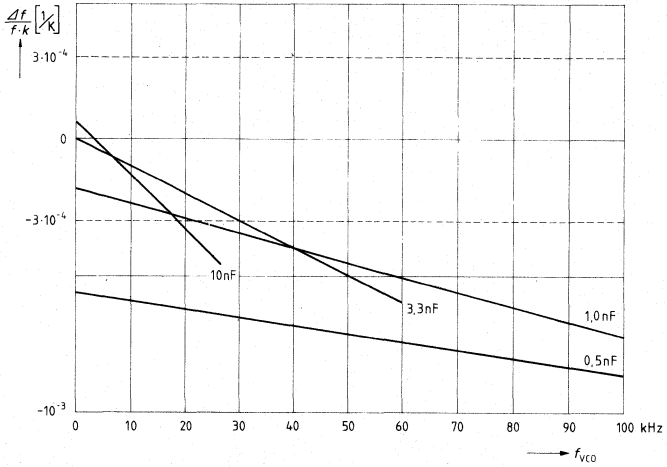


VCO frequency versus R_T and C_T.

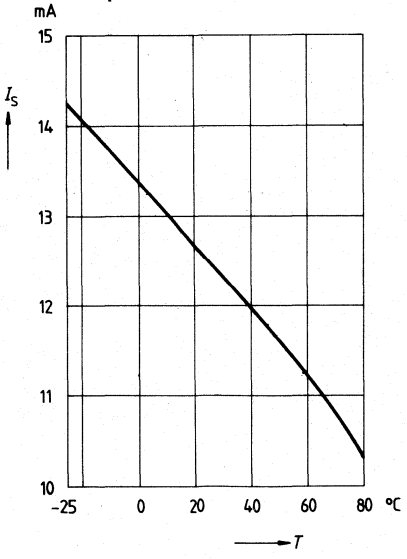


VCO temperature response
$V_S = 12$ V; D = max.

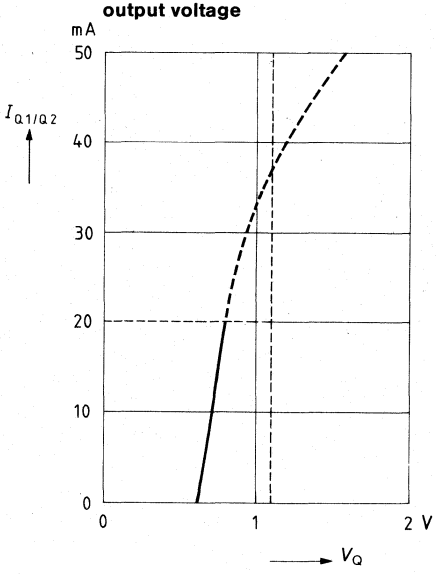
$\frac{\Delta f_{VCO}}{f_K \cdot K}\left[\frac{1}{K}\right]$ with C_T as parameter



Current consumption versus temperature



Output current versus output voltage



Control IC for Single-Ended and Push-Pull Switch-Mode Power Supplies (SMPS)

TDA 4718

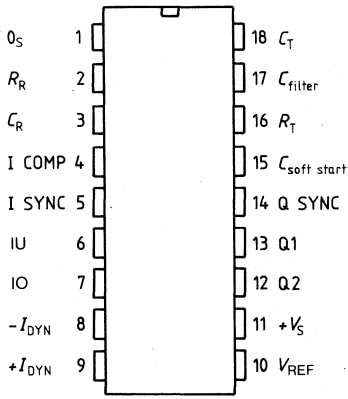
Bipolar IC

Type	Ordering Code	Package
TDA 4718	Q67000-Y638	C-DIP-18
TDA 4718 A	Q67000-Y639	P-DIP-18

This 18-pin SMPS control IC comprises digital and analog functions which are required to design high-quality flyback, single-ended, and push-pull converters in normal and half-bridge configurations. In addition to the control functions, the circuit contains operational amplifiers which detect malfunctions during electrical operation and activate suitable protective measures. A PLL circuit for synchronization is one of the special advantages offered by this IC in addition to the following features:

- Feed-forward control (line hum suppression)
- Push-pull outputs
- Dynamic current limitation
- Overvoltage protection
- Undervoltage protection
- Soft start
- Double pulse suppression

Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	0_S	Ground 0 V
2	R_R	Ramp generator R_R
3	C_R	Ramp generator C_R
4	I COMP	+ input comparator K2
5	I SYNC	Sync input
6	I U	Input undervoltage, ON/OFF
7	I O	Input overvoltage
8	$-I_{DYN}$	Input dynamic current limitation (–)
9	$+I_{DYN}$	Input dynamic current limitation (+)
10	V_{REF}	Reference voltage
11	$\pm V_S$	Supply voltage
12	Q2	Output Q2
13	Q1	Output Q1
14	Q SYNC	Sync output
15	$C_{soft\ start}$	Soft start
16	R_T	VCO R_T
17	C_{filter}	Capacitance
18	C_T	VCO C_T

Circuit Description

Voltage Controlled Oscillator (VCO)

The VCO generates a sawtooth voltage. The duration of the falling edge is determined by the value of C_T. The duration of the rising edge of the waveform and, therefore, approximately the frequency, is determined by the value of R_T. By varying the voltage at C_{filter}, the oscillator frequency can be changed by its rated value. During the fall time, the VCO provides a trigger signal for the ramp generator, as well as an L signal for a number of IC parts to be controlled.

Ramp Generator

The ramp generator is triggered by the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator waveform is to be shorter than the fall time of the VCO. To control the pulse width at the output, the voltage of the rising edge of the ramp generator signal is compared with a dc voltage comparator K2. The slope of the rising edge of the ramp generator signal is controlled by the current through R_R. This offers the possibility of an additional, superimposed control of the output duty cycle. This additional control capability, called »feed-forward control«, is utilized to compensate for known interference such as ripple on the input voltage.

Phase Comparator

If the component is operated without external synchronization, the sync input must be connected to the sync output for the phase comparator to set the rated voltage at C_{filter}. The VCO then oscillates with rated frequency. In the case of external synchronization, other components can be synchronized with the sync output. The component can be frequency-synchronized, but not phase-synchronized, with the sync input. The duty cycle of the square-wave voltage at the sync input is arbitrary. The best stability as to small phase and frequency interference is achieved with a duty cycle as offered by the sync output.

Push-Pull Flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K2

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge exceeds the lower of the plus levels, both outputs are disabled via the pulse turn-off flipflop. The period during which the respective, active output is low can be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Pulse Turn-Off Flipflop

The pulse turn-off flipflop enables the outputs at the start of each half cycle. If an error signal from comparator K7 or a turn-off signal from K2 is present, the outputs will immediately be switched off.

Comparator K3

Comparator K3 limits the voltage at capacitance $C_{\text{soft start}}$ (and also at K2!) to a maximum of +5 V. The voltage at the ramp generator output may, however, rise to 5.5 V. With a corresponding slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value.

Comparator K4

The comparator has its switching threshold at 1.5 V and sets the error flipflop with its output if the voltage at capacitance $C_{\text{soft start}}$ is below 1.5 V. However, the error flipflop accepts the set signal only if no reset pulse (error) is applied. In this way the outputs cannot be turned on again as long as an error signal is present.

Soft Start

The lower one of the two voltages at the plus inputs of K2 is a measure for the duty cycle at the output. At the instant of turning on the component, the voltage at capacitor $C_{\text{soft start}}$ equals 0 V. As long as no error is present, this capacitor is charged with a current of 6 µA to the maximum value of 5 V. In case of an error, $C_{\text{soft start}}$ is discharged with a current of 2 µA. A set signal is pending at the error flipflop below a charge of 1.5 V and the outputs are enabled if no reset signal is pending simultaneously. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually increased slowly and continuously not before the voltage at $C_{\text{soft start}}$ exceeds 1.8 V.

Error Flipflop

Error signals, which are led to input $\overline{R}$ of the error flipflop, cause an immediate disabling of the outputs, and after the error has been eliminated, the component to switch on again by the soft start.

Comparator K5, K6, K8, V_{REF} Overcurrent Load

These are error detectors which cause immediate disabling of the outputs via the error flipflop when an error occurs. After elimination of the error, the component switches on again by the soft start.

Comparator K7

K7 serves to recognize overcurrents. This is the reason why both inputs of the op amp have been brought out. Turning on is resumed after error recovery at the beginning of the next half period but without using the soft start.

Outputs

Both outputs are transistors with open collectors and operate in a push-pull arrangement. They are actively low. The time in which only one of the two outputs is conductive, can be varied infinitely. The length of the falling edge at VCO is equal to the minimum time during which both outputs are disabled simultaneously.

Reference voltage

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be utilized in the external wiring of the op amp, the error comparators, the ramp generator, or other external components.

Maximum Ratings

Description	Symbol	Conditions	min	max	Unit
Supply voltage	V_S		−0.3	33	V
Voltage at Q1, Q2	V_Q	Q1, Q2 high	−0.3	33	V
Current at Q1, Q2	I_Q	Q1, Q2 low		70	mA
Sync output	$V_{SYNC\ Q}$	SYNC Q high	−0.3	7	V
	$I_{SYNC\ Q}$	SYNC Q low	0	10	mA
Sync input	$V_{SYNC\ I}$		−0.3	33	V
Input C_{filter}	$V_{I\ Cf}$		−0.3	7	V
Input R_T	$V_{I\ RT}$		−0.3	7	V
Input C_T	$V_{I\ CT}$		−0.3	7	V
Input R_R	$V_{I\ RR}$		−0.3	7	V
Input C_R	$I_{I\ CR}$		−10	10	mA
Input comparator K2, K5, K6, K7	$V_{I\ K}$		−0.3	33	V
Output K5	$V_{Q\ K5}$		−0.3	33	V
Reference voltage	V_{REF}		−0.3	V_{REF}	V
Input $C_{soft\ start}$	$V_{I\ soft\ start}$		−0.3	7	V
Junction temperature	T_j			125	°C
Storage temperature	T_{stg}		−55	125	°C
Thermal resistance system – air TDA 4718	$R_{th\ SA}$			70	K/W
TDA 4718 A	$R_{th\ SA}$			60	K/W

Operating Range

Supply voltage	V_S		10.5	30	V
Ambient temperature TDA 4718	T_A		−25	85	°C
TDA 4718 A	T_A		0	70	°C
VCO frequency	f		40	250000	Hz
Ramp generator frequency	f_{RG}		40	250000	Hz

Characteristics

$V_S = 11$ V to 30 V; $T_A = -25$ °C to +85 °C

Description	Symbol	Test conditions	min	typ	max	Unit
Supply current	I_S	$C_T = 1$ nF, $f_{VCO} = 100$ kHz	8		20	mA
Reference						
Reference voltage	V_{REF}	0 mA < I_{REF} < 5 mA	2.35	2.5	2.65	V
Reference voltage change	ΔV_{REF}	14 V ± 20%		8		mV
Reference voltage change	ΔV_{REF}	25 V ± 20%		15		mV
Reference voltage change	ΔV_{REF}	0 mA < I_{REF} < 5 mA			15[1]	mV
Temperature coefficient	TC			0.25	0.4	mV/K
Response threshold of I_{REF} overcurrent	I_{REF}			10		mA
Oscillator (VCO)						
Frequency range	f_{VCO}		40		100000	Hz
Frequency change	$\Delta f/f_{VCO}$	14 V ± 20%		0.5		%
Frequency change	$\Delta f/f_{VCO}$	25 V ± 20%	−1		1	%
Tolerance	$\Delta f/f_{VCO}$	$\Delta R_T = 0, \Delta C_T = 0$	−7		7	%
Fall time sawtooth	t	$C_T = 1$ nF		1		µs
	t	$C_T = 10$ nF		10		µs
RC combination	C_T		0.82		47	nF
VCO	R_T		5		700	kΩ
Ramp Generator						
Frequency range	f		40		100000	Hz
Maximum voltage at C_R	V_H			5.5		V
Minimum voltage at C_R	V_L			1.8		V
Input current through R_R	I_{RR}		0		400	µA
Current transformation ratio	I_{RR}/I_{CR}			1/4		
Synchronization						
Sync output	$V_{Q\,H}$	$I_{Q\,H} = -200$ µA	4			V
	$V_{Q\,L}$	$I_{Q\,L} = 1.6$ mA			0.4	V
Sync input	$V_{I\,H}$		2			V
	$V_{I\,L}$				0.8	V
Input current	$-I_I$				5	µA
Comparator K2						
Input current	$-I_{I\,K2}$				2	µA
Turn-off delay[2]	$t_{D\,OFF}$				500	ns
Input voltage	$V_{I\,K2}$	for duty cycle				
		$D = 0$		1,8		V
		$D =$ max		5		V
Common-mode input voltage range	V_{IC}		0		5.5	V

[1]) At $T_A = 0$ °C to 70 °C, this value falls to max. 5 mV

[2]) At the input: step function $\Delta V = -100$ mV ↛ $\Delta V = +100$ mV

Characteristics

$V_S = 11$ V to 30 V; $T_A = -25\,°C$ to $+85\,°C$

Description	Symbol	Test conditions	min	typ	max	Unit
Soft Start K3, K4						
Charge current for $C_{soft\ start}$	I_{ch}			6		µA
Discharge current for $C_{soft\ start}$	I_{dch}			2		µA
Upper limiting voltage	V_{lim}			5		V
Switching voltage K4	V_{K4}			1.5		V
Output Stages Q1, Q2						
Output voltage	$V_{Q\,H}$				30	V
	$V_{Q\,L}$	$I_Q = 20$ mA			1.1	V
Output leakage current	I_Q	$V_{Q\,H} = 30$ V			2	µA
ON, OFF, Undervoltage K6						
Switching voltage	V		V_{REF}–30mV		V_{REF}+30mV	V
Input current	$-I$				2	µA
Turn-off delay time[1]	$t_{D\,OFF}$			250		ns
Error detection time[1]	t			50		ns
Dynamic Current Limitation K7						
Common-mode input voltage	V_{IC}		0		4	V
Input offset voltage	V_{IO}		−10		10	mV
Input current	$-I_I$				2	µA
Turn-off delay time[2]	$t_{D\,OFF}$			250		ns
Error detection time[2]	t			50		ns
Overvoltage K5						
Switching voltage	V		V_{REF}–30mV		V_{REF}+30mV	V
Input current	$-I_I$				2	µA
Turn-off delay time[1]	$t_{D\,OFF}$			250		ns
Error detection time[1]	t			50		ns
Supply Undervoltage						
Turn-on threshold for V_S rising	V_S	$0\,°C < T_A < 70\,°C$	8.8		11	V
					10.5	V
Turn-off threshold for V_S falling	V_S	$0\,°C < T_A < 70\,°C$	8.5		10.5	V
					10	V
Input C_{filter}						
Rated voltage for rated frequency	V_R			4		V
Frequency approx. proportional to voltage within the range	V_R		3		5	V
Voltage at open sync input	$V_{C\,filter}$			1.6		V

[1]) At the input: step function $V_{REF} = -100$ mV ⇀ $V_{REF} = +100$ mV

[2]) At the input: step function $\Delta V = -100$ mV ⇀ $\Delta V = +100$ mV

Dimensioning Notes for RC Network

1. Determination of the minimum time during which both outputs must be disabled
   → selection of C_T; selection of $C_R \leq C_T$.

2. Determination of the VCO frequency = 2 x output frequency
   → selection of R_T.

3. Determination of the rated slope of the rising ramp generator voltage, which the maximum possible turn-on period per half wave depends on
   → selection of R_R.

4. Duration of the soft start process
   → selection of $C_{soft\ start}$.

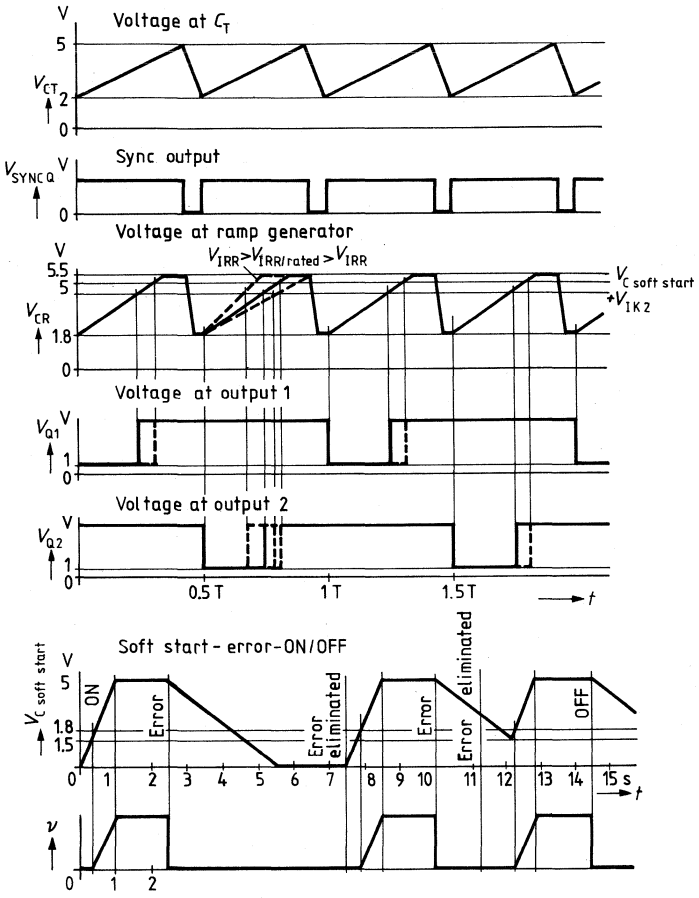
5. In the case of a free-running VCO: connect sync output with sync input.

6. Capacitance C_{filter} is not required in the free-running operation (sync input connected with sync output).

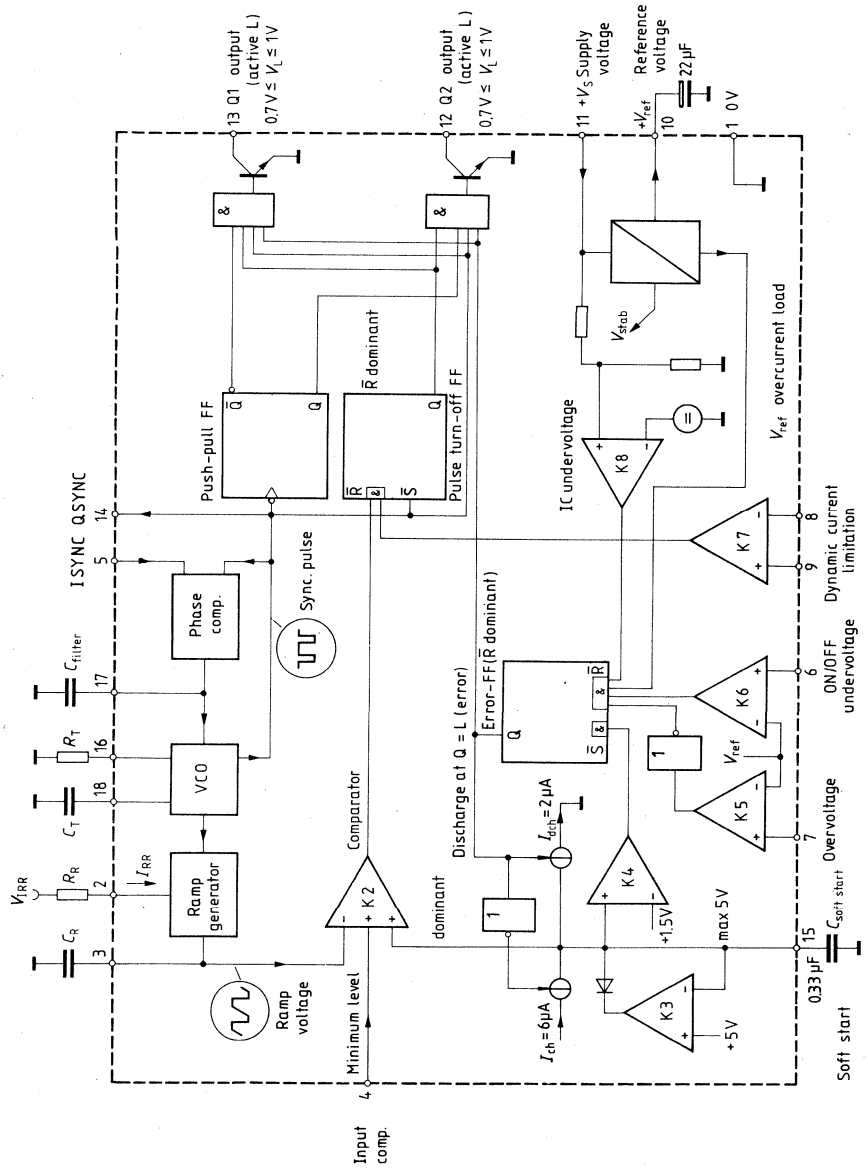
   In the case of external synchronization, that value depends on the selected operating frequency and the required maximum phase interference deviation.

Rated VCO frequency:	100 kHz	50 Hz
C_{filter} favorable:	10 nF	1 µF

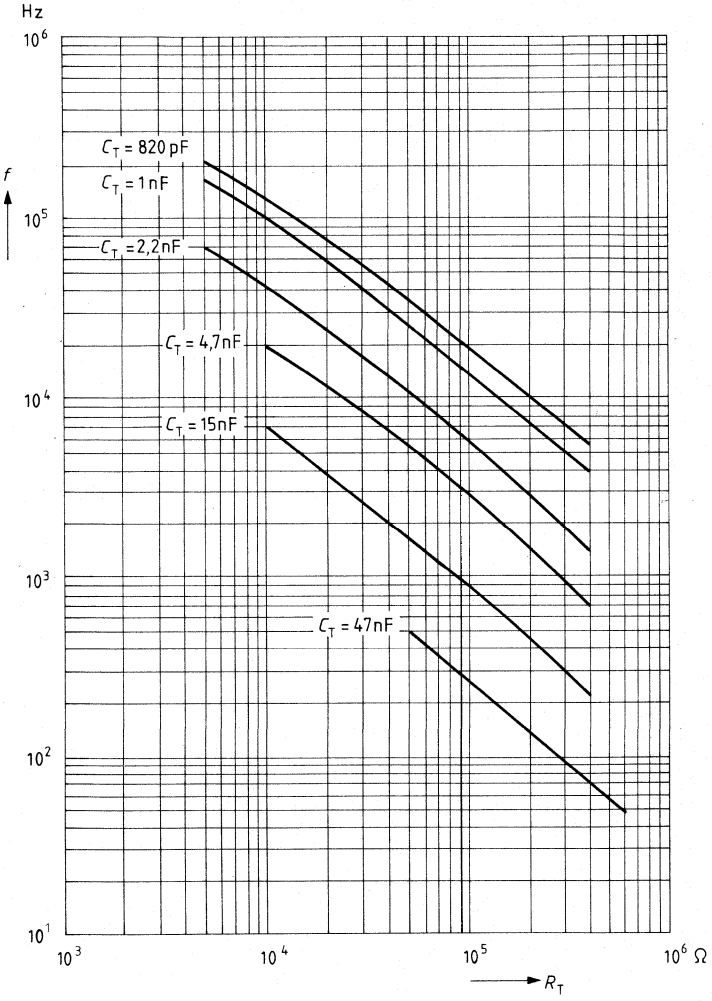
Pulse Diagram



Block Diagram



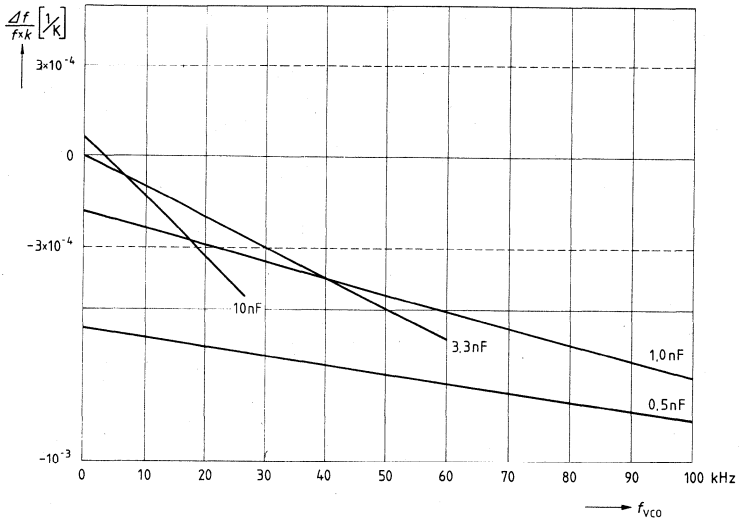
VCO frequency versus R_T and C_T



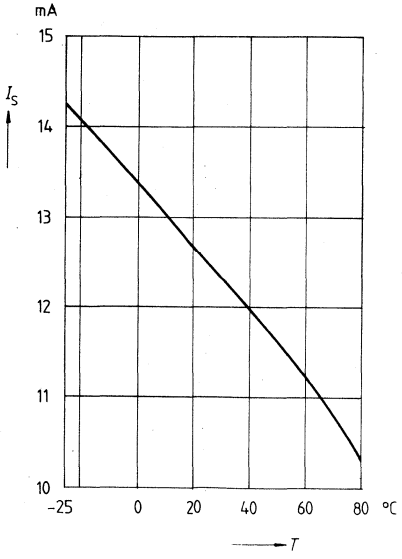
VCO temperature response

$V_S = 12$ V; D = max.

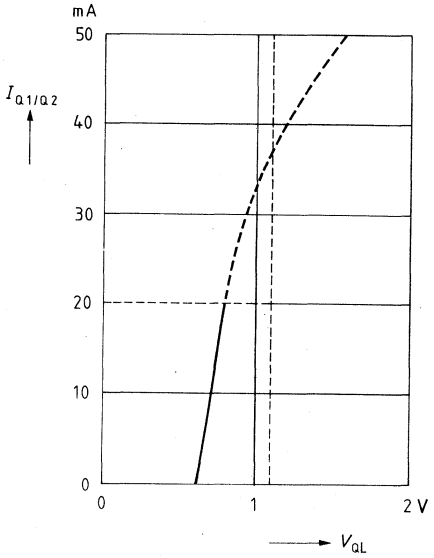
$\frac{\Delta f_{VCO}}{f_K \times K}$ $\left[\frac{1}{K}\right]$ with C_T as parameter



Current consumption versus temperature



Output current versus output voltage



Bipolar IC

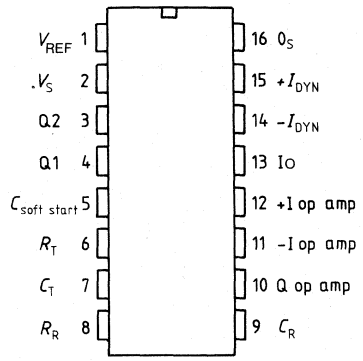
Type	Ordering Code	Package
TDA 4716 A	Q67000-Y865	P-DIP-16
TDA 4716 B	Q67000-Y870	

This versatile, 16-pin SMPS IC comprises digital and analog functions which are required to design high-quality flyback, single-ended, and push-pull converters in normal, half-bridge and full-bridge configurations. The component can also be used in single-ended voltage multipliers and speed-controlled motors. Malfunctions in electrical operation are recognized by the integrated op amps, which activate protective functions.

Features

- Push-pull outputs (open collector)
- Double pulse suppression
- Dynamic current limitation
- Overvoltage protection
- IC undervoltage protection
- Reference voltage source (± 2% for TDA 4716 B)
- Reference overload protection
- Feed-forward control
- Operational amplifier
- Soft start

Pin Configuration
top view



Pin Description

Pin	Symbol	Function
1	V_{REF}	Reference voltage V_{REF}
2	V_S	Supply voltage V_S
3	Q2	Output Q2
4	Q1	Output Q1
5	$C_{soft\ start}$	Soft start
6	R_T	VCO R_T
7	C_T	VCO C_T
8	R_R	Ramp generator R_R
9	C_R	Ramp generator C_R
10	Q op amp	Operational amplifier output
11	−I op amp	Operational amplifier input (−)
12	+I op amp	Operational amplifier Input (+)
13	I O	Input overvoltage
14	$-I_{DYN}$	Dynamic current limitation (−)
15	$+I_{DYN}$	Dynamic current limitation (+)
16	0_S	Ground 0 V

Circuit Description

The following is a description of the individual functional units and their interaction.

Voltage Controlled Oscillator (VCO)

The VCO generates a sawtooth voltage. The duration of the falling edge is determined by the value of C_T. The duration of the rising edge of the waveform and, therefore, approximately the frequency, is determined by the value of R_T. During the fall time, the VCO provides a trigger signal for the ramp generator, as well as an L signal for a number of IC parts to be controlled.

Ramp Generator

The ramp generator is triggered by the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator waveform is to be shorter than the fall time of the VCO. To control the pulse width at the output, the voltage of the rising edge of the ramp generator signal is compared with a dc voltage at comparator K2. The slope of the rising edge of the ramp generator signal is controlled by the current through R_R. This offers the possibility of an additional, superimposed control of the output duty cycle. This additional control capability, called »feed-forward control«, is utilized to compensate for known interference such as ripple on the input voltage.

Push-Pull Flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K2

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge exceeds the lower of the two plus levels, both outputs are disabled via the pulse turn-off flipflop. The period during which the respective, active output is low can be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Operational Amplifier K1

The op amp K1 is a high-quality amplifier. Fluctuations in the output voltage of the power supply are amplified by K1 and applied to the free + input of comparator K2. Variations in output voltage are, in this way, converted to a corresponding change in output duty cycle. K1 has a common-mode input voltage range between 0 V and +5 V.

Pulse Turn-Off Flipflop

The pulse turn-off flipflop enables the outputs at the start of each half cycle. If an error signal from comparator K7 or a turn-off signal from K2 is present, the outputs will immediately be switched off.

Comparator K3

Comparator K3 limits the voltage of capacitance $C_{soft\ start}$ (and also at K2!) to a maximum of +5 V. The voltage at the ramp generator output may, however, rise to 5.5 V. With a corresponding slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value.

Comparator K4

The comparator has its switching threshold at 1.5 V and sets the error flipflop with its output if the voltage at capacitance $C_{soft\ start}$ is below 1.5 V. However, the error flipflop accepts the set signal only if no reset pulse (error) is applied. In this way the outputs cannot be turned on again as long as an error signal is present.

Soft Start

The lower one of the two voltages at the plus inputs of K2 is a measure for the duty cycle at the output. At the instant of turning on the component, the voltage at capacitor $C_{soft\ start}$ equals 0 V. As long as no error is present, this capacitor is charged with a current of 6 µA at the maximum value of 5 V. In case of an error, $C_{soft\ start}$ is discharged with a current of 2 µA. A set signal is pending at the error flipflop below a charge of 1.5 V and the outputs are enabled if no reset signal is pending simultaneously. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually increased slowly and continuously not before the voltage at $C_{soft\ start}$ exceeds 1.8 V.

Error Flipflop

Error signals, which are led to input $\overline{R}$ of the error flipflop cause an immediate disabling of the outputs, and after the error has been eliminated, the component to switch on again by the soft start.

Comparator K5, K8, V_{REF} Overcurrent Load

These are error detectors which cause immediate disabling of the outputs via the error flipflop when an error occurs. After elimination of the error, the component switches on again by the soft start.

Comparator K7

K7 serves to recognize overcurrents. This is the reason why both inputs of the operational amplifier have been brought out. Turning on is resumed after error recovery at the beginning of the next half period but without using the soft start. K7 has a common-mode input voltage range between 0 V and +4 V. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

Outputs

Both outputs are transistors with open collectors and operate in a push-pull arrangement. They are actively low. The time in which only one of the two outputs is conductive can be varied infinitely. The length of the falling edge at VCO is equal to the minimum time during which both outputs are disabled simultaneously. The minimum L voltage is 0.7 V.

Reference Voltage

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be utilized in the external wiring of the op amp, the error comparators, the ramp generator, or other external components.

Maximum Ratings

Description	Symbol	Conditions	min	max	Unit
Supply voltage	V_S		−0.3	33	V
Voltage at Q1, Q2	V_Q	Q1, Q2 high	−0.3	33	V
Current at Q1, Q2	I_Q	Q1, Q2 low		70	mA
Input R_T	$V_{I\,RT}$		−0.3	7	V
Input C_T	$V_{I\,CT}$		−0.3	7	V
Input R_R	$V_{I\,RR}$		−0.3	7	V
Input C_R	$I_{I\,CR}$		−10	10	mA
Input comparator K5, K7	$V_{I\,K,\,5,\,7}$		−0.3	33	V
Output K5	$V_{Q\,K5}$		−0.3	33	V
Input op amp	$V_{I\,Op\,Amp}$		−0.3	33	V
Output op amp	$V_{Q\,Op\,Amp}$		−0.3	V_S−1 max. 7 V	V
Reference voltage	$V_{Q\,REF}$		−0.3	V_{REF}	V
Input $C_{soft\ start}$	$V_{I\,soft\ start}$		−0.3	7	V
Junction temperature	T_j			125	°C
Storage temperature	T_{stg}		−55	125	°C
Thermal resistance system – air	$R_{th\,SA}$			60	K/W

Operating Range

Supply voltage TDA 4716 A	V_S		10.5	30	V
TDA 4716 B	V_S		11	30	V
Ambient temperature TDA 4716 A	T_A		0	70	°C
TDA 4716 B	T_A		−25	85	°C
Frequency	f		40	100000	Hz
VCO frequency	f_{VCO}		40	250000	Hz
Ramp generator frequency	f_{RG}		40	250000	Hz

Characteristics

Description	Symbol	TDA 4716 A min	TDA 4716 A typ	TDA 4716 A max	TDA 4716 B min	TDA 4716 B typ	TDA 4716 B max	Unit
Supply voltage	V_S	10.5		30	11		30	V
Ambient temperature	T_A	0		70	−25		85	°C
Supply current $C_T = 1$ nF $f_{VCO} = 100$ kHz	I_S	8		16	8		20	mA
Reference								
Reference voltage 0 mA < I_{REF} < 5 mA	V_{REF}	2.35	2.5	2.65	2.45	2.5	2.55	V
Voltage change $V_S = 14$ V ± 20%	ΔV_{REF}		8			8		mV
Voltage change $V_S = 25$ V ± 20%	ΔV_{REF}		15			15		mV
Voltage change 0 mA < I_{REF} < 5 mA	ΔV_{REF}			5			15	mV
Temperature coefficient	TC		0.25	0.4		0.25	0.4	mV/K
Response threshold of I_{REF} overcurrent	I_{REF}		10			10		mA
Oscillator (VCO)								
Frequency range	f	40		100000	40		100000	Hz
Frequency change $V_S = 14$ V ± 20%	$\Delta f/f$		0.5			0.5		%
Frequency change $V_S = 25$ V ± 20%	$\Delta f/f$	−1		1	−1		1	%
Tolerance $\Delta R_T = 0; \Delta C_T = 0$	$\Delta f/f$	−7		7	−7		7	%
Fall time sawtooth								
$C_T = 1$ nF			1			1		µs
$C_T = 10$ nF			10			10		µs
RC combination	C_T	0.82		47	0.82		47	nF
VCO	R_T	5		700	5		700	kΩ
Ramp Generator								
Frequency range	f_{RG}	40		100000	40		100000	Hz
Maximum voltage at C_R	V_H		5.5			5.5		V
Minimum voltage at C_R	V_L		1.8			1.8		V
Input current through R_R	I_{RR}	0		400	0		400	µA
Current transformation ratio	I_{RR}/I_{CR}		1/4			1/4		

Description	Symbol	TDA 4716 A min	TDA 4716 A typ	TDA 4716 A max	TDA 4716 B min	TDA 4716 B typ	TDA 4716 B max	Unit
Comparator K2								
Input current	$-I_{K2}$			2			2	µA
Turn-off delay time[1])	$t_{D\ OFF}$			500			500	ns
Input voltage	$V_{I\ K2}$							
Duty cycle $D = 0$			1.8			1.8		V
D = max			5			5		V
Common-mode input voltage range	V_{IC}	0		5.5	0		5.5	V
Soft Start K3, K4								
Charge current for $C_{soft\ start}$	I_{ch}		6			6		µA
Discharge current for $C_{soft\ start}$	I_{dch}		2			2		µA
Upper limiting voltage	V_{lim}		5			5		V
Switching voltage K4	$V_{K\ 4}$		1.5			1.5		V
Operational Amplifier								
Open-loop voltage gain	G_{V0}	60	80		60	80		dB
Input offset voltage	V_{IO}	−10		10	−10		10	mV
Temperature coefficient of V_{IO}	TC	−30		30	−30		30	µV/K
Input current	$-I_I$			2			2	µA
Common-mode input voltage range	V_{IC}	0		5	0		5	V
Output current	I_Q	−3		1.5	−3		1.5	mA
Rise time of output voltage	$\Delta V/\Delta t$		1			1		V/µs
Transition frequency	f_T		3			3		MHz
Phase at f_T	φ_T		120			120		degr
Output voltage −3 mA < I < 1.5 mA	$V_{Q\ H/L}$	1.5		5.5	1.5		5.5	V
Output Stages Q1, Q2								
Output voltage	V_{QH}			30			30	V
I_Q = 20 mA	V_{QL}			1.1			1.1	V
Output leakage current V_{QH} = 30 V	I_Q			2			2	µA

[1]) At the input: step function $\Delta V = -100$ mV ↛ $\Delta V = +100$ mV

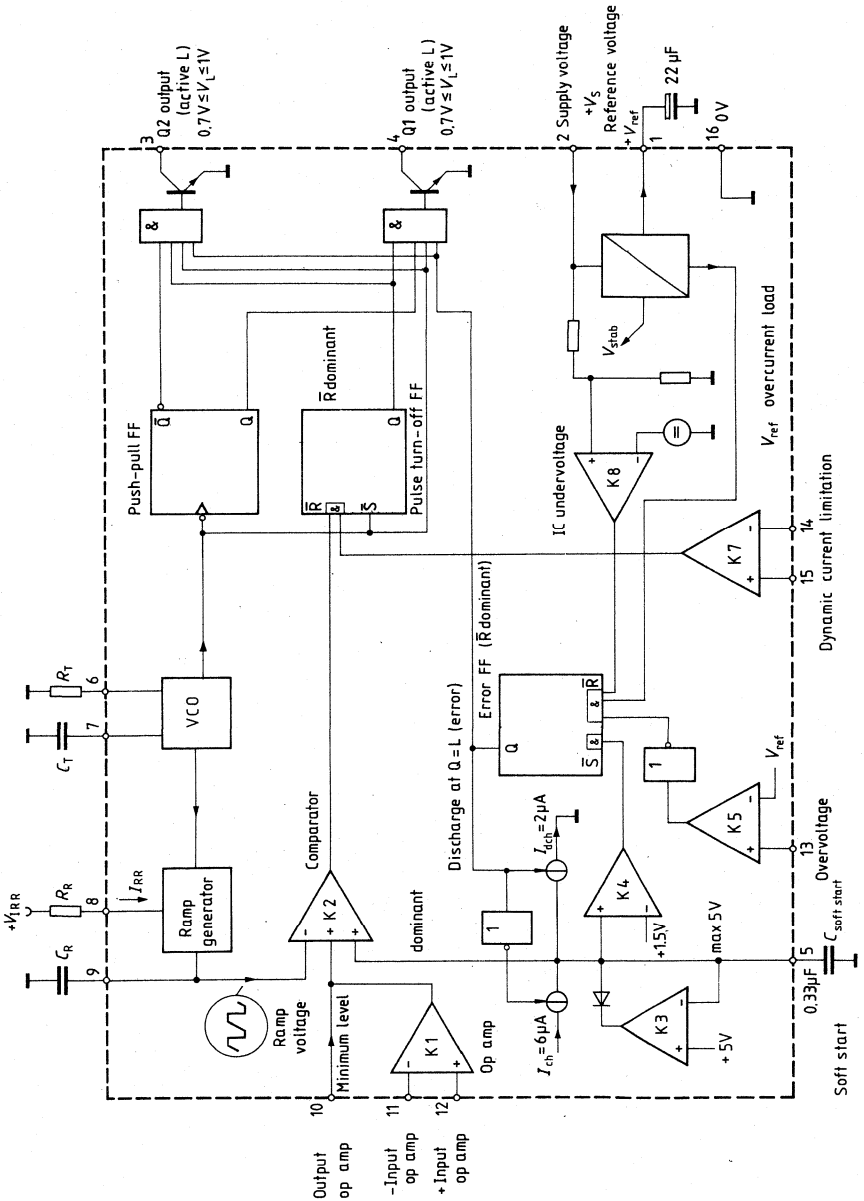
Description	Symbol	TDA 4716 A min	TDA 4716 A typ	TDA 4716 A max	TDA 4716 B min	TDA 4716 B typ	TDA 4716 B max	Unit
Dynamic Current Limitation K7								
Common-mode input voltage range	V_{IC}	0		4	0		4	V
Input offset voltage	V_{IO}	−10		10	−10		10	mV
Input current	$-I_I$			2			2	µA
Turn-off delay time[2]	$t_{D\ OFF}$		250			250		ns
Error detection time[2]	t		50			50		ns
Overvoltage K5								
Switching voltage	V	V_{REF} − 30 mV		V_{REF} + 30 mV	V_{REF} − 30 mV		V_{REF} + 30 mV	V
Input current	$-I_I$			2			2	µA
Turn-off delay time[1]	$t_{D\ OFF}$		250			250		ns
Error detection time[1]	t		50			50		ns
Supply Undervoltage								
Turn-on threshold for V_S, rising	V_S	8.8		10.5	8.8		11	V
Turn-off threshold for V_S, falling	V_S	8.5		10	8.5		10.5	V

[1]) At the input: step function $V_{REF} = -100$ mV ⌐→ $V_{REF} = +100$ mV
[2]) At the input: step function $\Delta V = -100$ mV ⌐→ $\Delta V = +100$ mV

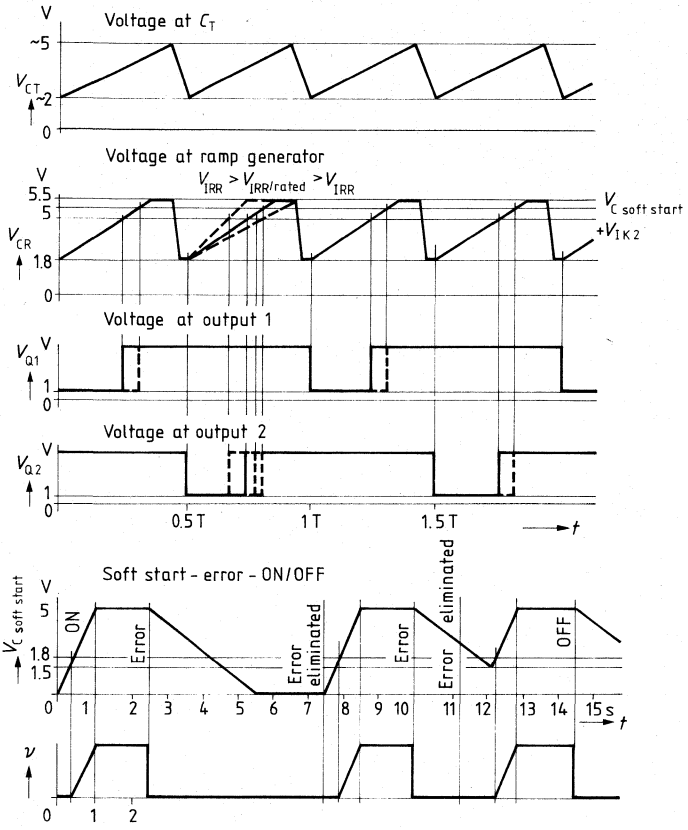
Dimensioning Notes for RC Network

1. Determination of the minimum time during which both outputs must be disabled
   → selection of C_T; selection of $C_R \leq C_T$.
2. Determination of the VCO frequency = 2 x output frequency
   → selection of R_T.
3. Determination of the rated slope of the rising ramp generator voltage, which the maximum possible turn-on period per half wave depends on
   → selection of R_R.
4. Duration of the soft start process
   → selection of $C_{soft\ start}$
5. Wiring of the operational amplifier according to the dynamic requirements

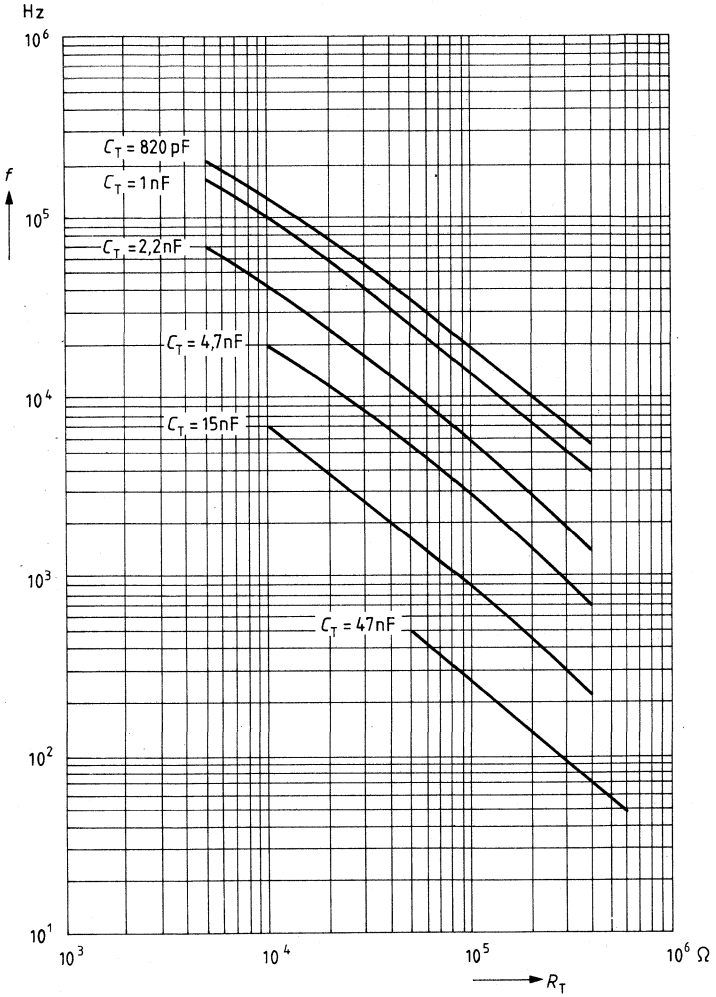
Block Diagram



Pulse Diagram



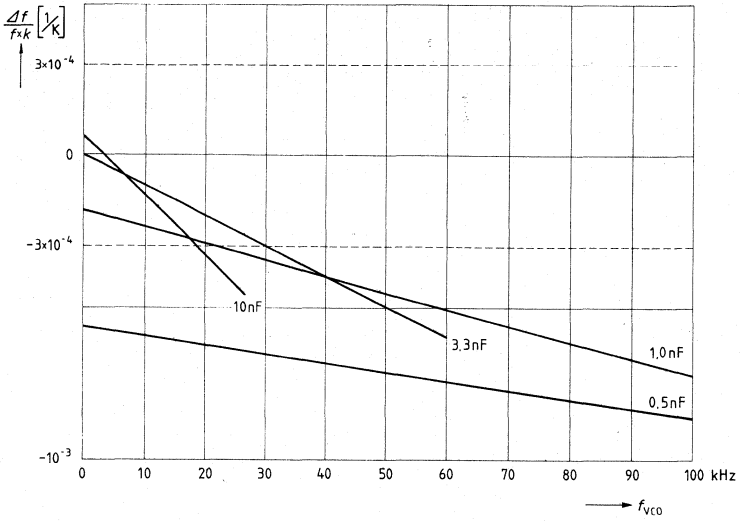
VCO frequency versus R_T and C_T



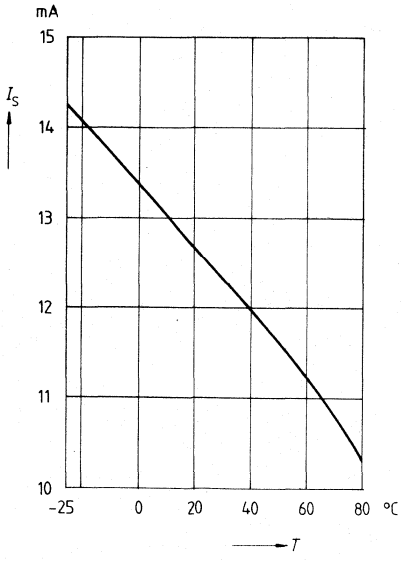
VCO temperature response

$V_S = 12$ V; D = max.

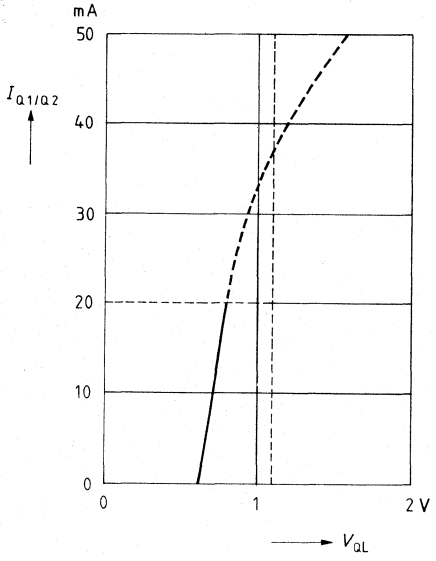
$\frac{\Delta f_{VCO}}{f_K \times K}$ $\left[\frac{1}{K}\right]$ with C_T as parameter



Supply current versus temperature



Output current versus L output voltage



Bipolar IC

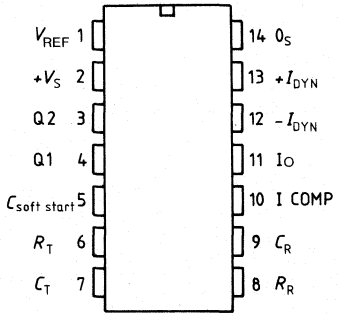
Type	Ordering Code	Package
S TDA 4714 A	Q67000-Y864	P-DIP-14
S TDA 4714 B	Q67000-Y869	

This versatile, 14-pin SMPS IC comprises digital and analog functions which are required to design high-quality flyback, single-ended, and push-pull converters in normal, half-bridge and full-bridge configurations. The component can also be used in single-ended voltage multipliers and speed-controlled motors. Malfunctions in electrical operation are recognized by the integrated op amps which activate protective functions.

Features

- Push-pull outputs (open collector)
- Double pulse suppression
- Dynamic current limitation
- Overvoltage protection
- IC undervoltage protection
- Reference voltage source (± 2% for TDA 4714 B)
- Reference overload protection
- Soft start
- Feed-forward control

Pin Configuration
top view



Pin Description

Pin	Symbol	Function
1	V_{REF}	Reference voltage
2	$+ V_S$	Supply voltage
3	Q2	Output Q2
4	Q1	Output Q1
5	$C_{soft\ start}$	Soft start
6	R_T	VCO R_T
7	C_T	VCO C_T
8	R_R	Ramp generator R_R
9	C_R	Ramp generator C_R
10	I COMP	Input comparator
11	I O	Input overvoltage
12	$-I_{DYN}$	Dynamic current limitation (–)
13	$+I_{DYN}$	Dynamic current limitation (+)
14	0_S	0_S

Circuit Description

The following is a description of the individual functional units and their interaction.

Voltage Controlled Oscillator (VCO)

The VCO generates a sawtooth voltage. The duration of the falling edge is determined by the value of C_T. The duration of the rising edge of the waveform and, therefore, approximately the frequency, is determined by the value of R_T. During the fall time, the VCO provides a trigger signal for the ramp generator, as well as an L signal for a number of IC parts to be controlled.

Ramp Generator

The ramp generator is triggered by the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator waveform is to be shorter than the fall time of the VCO. To control the pulse width at the output, the voltage of the rising edge of the ramp generator signal is compared with a dc voltage at comparator K2. The slope of the rising edge of the ramp generator signal is controlled by the current through R_R. This offers the possibility of an additional, superimposed control of the output duty cycle. This additional control capability, called »feed-forward control«, is utilized to compensate for known interference such as ripple on the input voltage.

Push-Pull Flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K2

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge exceeds the lower of the two plus levels, both outputs are disabled via the pulse turn-off flipflop. The period during which the respective, active output is low can be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Pulse Turn-Off Flipflop

The pulse turn-off flipflop enables the outputs at the start of each half cycle. If an error signal from comparator K7 or a turn-off signal from K2 is present, the outputs will immediately be switched off.

Comparator K3

Comparator K3 limits the voltage at capacitance $C_{\text{soft start}}$ (and also at K2!) to a maximum of +5 V. The voltage at the ramp generator output may, however, rise to 5.5 V. With a corresponding slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value.

Comparator K4

The comparator has its switching threshold at 1.5 V and sets the error flipflop with its output if the voltage at capacitance $C_{\text{soft start}}$ is below 1.5 V. However, the error flipflop accepts the set signal only if no reset pulse (error) is applied. In this way, the outputs cannot be turned on again as long as an error signal is present.

Soft Start

The lower one of the two voltages at the plus inputs of K2 is a measure for the duty cycle at the output. At the instant of turning on the component, the voltage at capacitor $C_{soft\ start}$ equals 0 V. As long as no error is present, this capacitor is charged with a current of 6 µA to the maximum value of 5 V. In case of an error, $C_{soft\ start}$ is discharged with a current of 2 µA. A set signal is pending at the error flipflop below a charge of 1.5 V and the outputs are enabled if no reset signal is pending simultaneously. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually increased slowly and continuously not before the voltage at $C_{soft\ start}$ exceeds 1.8 V.

Error Flipflop

Error signals, which are led to input $\overline{R}$ of the error flipflop cause an immediate disabling of the outputs, and after the error has been eliminated, the component to switch on again by the soft start.

Comparator K5, K8, V_{REF} Overcurrent Load

These are error detectors which cause immediate disabling of the outputs via the error flipflop when an error occurs. After elimination of the error, the component switches on again by the soft start.

Comparator K7

K7 serves to recognize overcurrents. This is the reason why both inputs of the op amp have been brought out. Turning on is resumed after error recovery at the beginning of the next half period but without using the soft start. K7 has a common-mode input voltage range between 0 V and 4 V. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

Outputs

Both outputs are transistors with open collectors and operate in a push-pull arrangement. They are actively low. The time in which only one of the two outputs is conductive can be varied infinitely. The length of the falling edge at VCO is equal to the minimum time during which both outputs are disabled simultaneously. The minimum L voltage is 0.7 V.

Reference Voltage

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be utilized in the external wiring of the op amp, the error comparators, the ramp generator, or other external components.

Maximum Ratings

Description	Symbol	Conditions	min	max	Unit
Supply voltage	V_S		−0.3	33	V
Voltage at Q1, Q2	V_Q	Q1, Q2 high	−0.3	33	V
Current at Q1, Q2	I_Q	Q1, Q2 low		70	mA
Input R_T	$V_{I\,RT}$		−0.3	7	V
Input C_T	$V_{I\,CT}$		−0.3	7	V
Input R_R	$V_{I\,RR}$		−0.3	7	V
Input C_R	$I_{I\,CR}$		−10	10	mA
Input comparator K2, K5, K7	$V_{IK\,2,\,5,\,7}$		−0.3	33	V
Output K5	$V_{QK\,5}$		−0.3	33	V
Reference voltage	$V_{Q\,REF}$		−0.3	V_{REF}	V
Input $C_{soft\ start}$	$V_{I\,soft\ start}$		−0.3	7	V
Junction temperature	T_j			125	°C
Storage temperature	T_{stg}		−55	125	°C
Thermal resistance system – air	$R_{th\,SA}$			60	K/W

Operating Range

Supply voltage TDA 4714 A	V_S		10.5	30	V
TDA 4714 B	V_S		11	30	V
Ambient temperature TDA 4714 A	T_A		0	70	°C
TDA 4714 B	T_A		−25	85	°C
Frequency range	f		40	100000	Hz
VCO frequency	f_{VCO}		40	250000	Hz
Ramp generator frequency	f_{RG}		40	250000	Hz

Characteristics

Description	Symbol	TDA 4714 A min	TDA 4714 A typ	TDA 4714 A max	TDA 4714 B min	TDA 4714 B typ	TDA 4714 B max	Unit
Supply voltage	V_S	10.5		30	11		30	V
Ambient temperature	T_A	0		70	−25		85	°C
Supply current $C_T = 1$ nF $f_{VCO} = 100$ kHz	I_S	8		16	8		20	mA
Reference								
Reference voltage 0 mA < I_{REF} < 5 mA	V_{REF}	2.35	2.5	2.65	2.45	2.5	2.55	V
Voltage change $V_S = 14$ V ± 20%	ΔV_{REF}		8			8		mV
Voltage change $V_S = 25$ V ± 20%	ΔV_{REF}		15			15		mV
Voltage change 0 mA < I_{REF} < 5 mA	ΔV_{REF}			5			15	mV
Temperature coefficient	TC		0.25	0.4		0.25	0.4	mV/K
Response threshold of I_{REF} overcurrent	I_{REF}		10			10		mA
Oscillator (VCO)								
Frequency range	f	40		100000	40		100000	Hz
Frequency change $V_S = 14$ V ± 20%	$\Delta f/f$		0.5			0.5		%
Frequency change $V_S = 25$ V ± 20%	$\Delta f/f$	−1		1	−1		1	%
Tolerance $\Delta R_T = 0$; $\Delta C_T = 0$	$\Delta f/f$	−7		7	−7		7	%
Fall time sawtooth $C_T =$ 1 nF $C_T = 10$ nF			1 10			1 10		µs µs
RC combination	C_T	0.82		47	0.82		47	nF
VCO	R_T	5		700	5		700	kΩ
Ramp Generator								
Frequency range	f_{RG}	40		100000	40		100000	Hz
Maximal voltage at C_R	V_H		5.5			5.5		V
Minimum voltage at C_R	V_L		1.8			1.8		V
Input current through R_R	I_{RR}	0		400	0		400	µA
Current transformation ratio	I_{RR}/I_{CR}		1/4			1/4		

Description	Symbol	TDA 4714 A min	TDA 4714 A typ	TDA 4714 A max	TDA 4714 B min	TDA 4714 B typ	TDA 4714 B max	Unit
Comparator K2								
Input current	$-I_{K2}$			2			2	µA
Turn-off delay time[1])	$t_{D\ OFF}$			500			500	ns
Input voltage	$V_{I\ K2}$							
Duty cycle $D = 0$			1.8			1.8		V
Duty cycle D = max.			5			5		V
Common-mode input voltage range	V_{IC}	0		5.5	0		5.5	V
Soft Start K3, K4								
Charge current for $C_{soft\ start}$	I_{ch}		6			6		µA
Discharge current for $C_{soft\ start}$	I_{dch}		2			2		µA
Upper limiting voltage	V_{lim}		5			5		V
Switching voltage K4	V_{K4}		1.5			1.5		V
Output Stages Q1, Q2								
Output voltage $I_Q = 20$ mA	V_{QH}			30			30	V
	V_{QL}			1.1			1.1	V
Output leakage current $V_{QH} = 30$ V	I_Q			2			2	µA
Dynamic Current Limitation K7								
Common-mode input voltage range	V_{IC}	0		4	0		4	V
Input offset voltage	V_{IO}	−10		10	−10		10	mV
Input current	$-I_I$			2			2	µA
Turn-off delay time[1])	$t_{D\ OFF}$		250			250		ns
Error detection time[1])	t		50			50		ns
Overvoltage K5								
Switching voltage	V	V_{REF} − 30 mV		V_{REF} + 30 mV	V_{REF} − 30 mV		V_{REF} + 30 mV	V
Input current	$-I_I$			2			2	µA
Turn-off delay time[2])	$t_{D\ OFF}$		250			250		ns
Error detection time[2])	t		50			50		ns
Supply Undervoltage								
Turn-on threshold for V_S, rising	V_S	8.8		10.5	8.8		11	V
Turn-off threshold for V_S, falling	V_S	8.5		10	8.5		10.5	V

[1]) At the input: step function $\Delta V = -100$ mV ⌐→ $V = +100$ mV

[2]) At the input: step function $V_{REF} = -100$ mV⌐→$\Delta V_{REF} = +100$ mV

Dimensioning Notes for RC Network

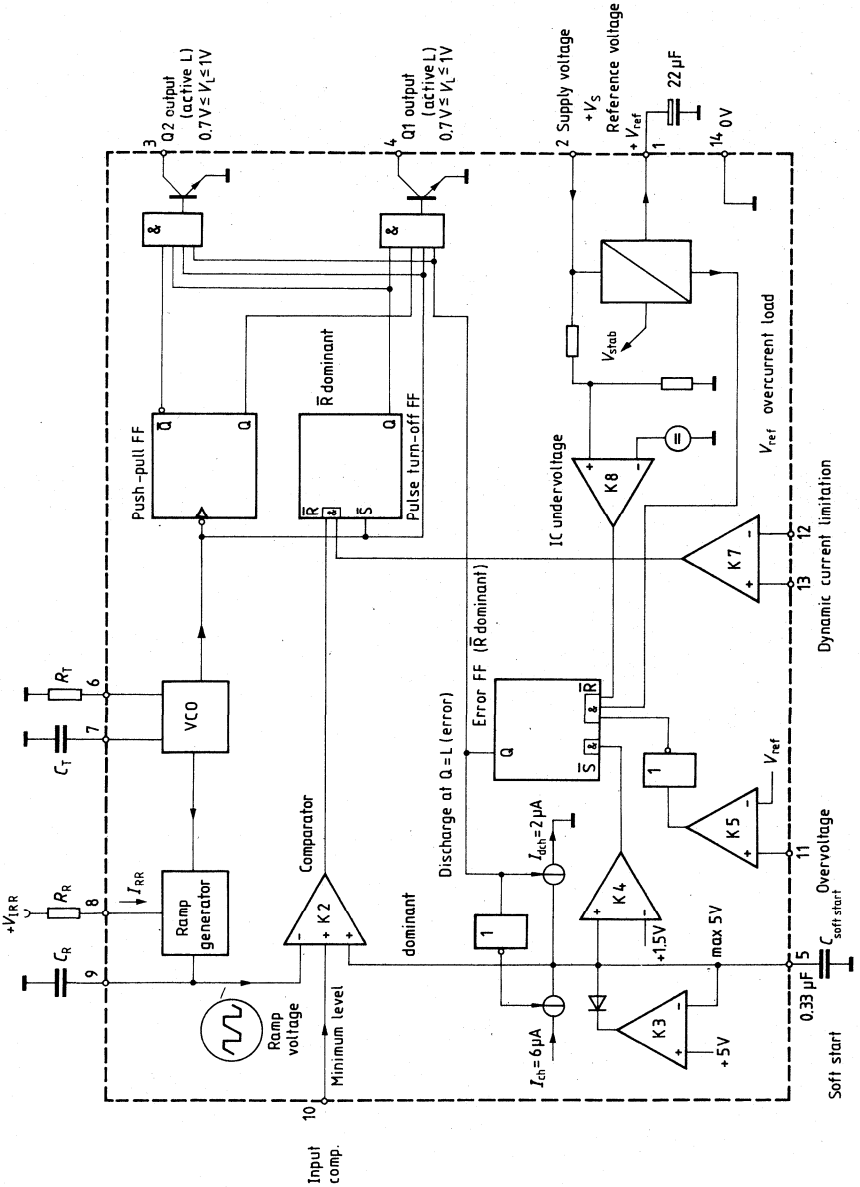
1. Determination of the minimum time during which both outputs must be disabled
   → selection of C_T; selection of $C_R \leq C_T$.

2. Determination of the VCO frequency = 2 x output frequency
   → selection of R_T.

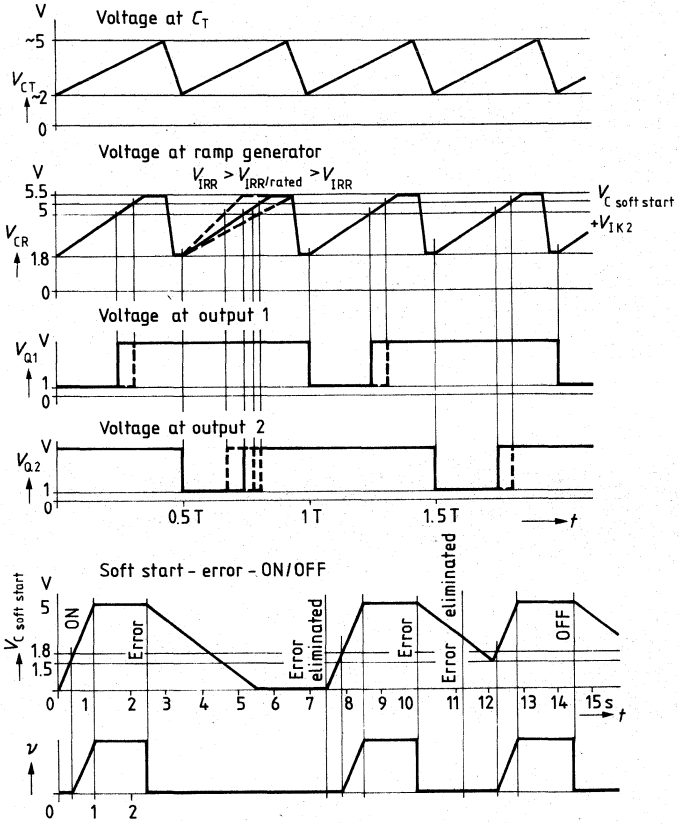
3. Determination of the rated slope of the rising ramp generator voltage, which the maximum possible turn-on period per half wave depends on
   → selection of R_R.

4. Duration of the soft start process
   → selection of $C_{soft\ start}$.

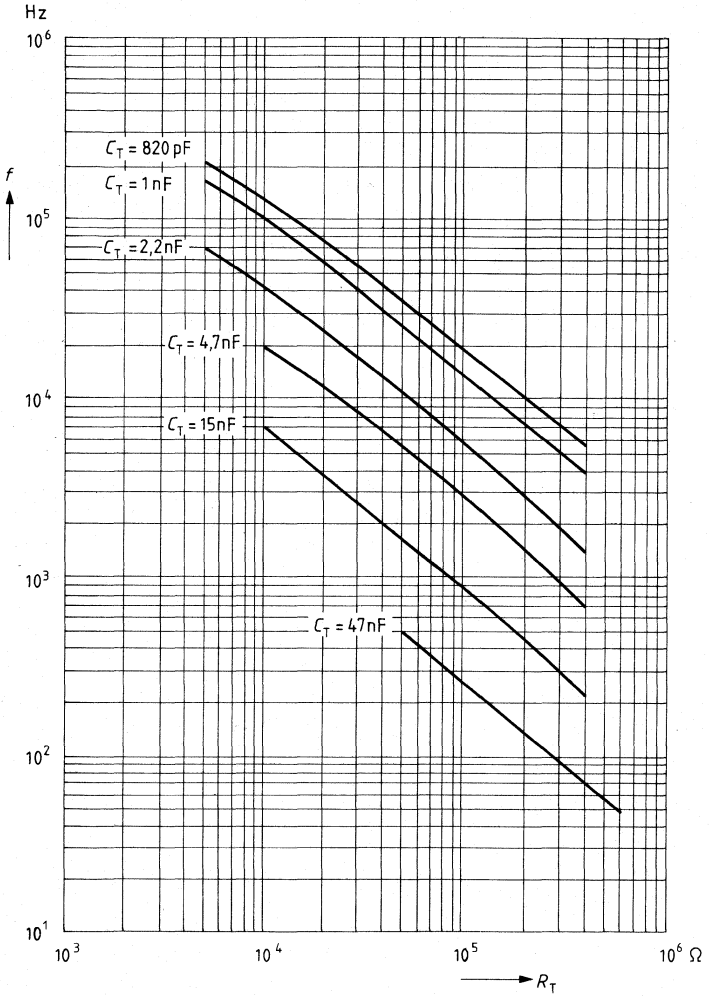
Block Diagram



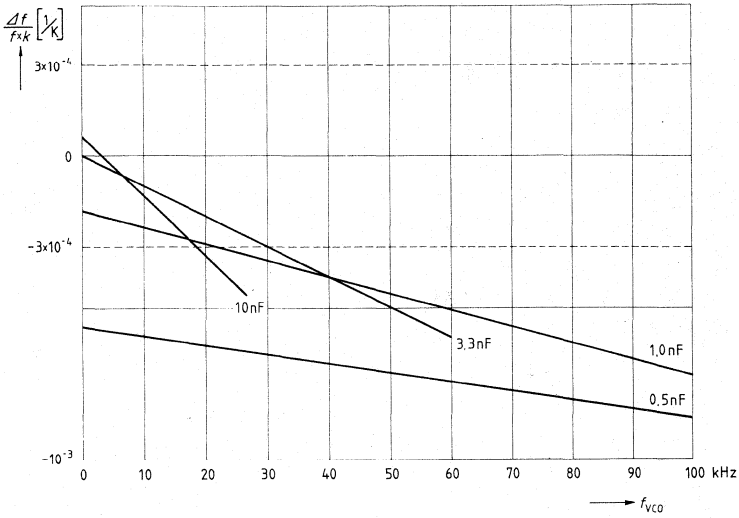
Pulse Diagram



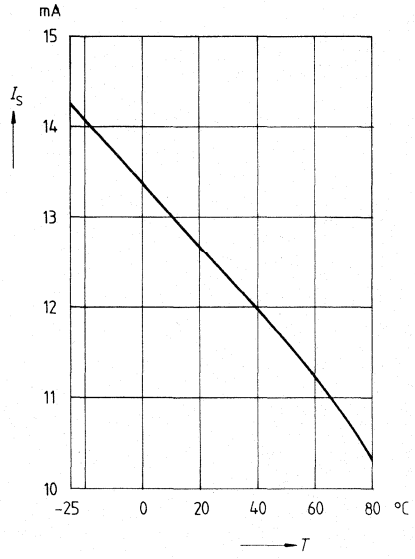
VCO frequency versus R_T and C_T



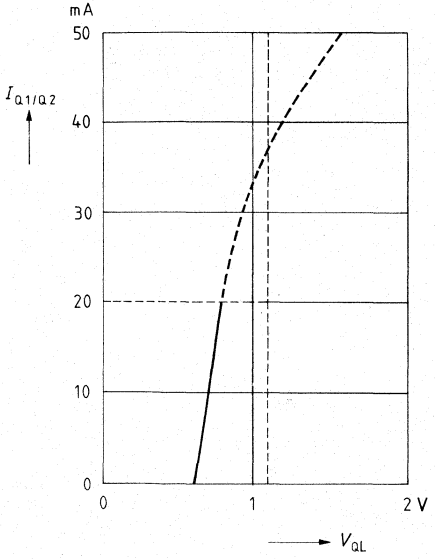
VCO temperature response
$V_S = 12$ V; D = max.
$\frac{\Delta f_{VCO}}{f_K \times K} \left[\frac{1}{K}\right]$ with C_T as parameter



Supply current versus temperature



Output current versus L output voltage



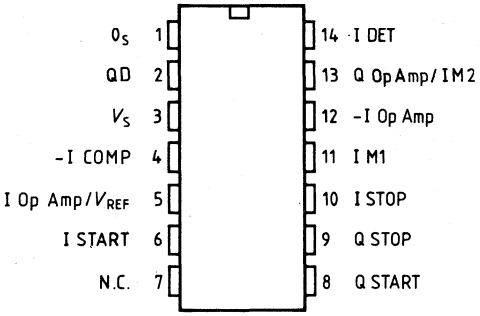
Bipolar IC

Type	Ordering Code	Package
TDA 4814 A	Q67000-A8163	P-DIP-14

This device contains the components for designing a switch-mode power supply with sinusoidal line-current consumption. Sinusoidal line current is drawn from the supply network in particular when there is high power consumption. One possible application is in electronic ballasts for fluorescent lamps, especially when a large number of these lamps are concentrated on one supply point. This IC is additionally suitable for general driving of switch-mode power supplies. The possibility of regulating the output voltage will enable operation on different line voltages (110 Vac/220 Vac) without any switchover.

A monitoring circuit makes it possible to control various turn-on and turn-off functions of different units of equipment.

Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	0_S	Ground 0 V
2	QD	Driver output
3	V_S	Supply voltage
4	–I COMP	Negative comparator input
5	+I Op Amp/V_{REF}	Positive input
6	I START	Start input
7	N.C.	Not connected
8	Q START	Start output
9	Q STOP	Stop output
10	I STOP	Stop input
11	I M1	Multiplier input M1
12	–I Op Amp	Negative input Op Amp
13	Q Op Amp/I M2	Op Amp output/ multiplier input M2
14	I DET	Detector input

Circuit Description

The IC switches from standby to full current consumption when the turn-on threshold on V_S is exceeded. Turn-off is controlled by hysteresis. The integrated Z diode limits the voltage on V_S when impressed current is fed.

The operational amplifier (op amp) can be wired as a control amplifier. It will then compare the divided output voltage V_Q to a reference voltage V_{REF} that is stable with temperature. The output voltage of the op amp that is produced in this way is multiplied by a sine-magnitude voltage in the multiplier (M). At the output of the latter a sine-magnitude voltage then appears that is variable in amplitude. This nominal voltage is applied to the plus input of the comparator. The nominal voltage at the multiplier output can then be compared via the comparator to a voltage derived from the actual line current. The output of the comparator feeds the reference signal via a logic circuit to the driver that switches the SIPMOS transistor. No current gaps may appear in the choke, otherwise the line current would no longer be sinusoidal. To achieve that, the detector input I DET senses when the choke current has fallen to zero after turn-off of the SIPMOS transistor. This ensures that the SIPMOS transistor does not turn on too early and that no current gaps occur.

When the detector input I DET is on High potential, the SIPMOS driver output QD is blocked. At the same time the flipflop can be set by the comparator.

When I DET is Low, the Q output is enabled and can be disabled again by the comparator by resetting the flipflop.

Consequently the choke is always currentless when the SIPMOS transistor turns on and no current gaps appear in the choke.

Driver Output QD for SIPMOS Transistors

The output driver is designed as a push-pull stage. There is a resistor of 10 Ω in series with the output for the purpose of current limiting. Between Q and ground there is a resistor of 10 kΩ. This keeps the SIPMOS transistor reliably turned off during standby.

The Q output is additionally connected to the supply voltage V_S and to ground by way of diodes.

When the supply voltage to the switched-mode power supply is turned on, the diode towards V_S conducts the capacitive displacement currents from the gate of the SIPMOS transistor into the smooting capacitor on V_S. The voltage V_S may not exceed 0.7 V if the SIPMOS transistor is to remain turned off.

The diode towards ground clamps negative voltages on Q to −0.7 V. Capacitive currents produced by voltage incursion on the drain of the SIPMOS transistor are thus able to flow away unhindered.

Reference Voltage (V_{REF})

The reference-voltage source is highly stable with temperature. It can be used if additional, external components are wired.

Monitoring Circuit (I START, I STOP, Q START, Q STOP)

The monitoring circuit guarantees the secure operation of a unit of equipment. Any circuitry that is shut down because of a fault, for instance, cannot be started up again until the monitoring start (I START/Q START) has turned on and a positive voltage pulse has been impressed on Q START.

If there is a defect present, the monitoring stop (I STOP/Q STOP) will turn on and shut down either the entire unit or simply the circuitry that has to be protected. No restart is then possible until the hold current impressed on I START or I STOP has been interrupted (e.g. by a power-down).

Maximum Ratings

Description	Symbol	Notes	min	max	Unit
Supply voltage	V_S	V_Z = Z Voltage	−0.3	V_Z	V
Inputs					
Comporator	$V_{I\ COMP}$		−0.3	33	V
	$V_{-I\ COMP}$		−0.3	33	V
Op Amp	$V_{I\ Op\ Amp}$		−0.3	6	V
	$V_{-I\ Op\ Amp}$		−0.3	6	V
Multiplier	V_{M1}		−0.3	33	V
Output op amp	$V_{Q\ Op\ Amp}/I_{M2}$		−0.3	6	V
Z current V_S GND	I_Z	Observe P_{max}	0	300	mA
Driver output	V_Q		−0.3	V_S	V
Q clamping diodes	$I_{Q\ D}$	$V_Q > V_S$ or $V_Q < -0.3$ V	−10	10	mA
Input START	$V_{I\ START}$	see characteristic	−0.3	25	V
STOP	$V_{I\ STOP}$	see characteristic	−0.3	33	V
Output START	$V_{Q\ START}$		−10	3	V
STOP	$V_{Q\ STOP}$		−0.3	6	V
Detector input	$V_{I\ DET}$		0.9	6	V
Detector clamping diodes	$I_{I\ DET}$	$V_{I\ DET} > 6$ V or $V_{I\ DET} < 0.9$ V	−10	10	mA
Capacitance at I START to ground	$C_{I\ START}$			150	µF
Junction temperature	T_j			125	°C
Storage temperature	T_{stg}		−55	125	°C
Thermal resistance system – air	$R_{th\ SA}$			65	K/W

Operating Range

Supply voltage	V_S	Values for $V_{S\ ON}$, V_Z: see characteristics	$V_{S\ ON}$	V_Z	V
Z current	I_Z	Observe P_{max}	0	200	mA
Driver current	$I_{Q\ D}$		−300	300	mA
Operating temperature	T_A		−25	85	°C

Characteristics ($V_{S\,ON}$[1]) < V_S < V_Z; T_A = −25 °C to +85 °C)

Description	Symbol	min	typ	max	Unit
Current Consumption					
Without load on driver Q and V_{REF}; Q Low					
0 V < V_S < $V_{S\,ON}$	I_S			0.5	mA
$V_{S\,ON}$ < V_S < V_Z	I_S	2.5	5	6.5	mA
Load on QD with SIPMOS gate; dynamic operation 50 kHz V_S = 12 V load on Q = 10 nF	I_S			15	mA
Hysteresis on V_S					
Turn-on threshold for V_S rising	$V_{hy\,H}$	9.6	10.4	11.2	V
Switching hysteresis	$V_{S\,hy}$	1.0		1.7	V
Comparator (COMP)					
Input offset voltage	V_{IO}	−10		10	mV
Input current	$-I_I$			2	µA
Common-mode input voltage range	V_{IC}	0		3.5	V
Operational Amplifier (Op Amp)					
Open-loop voltage gain	G_{V0}	60	80		dB
Input offset voltage	V_{IO}	−30		−10	mV
Input current	$-I_I$			2	µA
Common-mode input voltage range	V_{IC}	0		3.5	V
Output current	$I_{Q\,Op\,Amp}$	−3		1.5	mA
Output voltage	$V_{Q\,Op\,Amp}$	1.2		4	V
Transition frequency	f_T		2		MHz
Transition phase	φ_T		120		deg.

For explanations refer to page 239

Characteristics ($V_{S\,ON}$[1]) $< V_S < V_Z$; $T_A = -25\,°C$ to $+85\,°C$)

Description	Symbol	min	typ	max	Unit
Output driver (QD)					
Output voltage high $I_Q = -10$ mA	V_{QH}	5			V
Output voltage low $I_Q = +10$ mA	V_{QL}			1	V
Output current rising edge $C_L = 10$ nF falling edge $C_L = 10$ nF	$-I_Q$ I_Q	200 250	300 350	400 450	mA mA
Reference-Voltage Source					
Voltage $0 < I_{REF} < 3$ mA	V_{REF}	1.8	2	2.2	V
Load current	$-I_L$	0		3	mA
Voltage change $10\,V < V_S < V_Z$	ΔV_{REF}			5	mV
Voltage change $0\,mA < I_{REF} < 3$ mA	ΔV_{REF}			20	mV
Temperature response	$\Delta V_{REF}/\Delta T$	−0.5		+0.5	mV/K
Z Diode (V_S − GND)					
Z voltage $I_Z = 200$ mA Observe P_{max}	V_Z	13	15.5	17	V
Multiplier (M1)[2])					
Quadrant for input voltages			1		qu.
Input voltage M1	V_{M1}	0		1	V
Reference level for M1	$V_{REF\,M1}$		0		V
Input voltage M2	V_{M2}	V_{REF}		$V_{REF}+1$	V
Reference level for M2	$V_{REF\,M2}$		V_{REF}		V
Input current M1, M2	$-I_I$	0		2	µA
Coefficient for output-voltage source	C_Q	0.4	0.6	0.8	I/V
Temperature response of output-voltage coefficient	$\Delta TC/C_Q$	−0.3	−0.1	0.1	%/K

For explanations refer to page 239

Characteristics ($V_{S\,ON}$[1]) < V_S < V_Z; T_A = −25 °C to +85 °C)

Description	Symbol	min	typ	max	Unit
Monitoring Circuit					
Input I START					
Turn-on voltage	$V_{I\,ON\,START}$	17	22	26	V
Turn-on current	$I_{I\,ON\,START}$	50	90	130	µA
Turn-off voltage	$V_{I\,OFF\,START}$	2	3.5	5	V
Turn-off current	$I_{I\,OFF\,START}$	70	110	150	µA
Input I STOP*)					
Turn-on voltage	$V_{I\,ON\,STOP}$	27	30	33	V
Turn-on current	$I_{I\,ON\,STOP}$	100	150	200	µA
Turn-off voltage	$V_{I\,OFF\,STOP}$	4.5	6.5	8.5	V
Turn-off current	$I_{I\,OFF\,STOP}$	175	250	320	µA
Transfer I START – Q START					
Output current on Q START V_{START} = 15 V; $V_{Q\,START}$ = 2 V	$-I_{Q\,START}$	400	600	800	mA
Transfer I STOP – Q STOP					
Output current on Q STOP I_{STOP} = 1.5 mA; V_{STOP} = 18 V; $V_{Q\,STOP}$ = 1.2 V	$-I_{Q\,STOP}$	0.9	1.2		mA
I_{STOP} = 0.4 mA; V_{STOP} ≈ 7 V; $V_{Q\,STOP}$ = 1.2 V	$-I_{Q\,STOP}$	90	150		µA
Detector (I DET)					
Upper switching voltage for voltage rising (H)	$V_{DET\,H}$	1	1.3	1.6	V
Lower switching voltage for voltage falling (L)	$V_{DET\,L}$	0.95			V
Switching hysteresis	$V_{S\,hy}$	50		300	mV
Input current 0.9 V < V_{DET} < 6 V	$-I_{DET}$		5		µA
Clamping-diode current V_{DET} > 6 V or V_{DET} < 0.9 V	I_{DET}	−3		3	mA

*) The turn-on voltage of I_{STOP} exceeds the turn-on voltage of I_{START} by at least 3 V.
For explanations refer to page 239

Characteristics ($V_{S\,ON}$[1]) $V_S < V_Z$; $T_A = -25\,°C$ to $+85\,°C$)

Description	Symbol	min	typ	max	Unit
Delay Times					
Input comparator → Q[3])	t		200	500	ns

Explanations

[1]) $V_{S\,ON}$ means that V_{SH} has been exceeded but that the voltage is still greater than V_{SL}.

[2]) Calculation of the output voltage V_{QM}: $V_{QM} = C \cdot V_{M1}^* \cdot V_{M2}^*$ in V.
The voltages V_{M1}^* and V_{M2}^* are referred to the particular reference level.

[3]) Step functions at comparator input $\Delta V_{COMP} = -100$ mV ↓→ $\Delta V_{COMP} = +100$ mV.

Use and Advantages of IC TDA 4814 A in SMPS and Electronic Ballasts

1 Switch-Mode Power Supplies

The "active harmonics filter" consists of a rectifier arrangement in a bridge circuit followed by an up-converter. Through a controller action it is possible to draw a virtually sinusoidal current from the single-phase line and produce a regulated dc voltage at the output.

In the case of an SMPS with conventional line rectification it is possible to achieve a power factor (ratio of active power to apparent power) of 0.5 to 0.7. The active harmonics filter serves for improving the power factor, which reaches a value of almost 1, and for reducing the load on the line produced by harmonics. The losses caused by the active harmonics filter are more than compensated by the fact that a subsequent converter can constantly be operated at an optimal operating point because of the input control of the operating voltage.

The extra effort that is necessary, compared to an SMPS without an active harmonics filter, is made good upwards of about 500 W by savings elsewhere (e.g. smaller smoothing capacitance and transistors of a higher resistance in the SMPS). With the wide-ranging power supplies that are in increasing demand, i.e. power supplies that can work on a line of 90 through 240 Vac without any switching changes, the power pay-off limit reduces considerably.

2 Electronic Ballasts for Fluorescent Lamps

The VDE and the EVUs require of **industrial** consumers that they take "sinusoidal current from the line, i.e. exhibit a purely ohmic response. This is the case with incandescent lamps, cooker rings and heating fixtures.

In all electronic devices with rectification and a CR load the current drain is pulsed, i.e. afflicted by a large harmonic content and impermissible according to VDE. The reflected current ripple can interfere with installations for AF power-line carrier control for instance, i.e. lead to faulty switching. Consequently the harmonic content of the current may not exceed certain values.

The line current for a ballast operating with a stable fluorescent lamp must be such that the share of harmonics in relation to the fundamental does not exceed the values given in table 1.

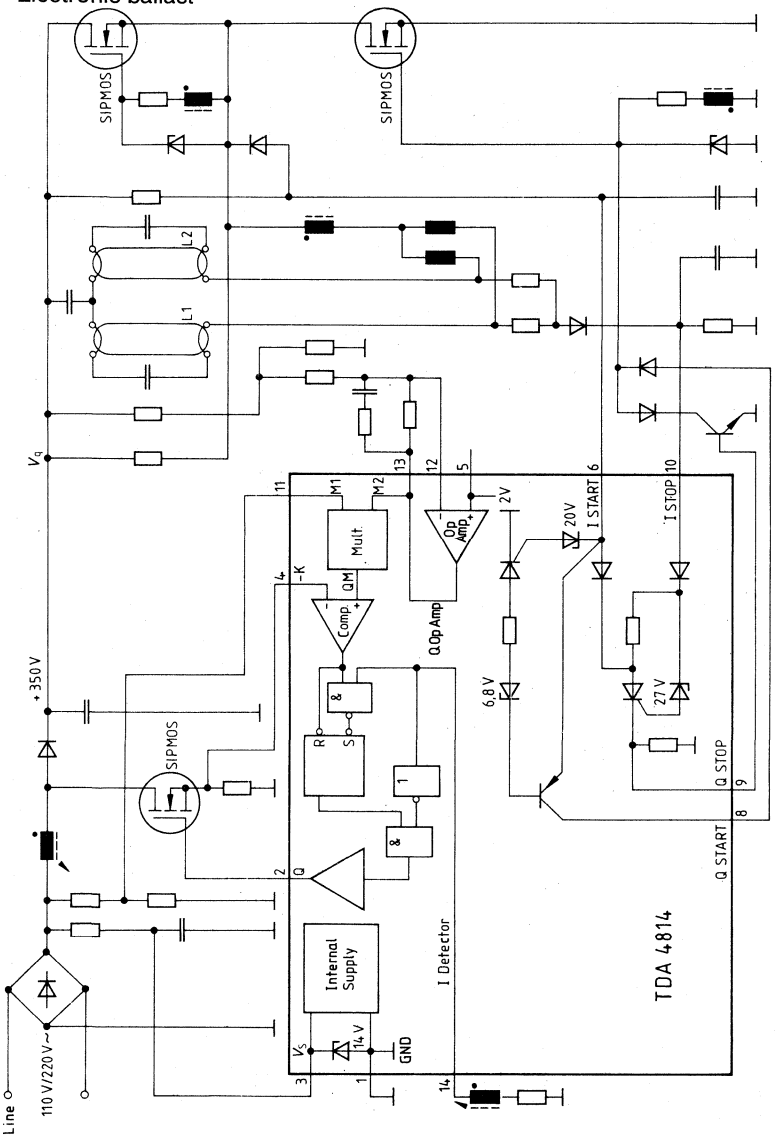
Table 1 Line-Current Harmonic Content in acc. with VDE 0712, Part 2

Harmonics	Permissible harmonic content[1] in %
3rd harmonic	$25 \times \frac{\lambda}{0.9}$
5th harmonic	7
7th harmonic	4
9th harmonic	3
11th harmonic	2
13th harmonic and higher	1

1) λ is the power factor

The values given here are achieved using the TDA 4814 A to drive a SIPMOS in an up-converter regulating circuit.

Application Example
Electronic ballast



Remark
Kindly note that the SIEMENS AG holds patents on electronic ballasts for fluorescent lamps, published in "Siemens Energy and Automation", Vol. II, No. 2, March/April 1985

Type	Ordering Code	Package
TDA 4918 A	Q67000-A8021	P-DIP-20
TDA 4918 G	Q67000-A8142	P-DSO-20-L (SMD)
TDA 4919 A	Q67000-A8143	P-DIP-20
TDA 4919 G	Q67000-A8018	P-DSO-20-L (SMD)

Functional Description

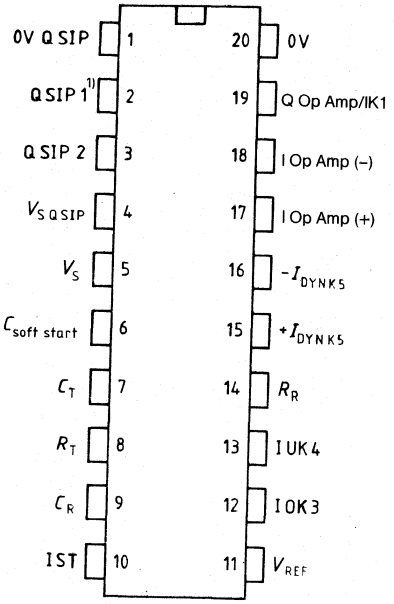
The versatile switch-mode power supply ICs for the direct control of SIPMOS power transistors comprise digital and analog functions. These functions are required for the design of high-quality flyback and forward converters during single-phase and push-pull operation in normal, half-bridge and full-bridge configurations. The ICs can also be used for transformerless voltage multipliers and speed-controlled motors. Malfunctions in the electrical operation of the switch-mode power supply are recognized by on-chip comparators which activate protective functions. The TDA 4918 has two driver outputs for push-pull switch-mode power supplies, as well as single-phase SMPS with a duty cycle limitation of 50%. The TDA 4919 with a driver output is suitable for single-ended SMPS with duty cycles of up to 100% approximately.

Features

- Switching frequency up to 300 kHz (TDA 4919) or 150 kHz (TDA 4918)
- Push-pull output driver with +700 mA/−500 mA
- Separate GND for the driver outputs
- Feed-forward control
- Soft start
- Hysteresis adjustable at overvoltage and undervoltage comparator
- Current-saving starting circuit
- Current mode and voltage mode operation are possible

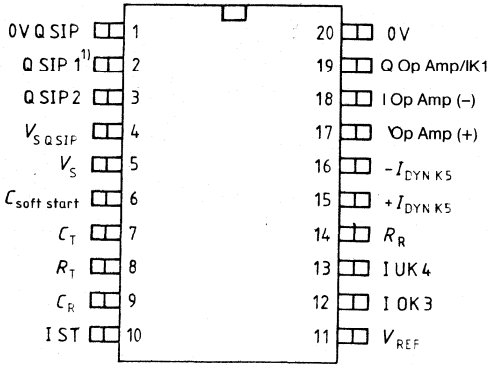
Pin Configurations
(top view)

TDA 4918 A/TDA 4919 A



1) only TDA 4918 A

TDA 4918 G/TDA 4919 G



1) only TDA 4918 G

Pin Description

Pin	Symbol	Function
1	0 V Q SIP	GND driver
2	Q SIP1	SIPMOS driver 1 (only TDA 4918)
3	Q SIP2	SIPMOS driver 2
4	$V_{S\ QSIP}$	Supply voltage driver
5	V_S	Supply voltage
6	$C_{soft\ start}$	Soft start
7	C_T	Frequency generator
8	R_T	Frequency generator
9	C_R	Ramp generator
10	I ST	Input standby
11	V_{REF}	Reference voltage
12	I OK3	Input overvoltage
13	I UK4	Input undervoltage
14	R_R	Ramp generator
15	$+I_{DYN\ K5}$	Dyn. current limitation
16	$-I_{DYN\ K5}$	Dyn. current limitation
17	I Op Amp (+)	Input operational amplifier
18	I Op Amp (−)	Input operational amplifier
19	Q Op Amp /IK1	Output operational amplifier Q Op Amp / input comparator
20	0 V	GND

Circuit Description

The various functional units of the component and their interaction are described in the following.

Supply Voltage V_S

The IC enables the two outputs not before the turn-on threshold ($V_{S\ ON}$) at V_S is exceeded. The duty cycle (active time/disable time) at the enabled outputs can then rise from zero to the value set with K1 in the time specified by the soft start.

An undervoltage at the standby input causes the current consumption I_S to remain at the very low standby current level independent of the voltage V_S.

Voltage Controlled Oscillator (VCO)

The VCO is connected with the capacitor C_T and the resistor R_T. The charge current at C_T flows continuously and is set with resistor R_T. The discharge current is active during the discharge of C_T and is set internally.

In the typical mode of operation the duration of the rising edge is considerably greater than that of the falling edge. During the falling edge the VCO passes a trigger signal to the ramp generator thus discharging the ramp generator capacitance. Additionally, the trigger signal is routed to other parts of the IC.

Ramp generator

The ramp generator is triggered by the VCO and operates at the same frequency as the VCO. The duration of the ramp generator falling edge must be shorter than the VCO fall time. Only then do the ramp generator upper and lower switching levels reach their rated values.

To control the pulse width at the output, the voltage of the ramp generator rising edge is compared with an externally adjustable dc voltage at comparator K1. The slope of the rising edge is adjusted via the current by means of R_R. This provides the possibility of an additional superimposed control of the output duty cycle. This control capability (feed-forward control) permits the compensation of known interference (e.g. input voltage ripple). A superimposed load current control **(current mode control)** however, can also be implemented.

Push-Pull Flipflop (only TDA 4918)

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two SIPMOS driver outputs is enabled at a time.

Comparator K1 (Duty Cycle Control)

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge (minus input) exceeds the lower level of the two plus inputs, the currently active output is disabled via the turn-off flipflop. The "high"-duration of the respectively active output can thus be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Operational Amplifier (Op Amp)

The op amp is a high quality operational amplifier. It can be used in the control circuit to transmit the amplified variations of the voltage to be regulated to the free plus input of comparator K1. A voltage change is thus converted to a duty cycle change.

Turn-off Flipflop

The falling edge of the VCO causes a pulse at the turn-off flipflop set input. It can, however, only be actually set if no reset signal is pending. With the turn-off flipflop set, the outputs are enabled. Upon an error signal from K5 or upon a turn-off signal from K1 the flipflop disables the outputs.

Z Diode

The Z diode limits the voltage at capacitor $C_{\text{soft start}}$ to a maximum of 5 V. The ramp generator voltage can reach 5.5 V. For an appropriate slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value. This can be a possible advantage in flyback converter operation.

Comparator K2

The comparator has its switching threshold at 1.5 V at the plus input, and with its output it sets the error flipflop if the voltage at capacitor $C_{\text{soft start}}$ is below 1.5 V. The error flipflop, however, will only accept the set pulse if no reset pulse (error) is pending. This prevents a restart of the outputs as long as an error signal is pending.

Soft Start

The lower of the two voltages at the K1 plus inputs – compared with the ramp generator voltage – is a measure for the duty cycle at the output. At component turn-on, the voltage at capacitor $C_{\text{soft start}}$ is equal to 0. As long as no error exists, the capacitor will be charged to the maximum value of 5 V with a current of 6 µA.

In the case of an error, $C_{\text{soft start}}$ is discharged with a current of 2 µA. The currently active output, however, is immediately disabled by the error flipflop. Below a charge voltage of 1.5 V, a set signal is pending at the error flipflop and the outputs are enabled if no reset signal is pending at the same time. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually only increased slowly and continuously after the voltage at $C_{\text{soft start}}$ exceeds 1.8 V.

Error Flipflop

Error signals, routed to the error flipflop reset input, cause an immediate disabling of the outputs (low), and after elimination of the error, a restart of the outputs by soft start.

Comparators K3 (Overvoltage), K4 (Undervoltage), V_{REF} Overcurrent, V_S Undervoltage

These are error detectors that on error cause the error flipflop to immediately disable the outputs. After elimination of the error, the duty cycle is raised again using the soft start. Upon overvoltage, a current is impressed at the inputs of K3 and K4, that can be used to enable an adjustable hysteresis or a holding function. The value of the hysteresis is derived from the internal resistance of the external control source and the current impressed internally at the input of K3 or K4. In the undervoltage case, the set current flows at K4 into the component in the technical direction of current flow, with overvoltage at K3 out of the component.

Comparator K5 (Dynamic Current Limiter)

K5 serves to recognize overcurrents at the switching transistors. Both inputs of the comparator are externally accessible. After elimination of the error, the outputs are enabled with the VCO trigger pulse at the turn-off flipflop. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

Standby Input (I ST)

This input switches with voltage and current hysteresis. The voltage levels for switching from standby to active operation can be set with an external voltage divider between V_S – standby input – ground.

In standby mode the component has a much lower current consumption compared to active operation. The outputs are then active low.

Should the component be operated by means of feedback supply from the switch-mode power supply, the starting phase can optimally be dimensioned.

Reference Voltage (V_{REF})

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be used for the external wiring of the op amp, the error comparators, the ramp generator, or other external components. The voltage source is short-circuit proof to ground.

SIPMOS Driver Outputs (Q SIP)

TDA 4918

The two outputs operate in the push-pull mode. They are active high. The duration during which one of the outputs is active, can be varied infinitely. The duration of the falling edge at the frequency generator is equal to the minimum duration during which both outputs are simultaneously low.

TDA 4919

The output is active high. The duration during which the output is active can be varied infinitely. The duration of the falling edge at the frequency generator is equal to the minimum duration during which the output is low (dead time).

The output drivers are designed as a push-pull stage. The output current is internally limited to the specified values.

A 10 kΩ resistor is connected between the output and ground. This resistor holds the SIPMOS transistor reliably disabled during standby operation (undervoltage at I ST).

Output Q SIP is connected with the supply voltage $V_{S\,Q\,SIP}$ and with ground via diodes.

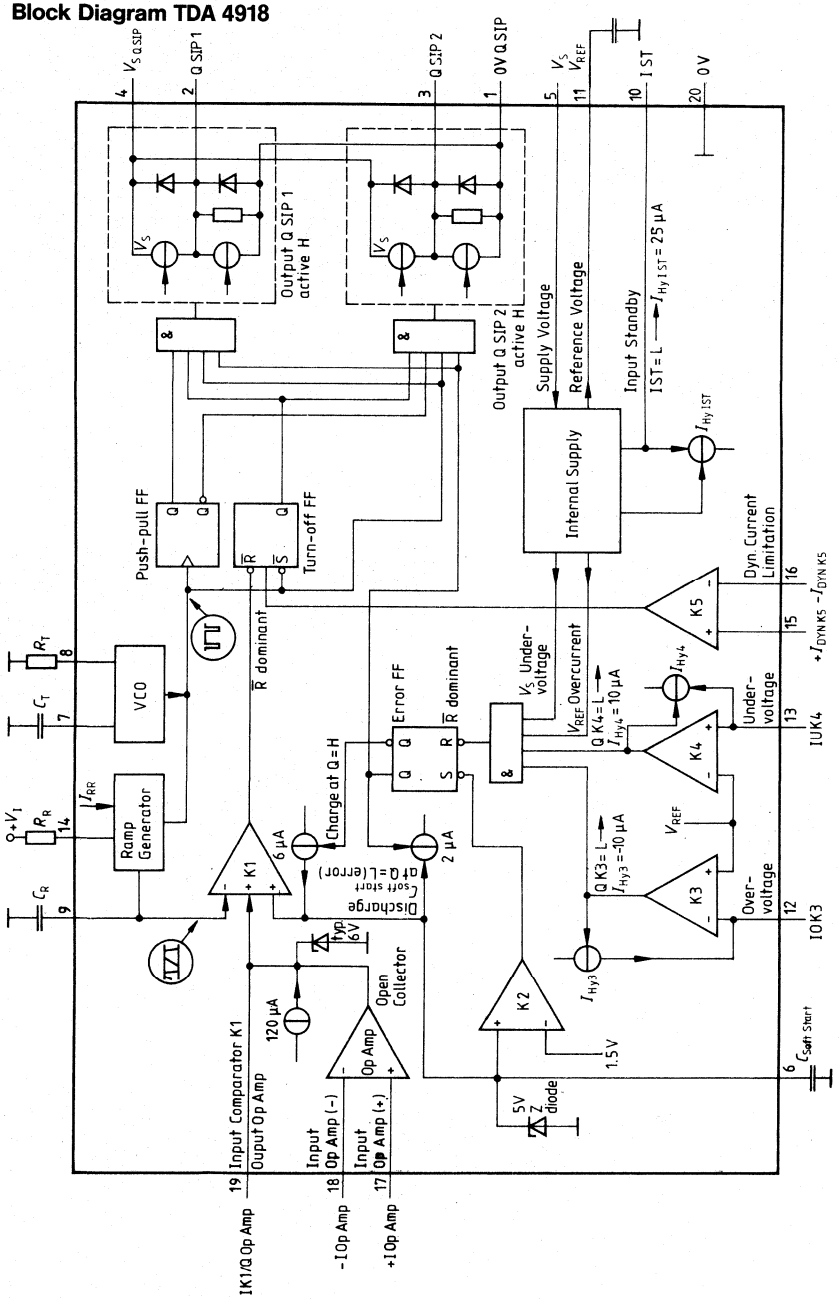
The diode connected to V_S routes the capacitive shift currents from the SIPMOS transistor gate to the filter capacitor at V_S during turning on the SMPS supply voltage. The voltage at V_S can reach approximately 2.3 V without the SIPMOS transistor being turned on.

The diode connected to ground connects negative voltages at Q SIP to −0.7 V. This provides an unimpeded flow off of capacitive currents occurring during voltage breakdown at the SIPMOS transistor drain connection.

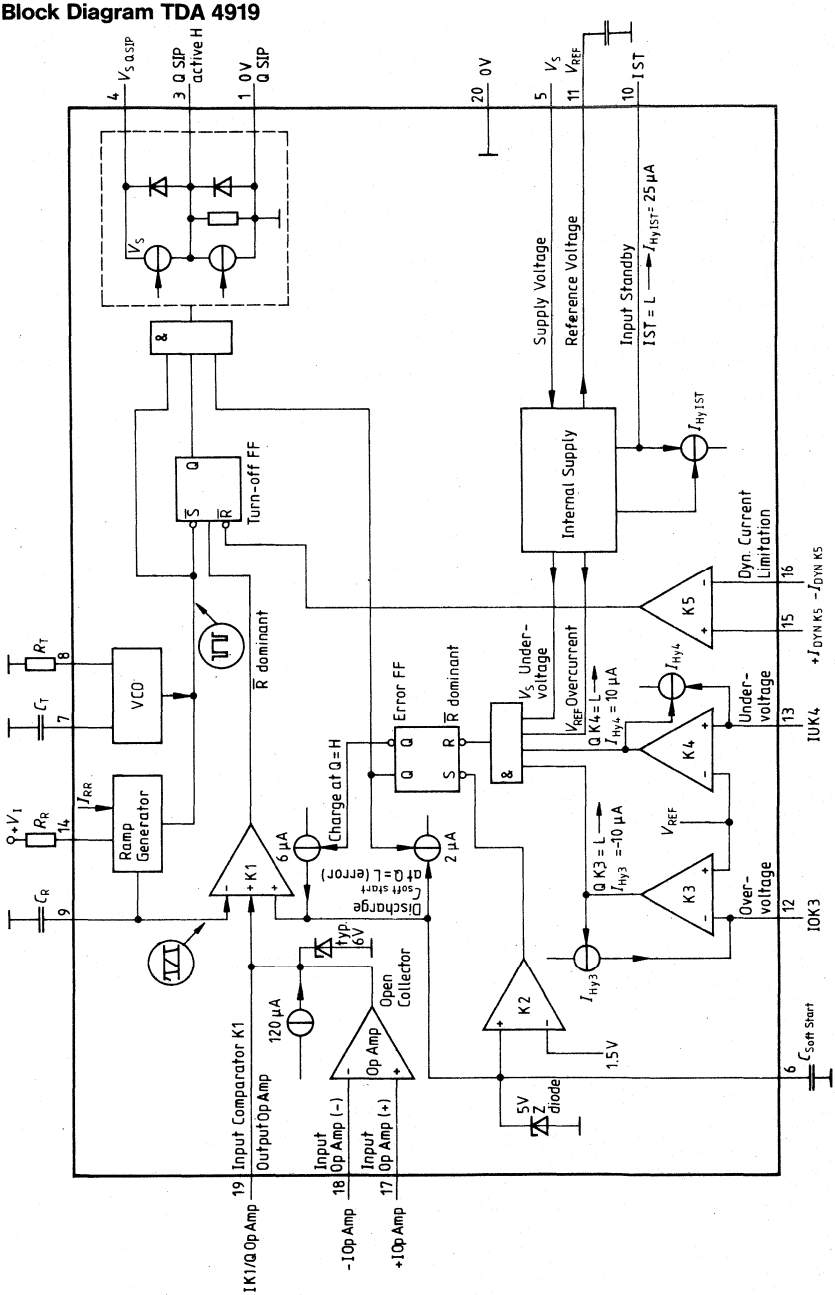
For supply voltages starting at approx. 2 V, both outputs are active low in the disabled state. The function of the diode connected to V_S is then taken over by the pull-down source.

The maximum output voltage is limited by the respectively lowest value of V_S, $V_{S\,Q\,SIP}$ or an internal Z diode. The internal Z diode limits the voltage at Q SIP to typ. 20 V.

Block Diagram TDA 4918



Block Diagram TDA 4919



Maximum Ratings

$T_A = -40$ to $+85$ °C

Description	Symbol	min	max	Unit
Supply voltage	$V_{S\,QSIP}$, V_S	−0.3	33	V
Inputs Op Amp, K3, K5, I ST	V_I	−0.3	33	V
Input K4	V_I	−0.3	V_S	V
Frequency generator (VCO)				
Voltage at R_T; C_T	V_{CT}, V_{RT}	−0.3	6	V
Current at C_T	I_{CT}		3	mA
$V_{CT} > 6$ V				
Ramp generator				
C_R input	V_{CR}	−0.3	6	V
R_R input	I_{RR}	0	3	mA
Reference voltage	V_{REF}	−0.3	6	V
Output Op Amp	$V_{Q\,op\,amp}$	−0.3	6	V
$V_{Q\,op\,amp} > 6$ V	$I_{Q\,op\,amp}$		2	mA
Driver output Q SIP[1]	$V_{Q\,SIP}$	−0.3	V_S	V
Q SIP clamp diodes	$I_{Q\,SIP}$	−100	100	mA
$V_{Q\,SIP} > V_S$ or $V_{Q\,SIP} < -0.3$ V				
Soft start	$V_{C\,soft\,start}$	−0.3	6	V
$V_{C\,soft\,start} > 6$ V	$I_{C\,soft\,start}$	0	100	µA
Junction temperature[2]	T_j		125	°C
Storage temperature	T_{stg}	−65	125	°C
Thermal resistance				
system – air P-DIP-20	$R_{th\,SA}$		60	K/W
P-DSO-20	$R_{th\,SA}$		90	K/W

Operating Range

Supply voltage	V_S	$V_{S\,ON}$[3]	30	V
	$V_{S\,Q\,SIP}$		30	V
Frequency generator (VCO)	f_{VCO}		300	kHz
Ramp generator	f_R		300	kHz
Ambient temperature	T_A	−40	85	°C
Ground QSIP		GND 0 V −0.3	GND 0 V +0.5	V

The characteristics refer to both the pins connected to ground.

1) With this, the max. power dissipation or junction temperature must be taken into account!
2) At a planned max. operating time of 70000 hours a continuous max. junction temperature of 150 °C is permitted.
3) For $V_{S\,ON}$ values refer to characteristic data.

Characteristics

$V_{S\,ON} < V_S < 30$ V[1]), $T_A = -40$ to $+85$ °C

Description	Symbol	Test conditions	min	typ	max	Unit
Current consumption without load at V_{REF} Q op amp, Q SIP 1/2	I_S	$C_T = 1$ nF frequency generator with 100 kHz outputs active			18	mA
Standby operation	I_{ST}	$V_S = 20$ V			3.5	mA
Hysteresis at V_S						
Turn-on threshold for V_S rising	$V_{S\,H}$	$V_{I\,ST} \geq V_{IST\,H}$			9.6	V
Turn-off threshold for V_S falling	$V_{S\,L}$		7.8			V
Reference						
Voltage	V_{REF}	$I_{REF} = 1$ mA $T_A = 25$ °C $V_S = 15$ V	2.475	2.5	2.525	V
Load current	$-I_{REF}$		0		3	mA
Voltage change	ΔV_{REF}	$I_{REF} = 1$ mA ± 20%			10	mV
Voltage change	ΔV_{REF}	$V_S = 15$ V ± 20%			3	mV
Temperature response	$\Delta V_{REF}/\Delta T$		−0.3		0.3	mV/K
Response threshold for V_{REF} overcurrent	$-I_{REF\,O}$		4	7	10	mA
Frequency generator (VCO)						
Frequency range	f_{VCO}				300	kHz
Frequency change	$\Delta f/f_{VCO}$	$V_S = 15$ V ± 20%			1	%
Tolerance	$\Delta f/f_{VCO}$	$C_T = 1$ nF $f_{VCO} = 100$ kHz; $T_A = 25$ °C	−7		7	%
Charge current for C_T (perm.) = current at pin R_T	$-I_{RT}$	$I_{RT} = V_{REF/RT}$	0		1	mA
Discharge current for C_T	I_{dch}	internally fixed		2		mA
C_T range			0.47		10	nF[2)]
Dead time	τ_t	$C_T = 470$ pF, $f_{VCO} = 100$ kHz		350	450	ns
		$C_T = 470$ pF, $f_{VCO} = 300$ kHz		400	500	ns[2)]

[1)] $V_{S\,ON}$ means that $V_{S\,HIGH}$ has been exceeded, while $V_{S\,LOW}$ has not yet been undercut.

[2)] The time of the falling edge (fall time) is proportional to C_T, if the discharge current largely exceeds the charge current. The fall time is proportional to the minimum dead time at the outputs.

Characteristics

$V_{S\,ON} < V_S < 30$ V[1]), $T_A = -40$ to $+85$ °C

Description	Symbol	Test conditions	min	typ	max	Unit
Ramp generator						
Frequency range	f_R				300	kHz
Maximum voltage at C_R Minimum voltage at C_R	$V_{CR\,H}$ $V_{CR\,L}$		5.4 1.65	6.1 1.8	6.7 1.95	V V
Charge current for C_R (perm) = current at pin R_R Discharge current for C_R	I_{ch} I_{dch}	V_{RR} approx. 0.7 V internally fixed	0 1.3	 2	1 2.7	mA mA
Ratio $I_{RR}/I_{CR\,charge}$		$I_{RR} = 0.5$ mA	0.95		1.1	
Capacitance	C_R		100			pF
Comparator K1						
Input current	$-I_{K1}$				2	µA
Common-mode input voltage range	V_{IC}		0		$V_{CR\,H}$	V
Turn-off delay time	t	Rated load 3 nF at Q SIP			500	ns[2])
Operational amplifier						
Open-loop voltage gain	G_{V0}		60	80		dB
Input offset voltage	V_{IO}	Pin 19 n.c.	−10		10	mV
Input current	$-I_{I\,op\,amp}$				2	µA
Common-mode input voltage range	V_{IC}		0		4	V
Output current	$I_{Q\,op\,amp}$		0		2	mA
Output voltage range	V_Q	0 mA $< I_Q <$ 2 mA	0.5		$V_{CR\,H}$	V
Transition frequency Transition phase	f_T Φ_T			3 120		MHz deg.
Temperature coefficient of V_{IO}	TC	Pin 19 n.c.; $V_{IC} = 3$ V	−30		+30	µV/K
Source current at Q Op Amp	$I_{op\,amp}$	0.5 V $< V_Q < V_{CR\,H}$	70	100	130	µA

[1]) $V_{S\,ON}$ means that $V_{S\,HIGH}$ has been exceeded, while $V_{S\,LOW}$ has not yet been undercut.

[2]) Step function $V_{REF} = -100$ mV → $V_{REF} = +100$ mV (for transit time from input comparator to Q SIP

Characteristics

$V_{S\,ON} < V_S < 30$ V[1]), $T_A = -40$ to $+85$ °C

Description	Symbol	Test conditions	min	typ	max	Unit
Soft start						
Charge current for $C_{soft\ start}$	$-I_{ch}$		4	6	8	µA
Discharge current for $C_{soft\ start}$	I_{dch}		1	2	3.2	µA
Upper limiting voltage	V_{lim}		4.4	4.8	5.0	V
Switching voltage of K2	V_{K2}		1.3	1.5	1.7	V
Dynamic current limitation K5						
Input current	$-I_{I\,DYN}$				2	µA
Input offset voltage	V_{IO}		−10		10	mV
Common-mode input voltage range	V_{IC}		0		V_S-3	V
Turn-off delay time	t	Rated load 3 nF at QSIP		250	400	ns[2])
Undervoltage K4						
Input current at K4	$-I_{I\,K4}$				0.2	µA
Switching voltage at K4	V_{sw}		V_{REF} −0.01		V_{REF} +0.01	V
Hysteresis current	$I_{Hy\,4\,H}$	$V_{(+\,K4)} < V_{sw}$	11	18	22	µA
	$I_{Hy\,4\,L}$	$V_{(+\,K4)} > V_{sw}$			0.1	µA
Turn-off delay time	t				3	µs[2])
Overvoltage K3						
Input current	$-I_{I\,K3}$				0.2	µA
Switching voltage	V_{sw}		V_{REF} −0.01		V_{REF} +0.01	V
Turn-off delay time	t				3	µs[2])
Hysteresis current	$-I_{Hy\,4\,H}$	$V_{(-\,K3)} > V_{sw}$	6	9	12	µA
	$-I_{Hy\,4\,L}$	$V_{(-\,K3)} < V_{sw}$			0.1	µA

[1]) $V_{S\,ON}$ means that $V_{S\,HIGH}$ has been exceeded, while $V_{S\,LOW}$ has not yet been undercut.

[2]) Step function $V_{REF} = -100$ mV ⤳ $V_{REF} = +100$ mV (for transit time from input comparator to Q SIP)

Characteristics

$V_{S\,ON} < V_S < 30$ V[1]), $T_A = -40$ to $+85$ °C

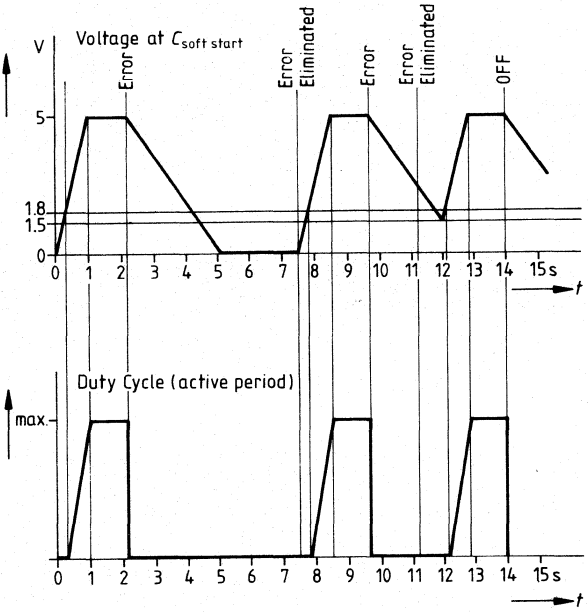
Description	Symbol	Test conditions	min	typ	max	Unit
Output driver QSIP 1/2						
Output voltage high	V_{QH}	$I_{Q\,SIP} = -250$ mA; $V_S = V_{SQSIP}$	$V_S - 3$			V
Output voltage low	V_{QL}	$I_{Q\,SIP} = +250$ mA; $V_S = V_{SQSIP}$			2.1	V
	V_{QL}	$I_{Q\,SIP} = +10$ mA; $V_S = V_{SQSIP}$			1.4	V
Output current	$I_{Q\,SIP}$	$C_{Q\,SIP} = 10$ nF; $V_S = V_{S\,Q\,SIP} = 20$ V	500	700		mA[2])
	$-I_{Q\,SIP}$		300	500		mA[2])
	$I_{Q\,SIP}$	$C_{Q\,SIP} = 10$ nF; $V_S = V_{S\,Q\,SIP} = 15$ V		600		mA[2])
	$-I_{Q\,SIP}$			500		mA[2])
	$I_{Q\,SIP}$	$C_{Q\,SIP} = 10$ nF; $V_S = V_{S\,Q\,SIP} = 10$ V		400		mA[2])
	$-I_{Q\,SIP}$			400		mA[2])
Input standby IST						
Turn-on threshold for $V_{I\,ST}$ rising	$V_{I\,ST\,H}$	$V_S > V_{S\,ON}$; $T_A = 25$ °C	6.1	6.8	7.5	V
Temperature response	$\Delta V_{ISTH}/\Delta T$			−0.023		%/K
Turn-off threshold for $V_{I\,ST}$ falling	$V_{I\,ST\,H}$		5.5	6.1	6.7	V
Temperature response	$\Delta V_{ISTL}/\Delta T$			+0.047		%/K
Hysteresis current	$-I_{Hy\,IST\,H}$	$V_{IST} > V_{IST\,H}$			2	µA
	$I_{Hy\,IST\,L}$	$V_{ISL} \leq V_{IST} \leq V_{ISTH}$; $T_A = 25$ °C	35	50	65	µA
Temperature response	$\Delta I_{Hy\,ISTL}/\Delta T$			+0.01		%/K

[1]) $V_{S\,ON}$ means that $V_{S\,HIGH}$ has been exceeded, while $V_{S\,LOW}$ has not yet been undercut.

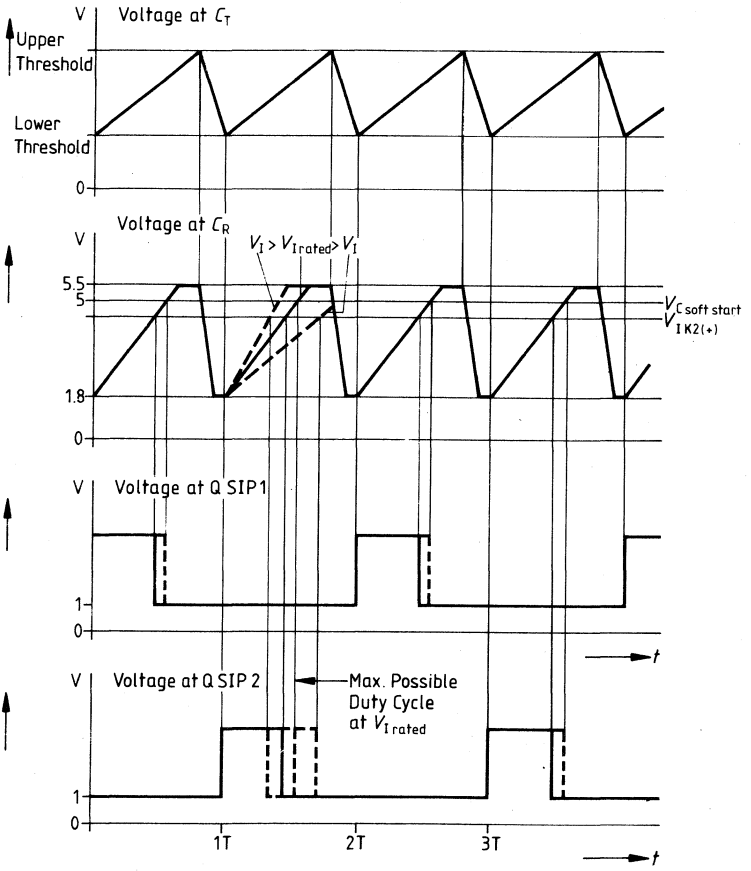
[2]) Dynamic maximum current during rising or falling edge

Pulse Diagram

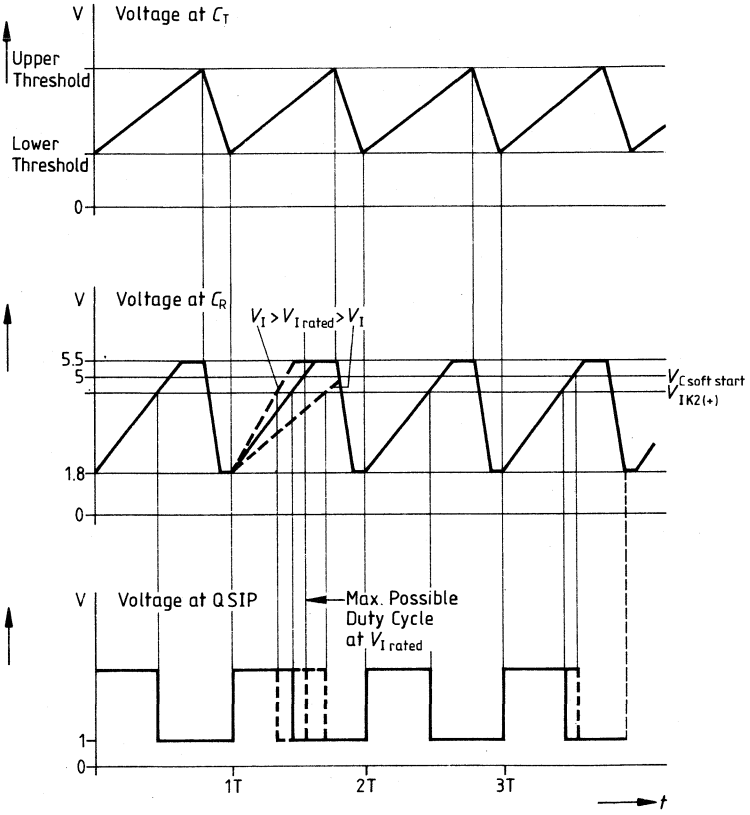
Soft Start/Error/ON-OFF



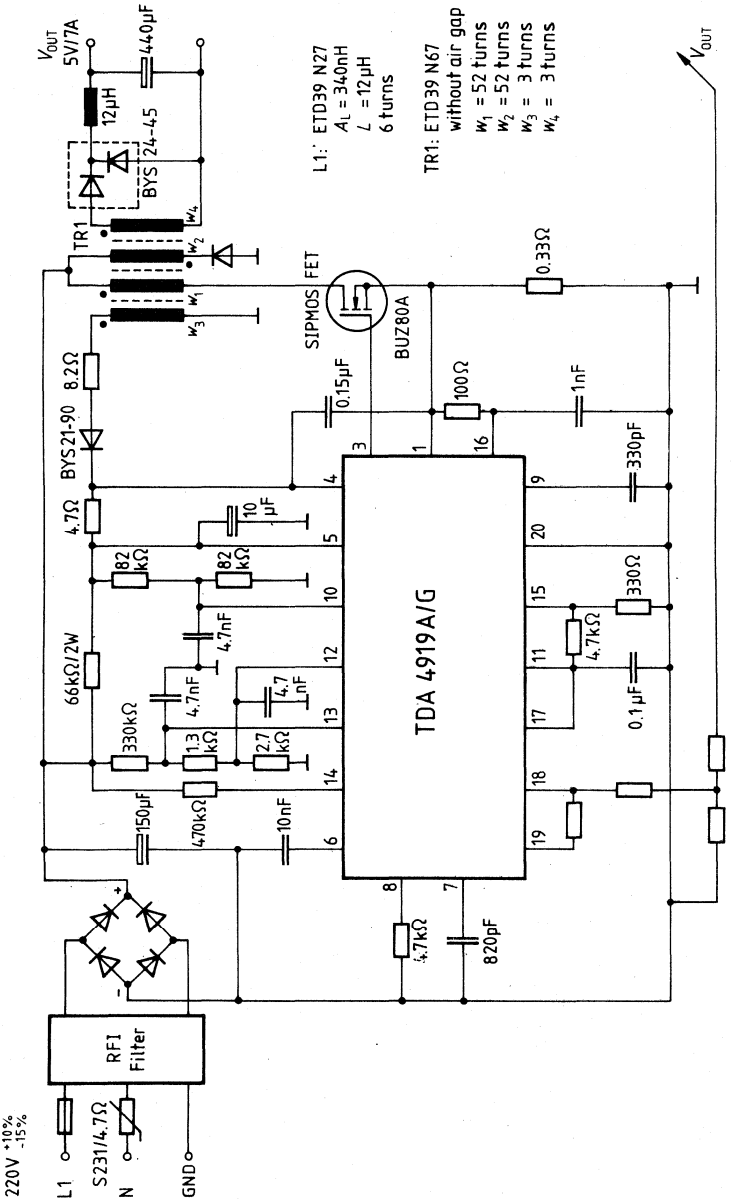
Pulse Diagram TDA 4918



Pulse Diagram TDA 4919



Application Circuit



Preliminary Data **Bipolar IC**

Type	Ordering Code	Package
TLE 4258	Q67000-A8238	P-T66-7-H (similar to TO-220)

The TLE 4258 is a very-low-drop voltage controller which provides two controlled 5-V output voltages. The main controller can be loaded with 750 mA and is turned on and off by pin 5 (pin 5 unconnected = main controller off). In addition, the main controller incorporates a short-circuit current limitation and is turned off in case of overvoltage ($V_I > V_{I\ OFF}$). The standby controller can be loaded with 40 mA, it does not incorporate a short-circuit current limitation and remains permanently active at positive input voltage independently of the turn-off functions of the main controller.

If the main controller output voltage is less than 4.5 V, the reset output is switched to low without delay. As soon as the reset threshold has been exceeded, a delay time to be set by an external capacitor expires and afterwards the reset output switches to high again.

If the lines to the controller are long, the oscillating circuit of line inductance and input capacitance C_I can be attenuated by a resistor $\leq 1\ \Omega$ connected in series to C_I.

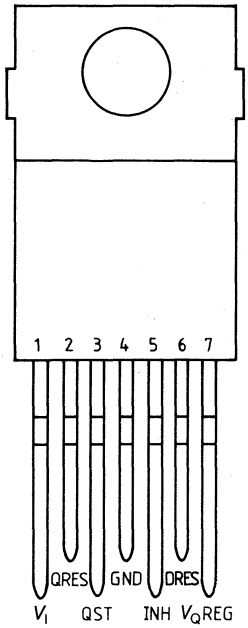
Features

- Low-drop controller
- Low quiescent current
- Reset output
- Protection against reverse polarity
- Overvoltage protection 70 V
- Short-circuit proof
- Suited for automotive electronics
- Inhibit input
- Wide temperature range

Circuit Description

The TLE 4258 incorporates a main and standby-control amplifier. Both the amplifiers regulate the output voltage by comparing the output voltage (from the voltage divider) with a highly precise reference voltage. The standby controller directly controls the base of a PNP series transistor and the main controller via a buffer that can be turned off with inhibit pulse at pin 5. If the output voltage V_Q at pin 7 drops below 4.5 V, a reset signal is released which can only be disabled after a delay time to be set at pin 6. The main output is current-limited and remains active up to the input voltage $V_{I\ OFF}$.

Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	V_I	**Input** of voltage controller
2	Q RES	**Reset output;** open-collector output NPN to pin 4. If the output voltage V_Q drops below the reset threshold, the output stage becomes conductive.
3	Q ST	**Standby output,** connect with a capacitor ≥ 10 µF
4	GND	**Ground;** reference potential
5	INH	**Inhibit (main controller on/off),** control input for turning on/off main controller, connected with a 22-kΩ series resistor. With open input, the main controller remains turned off.
6	D RES	**Reset delay;** pin for reset capacitor; the size of this capacitor determines the delay time of the reset signal typ. 175 ms/µF.
7	V_Q REG	**Main controller output,** connect with a capacitor ≥ 22 µF.

Maximum Ratings

$T_A = -40$ °C to +150 °C

Description	Symbol	min	max	Unit
Input (Pin 1)				
Supply voltage	V_I	−15	+36	V
Polarity reversal with test pulse $t_2 \leq 100$ ms see test circuit	V_I	−70		V
Load-dump with pulse shape $t_2 \leq 400$ ms see test circuit	V_I		70	V
Slew rate 0 V ≤ V_I ≤ 24 V	SR		100	V/µs
Slew rate 24 V ≤ V_I ≤ 70 V	SR		10	V/µs
Current	I_I		2.5	A
Reset Output (Pin 2)				
Voltage	V_R		8	V
Current	I_R		10	mA
Standby Output (Pin 3)				
Voltage	V_{ST}		6	V
Current	I_{ST}		50	mA
Ground (Pin 4)				
Current	I_{GND}		1.8	A
Inhibit (main controller on/off), (Pin 5) Current	I_{INH}		±7.5	mA
Reset delay (Pin 6) Voltage	V_C		V_Q	V
Main controller output (Pin 7) Voltage $V_I \geq V_Q$	V_Q		18	V
Current	I_Q		1.8	A
Temperature				
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−50	150	°C
Operating Range				
Input voltage	V_I	6	24	V
Junction temperature	T_j	−40	150	°C
Thermal resistance system – air system – case	 $R_{th\ SA}$ $R_{th\ SC}$		 65 4	 K/W K/W

Characteristics

$V_I = 13.5$ V; $T_A = 25$ °C; $V_5 > 3.5$ V (unless otherwise specified)

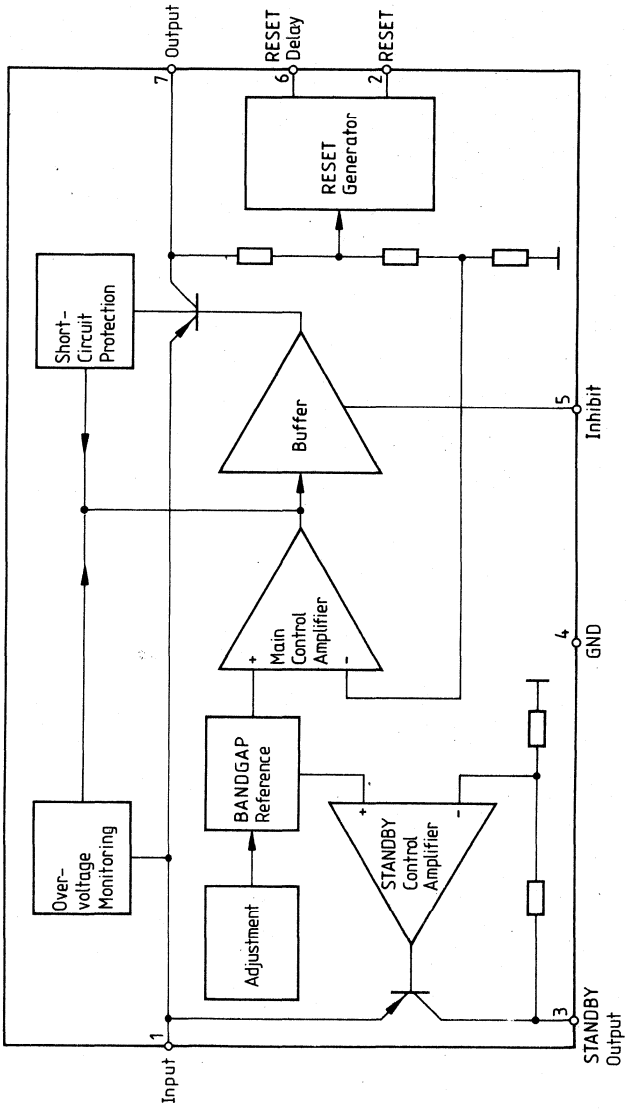
Description	Symbol	Test conditions	Test circuit	min	typ	max	Unit
Main Controller							
Output voltage	V_Q	$0\ mA \le I_Q \le 750\ mA$ $6\ V < V_I < V_{I\,off}$ $-40\,°C \le T_j \le 125\,°C$	1	4.85		5.15	V
Input current	I_Q	$I_Q = 0$ mA; $I_{ST} = 0$ mA	1			30	mA
Current consumption without load	I_Q	$I_Q = 450$ mA; $I_{ST} = 0$ mA	1			150	mA
Current consumption without load	I_Q	$I_Q = 750$ mA; $I_{ST} = 0$ mA	1			300	mA
Current consumption without load	I_Q	$V_I = 5.8$ V; $I_Q = 750$ mA; $I_{ST} = 0$ mA	1			300	mA
Turn-off voltage	$V_{I\,off}$	$V_I > V_{I\,off}$	1	25			V
Output current	I_Q	$V_I > V_{I\,off}$	1			20	mA
Short-circuit current	I_{SC}	$V_Q = 0$ V; $6\ V \le V_I < 13.5$ V	1	0.75	1	1.8	A
Drop voltage	V_{Dr}	$V_I = 4.5$ V; $I_Q = 450$ mA	1		0.3	0.5	V
Drop voltage	V_{Dr}	$V_I = 4.5$ V; $I_Q = 750$ mA	1		0.5	0.75	V
Static load regulation	$\Delta V_Q/\Delta I_Q$	$6\ V \le V_I \le 16$ V $0\ mA \le -I_Q \le 750\ mA$	1			0.2	Ω
Dynamic load regulation	ΔV_Q	$I_Q = 75$ mA of $I_Q = 750$ mA $C_Q \ge 50\ \mu F$	1			100	mV
Supply voltage-rejection	α_{SVR}	$I_Q = 750$ mA; $V_I = 12\ V + 1\ V \cdot \cos(2\pi \times 120\ Hz \cdot t)$; $\alpha_{SVR} = 20 \log (1\ V/\Delta V_Q)$	1	60			dB
Reverse output current	$-I_{QR}$	$V_I = 0$; $0\ V \le V_Q \le 4.85$ V	1		5	30	mA
Temperature drift of output voltage	α_{VQ}	$6\ V \le V_I \le V_{I\,off}$ $\Delta T_j > 50$ K	1	−0.5		0.5	mV/K
Reset Generator							
Switching threshold	V_{RT}		1	4.4	4.5	4.6	V
Switching voltage	V_R	$V_Q < V_{RT}$; $I_R = 10$ mA	1			0.8	V
Switching voltage	V_R	$V_Q > V_{RT}$	1	4.4		V_Q	V
Reverse current	I_R	$V_R > 4.6$ V;	1			5	µA
Charge current	I_{ch}	$0.5\ V < V_{Cd} < (0.75 \cdot V_Q)$	1	10		30	µA
Reset delay time	t_D/C_D		1		175		ms/µF
Switching voltage	V_R	$V_I \ge 3.75$ V; $I_R = 10$ mA $3.5\ V \le V_Q \le V_{RT}$	1 1			0.8	V

Characteristics

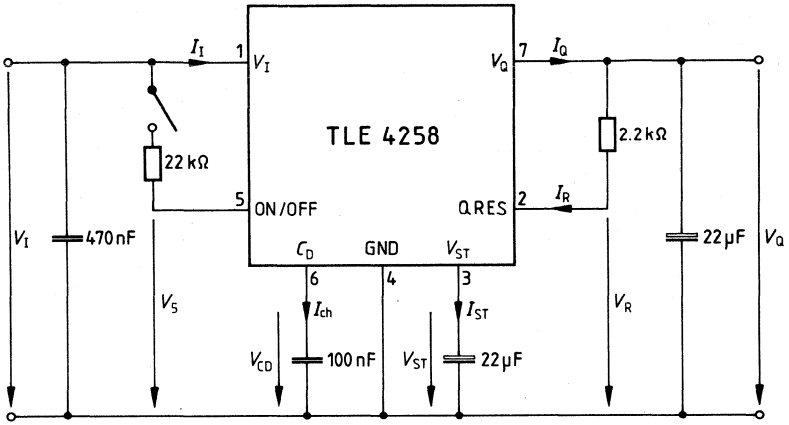
$V_I = 13.5$ V; $T_A = 25$ °C; $V_5 > 3.5$ V (unless otherwise specified)

Description	Symbol	Test conditions	Test circuit	min	typ	max	Unit
Standby Controller		$V_5 \leq 0.5$ V					
Output voltage	V_{ST}	$0\ mA \leq I_{ST} \leq 35\ mA$ $6\ V \leq V_I \leq V_{I\ off}$	1	4.7		5.3	V
Output voltage	V_{ST}	$0\ mA \leq I_{ST} \leq 35\ mA$ $V_{I\ off} \leq V_I \leq 70$ V; $t_2 \leq 400$ ms	1	4.5		6.0	V
Current consumption without load	I_{QST}	$I_Q = 0$ mA; $I_{ST} = 0$ mA	1			2	mA
Current consumption without load	I_{QST}	$I_Q = 0$ mA; $I_{ST} = 35$ mA	1			15	mA
Drop voltage	V_{DrST}	$V_I = 4.5$ V; $I_{ST} = 35$ mA	1			0.75	V
Static load regulation	$\Delta V_{ST}/\Delta I_{ST}$	$6\ V \leq V_I < V_{I\ off}$ $0\ mA \leq I_{ST} \leq 35\ mA$	1		1		Ω
Supply voltage rejection	$\alpha_{SVR\ ST}$	$I_{ST} = 35$ mA; $V_I = 12$ V + 1 V · cos (2 x 120 Hz · t)	1	60			dB
Reverse current	$-I_{ST}$	$V_I = 0$ V; $0\ V \leq V_{ST} \leq 4.7$ V	1			2	mA
General Ratings							
Reverse polarity	$-V_Q$	$V_I = -15$ V	1		0	0.7	V
Reverse polarity	$-I_Q$	$V_I = -15$ V	1		0	0.5	mA
Reverse polarity	$-V_{ST}$	$V_I = -15$ V	1		0	0.7	V
Reverse polarity	$-I_{ST}$	$V_I = -15$ V	1		0	0.5	mA
Synchronous operation V_{ST}; V_Q	$V_{ST}-V_Q$	$0\ mA \leq I_{ST} \leq 35\ mA$ $0\ mA \leq I_Q \leq 750\ mA$ $6\ V \leq V_I < V_{I\ off}$	1	-200		200	mV
Necessary series resistance	R_5		1	12	22	24	kΩ
Switching threshold for main controller	V_5	$V_Q > 3$ V; $I_Q = 0.5$ A	1	3.5			V
Switching threshold for main controller	V_5	$V_Q < 3$ V; $I_Q = 1$ mA	1			0.5	V
Load impedance	R_Q	$Z_Q = R + (j\omega C)^{-1}$	1		0	2	Ω

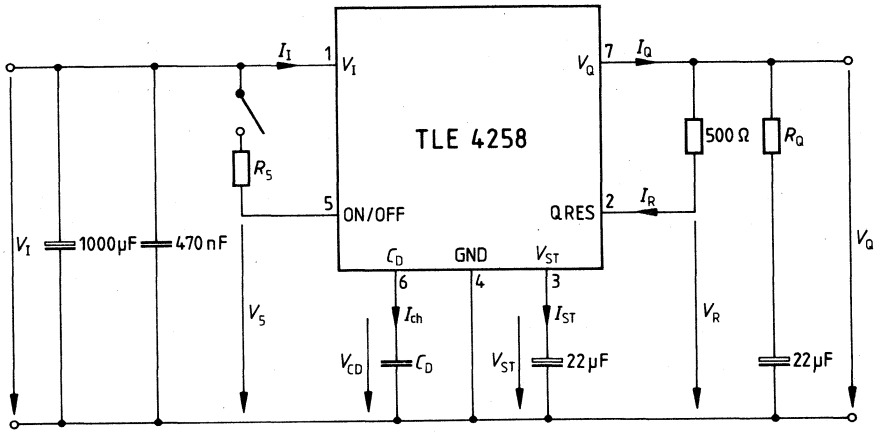
Block Diagram



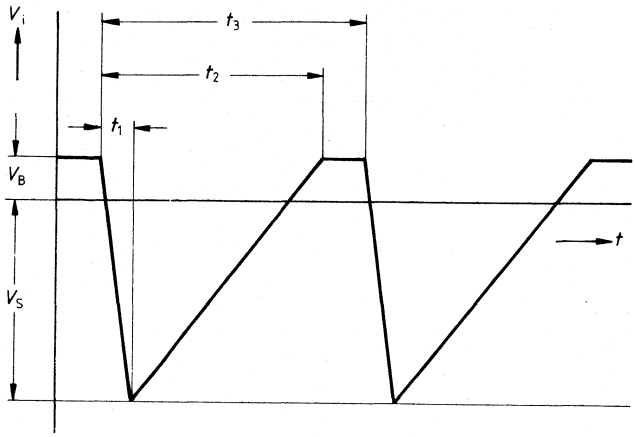
Application Circuit



Measurement Circuit

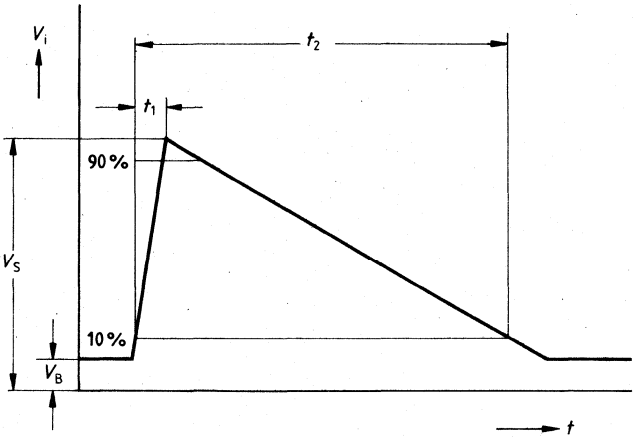


1. Test pulse for negative interference voltages V_i



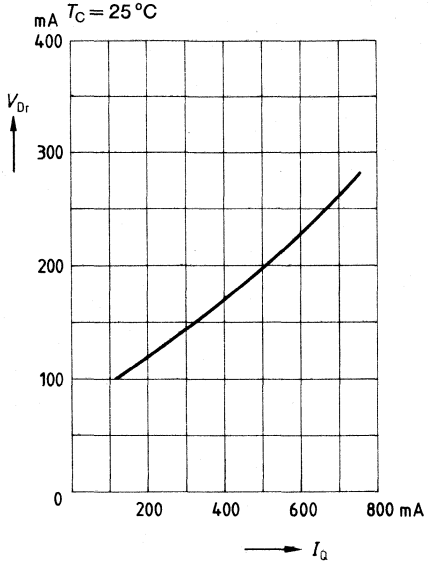
V_B = 14 V t_1 = 10 µs
$|V_S|$ = 70 V t_2 = 2 ms
R_i = 10 Ω t_3 = 0.5 s to 5 s

2. Pulse for load dump at V_{14}

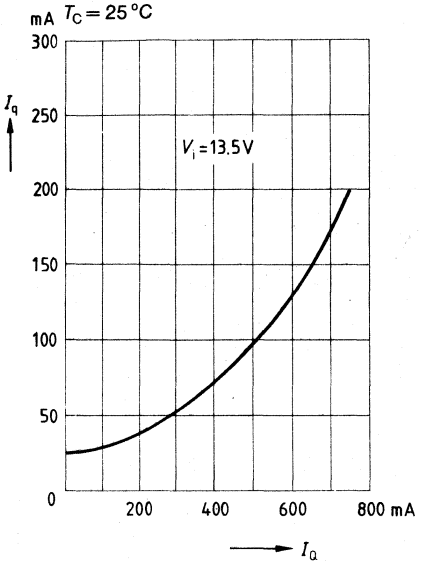


V_B = 14 V t_1 = 5 ms
V_S = 70 V t_2 = 400 ms
R_i = 0.5 Ω

Minimum drop voltage versus output current

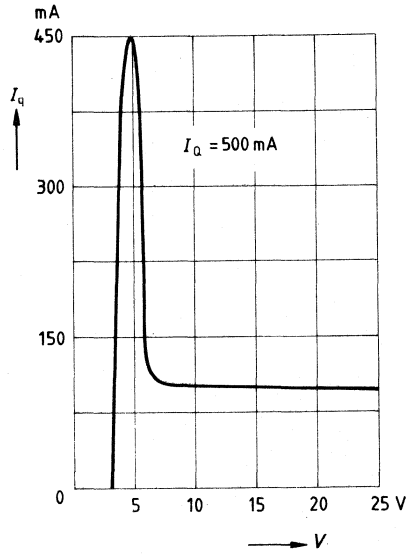


Current consumption without load versus output current

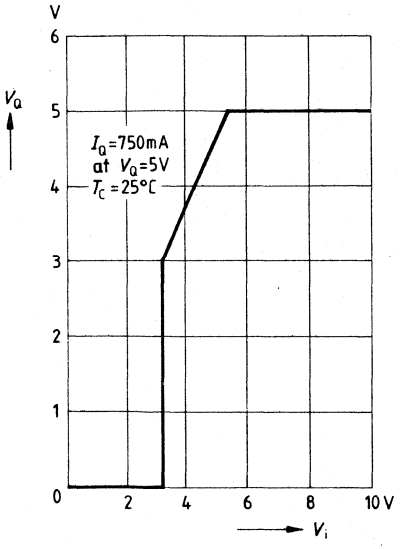


Current consumption without load versus input voltage

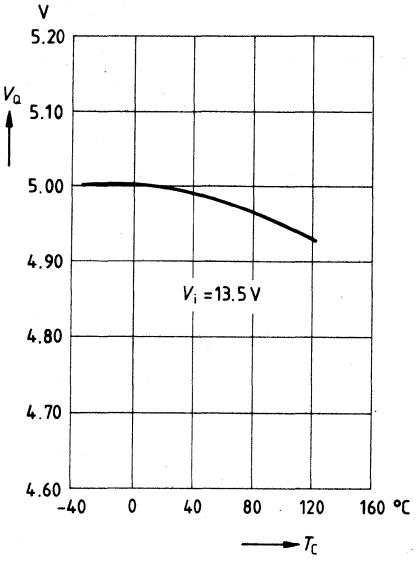
$T_C = 25\,°C$



Output voltage versus input voltage

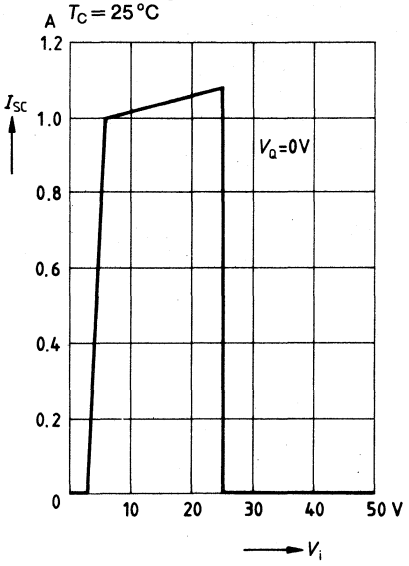


Output voltage versus temperature



Short-circuit current versus input voltage

$T_C = 25\,°C$



Preliminary Data **Bipolar IC**

Type	Ordering Code	Package
TLE 4260	Q67000-A8187	P-T66-5-H (similar to TO-220)

The TLE 4260 is a 5-V low-drop fixed voltage controller in a P-T66-5-H package. The maximum input voltage is 40 V. The IC can provide an output current greater than 500 mA. In addition, it is short-circuit proof and incorporates a temperature protection which interrupts the circuit at unpermissibly high temperatures.

Due to the wide temperature range of $T_A = -40\,°C$ to $+150\,°C$, the TLE 4260 is also suitable for use in automotive electronics.

Features

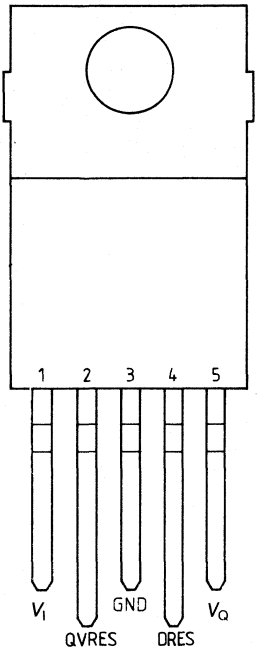
- Low drop controller
- Very low quiescent current
- Low starting current consumption
- Integrated temperature protection
- Protection against reverse polarity
- Input voltage up to 40 V
- Overvoltage protection up to 65 V
- Short-circuit proof
- Suited for automotive electronics
- Wide temperature range

Functional Description

The IC controls an input voltage V_I in the range of $6 < V_I < 40$ V to $V_{Qrated} = 5.0$ V. A reset signal is generated at an output voltage of $V_Q < 4.75$ V. The reset delay time can be set with an external capacitor. If the output current is reduced below 10 mA, the controller internally switches to standby and the reset generator is switched off. The standby current decreases to max. 600 µA.

The control amplifier compares a highly precise reference voltage with a voltage proportional to the output voltage, and controls the base of the series transistor via a buffer. A load current dependent saturation control prevents an oversaturation of the power unit. If the output voltage drops below 95.5% of its typical value, the reset generator discharges an external capacitor at pin 4. If the voltage at the capacitor reaches the lower threshold V_{ST}, it releases a reset signal at pin 2, which will only be disabled after exceeding the upper threshold V_{DT}. With an output current lower than $I_{QN\ OFF} = 10$ mA standby changeover turns the reset generator off. The reset generator is turned on again when the output current starts to rise, when the output voltage drops below 4.2 V or when the delay capacitor is discharged externally. The IC is protected against destruction by limiting the power. In the case of overvoltage or overtemperature the IC is turned off.

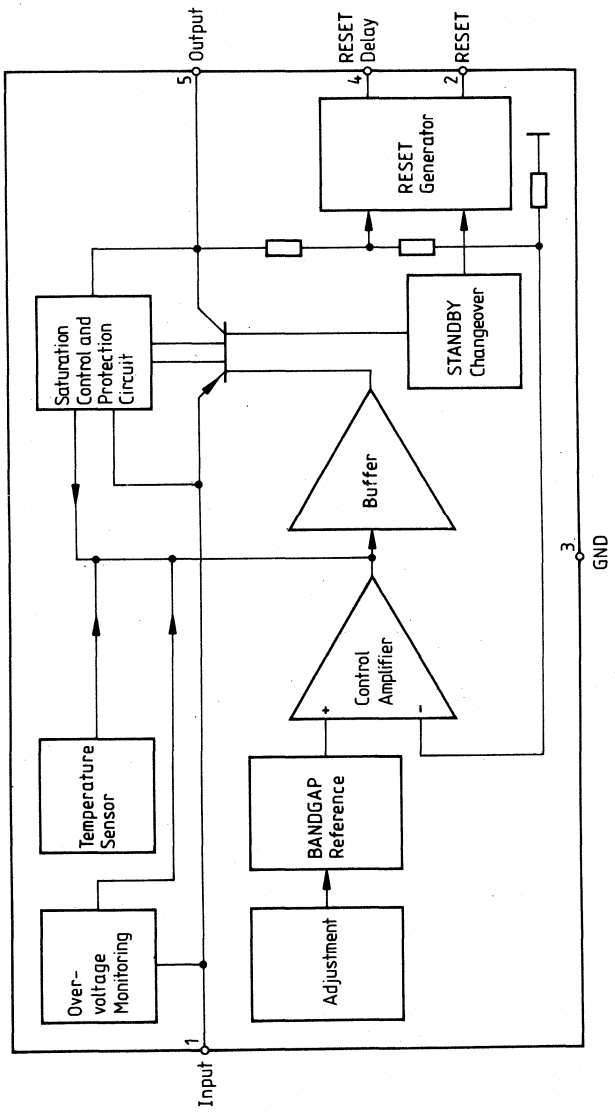
Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	V_I	Input
2	QVRES	Reset output
3	GND	Ground
4	DRES	Reset delay
5	V_Q	Output

Block Diagram



Maximum Ratings

Description	Symbol	min	max	Unit	Notes
Input (Pin 1)					
Input voltage	V_I	−42	42	V	
Input voltage	V_I		65	V	$t \leq 400$ ms
Input current	I_I		1.6	A	
Reset Output (Pin 2)					
Voltage	V_R	−0.3	42	V	
Current	I_R				internally limited
Ground (Pin 3)					
Current	I_{GND}	−0.5		A	
Reset Delay (Pin 4)					
Voltage	V_D	−0.3	42	V	
Current	I_D				internally limited
Output (Pin 5)					
Differential voltage	$V_I - V_Q$	−5.25	V_I	V	
Current	I_Q		1.4	A	
Temperature					
Junction temperature	T_j	−40	150	°C	
Storage temperature	T_{stg}	−50	150	°C	
Operating Range					
Input voltage	V_I	6	28	V	$I_Q = 0.5$ A
Input voltage	V_I	6	40	V	$I_Q = 0.15$ A
Junction temperature	T_j	−40	+150	°C	
Thermal resistance					
system – air	$R_{th\ SA}$		65	K/W	
system – case	$R_{th\ SC}$		3	K/W	

Characteristics

$V_I = 13.5$ V; $T_A = 25$ °C (unless otherwise specified)

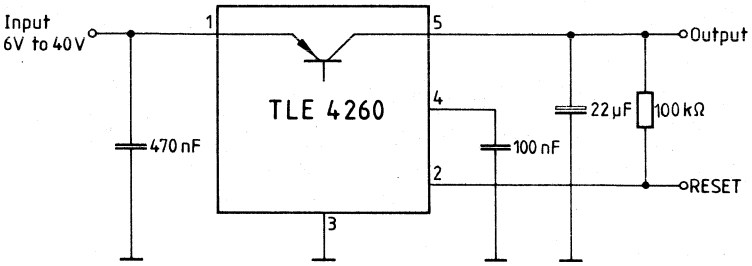
Description	Symbol	Test conditions	Test circuit	min	typ	max	Unit
Normal Operation							
Output voltage	V_Q	25 mA ≤ I_Q ≤ 500 mA 6 V ≤ V_I ≤ 28 V −40 °C ≤ T_j ≤ 125 °C	1	4.75	5.00	5.25	V
Output voltage	V_Q	25 mA ≤ I_Q ≤ 150 mA 6 V ≤ V_I ≤ 40 V −40 °C ≤ T_j ≤ 125 °C	1	4.75	5.00	5.25	V
Output current	I_Q	0 V ≤ V_I ≤ 2 V −40 °C ≤ T_j ≤ 125 °C	1			50	µA
Short-circuit current	I_{SC}	V_I = 17 V; V_Q = 0 V	1	750	1000		mA
Short-circuit current	I_{SC}	V_I = 28 V; V_Q = 0 V	1	500	700		mA
Short-circuit current	I_{SC}	V_I = 40 V; V_Q = 0 V	1	150	200		mA
Current consumption without load; $I = I\text{-}I_Q$	I	6 V ≤ V_I ≤ 28 V; I_Q = 150 mA	1		8.5	10	mA
Current consumption without load; $I = I\text{-}I_Q$	I	6 V ≤ V_I ≤ 28 V; I_Q = 500 mA	1		50	60	mA
Current consumption without load; $I = I\text{-}I_Q$	I	3.3 V ≤ V_I ≤ 6 V; I_Q = 150 mA	1			27.5	mA
Current consumption without load; $I = I\text{-}I_Q$	I	3,3 V ≤ V_I ≤ 6 V; I_Q = 500 mA	1			70	mA
Drop voltage	V_{Dr}	3.3 V < V_I < 5.45 V; I_Q = 0.5 A	1		0.35	0.5	V
Drop voltage	V_{Dr}	3.3 V < V_I < 5.05 V; I_Q = 0.15 A	1		0.20	0.3	V
Load regulation	ΔV_Q	I_Q = 25 mA to 500 mA	1		15	35	mV
Supply voltage regulation	ΔV_Q	V_I = 6 V to 28 V I_Q = 100 mA	1		15	75	mV
Supply voltage regulation	ΔV_Q	V_I = 6 V to 16 V I_Q = 100 mA	1		5	25	mV
Hum suppression	SVR	f_r = 100 Hz; V_r = 0.5 V_{SS}	1		54		dB
Temperature drift of output voltage	α_{VQ}		1		$2 \cdot 10^{-4}$		1/°C

Characteristics

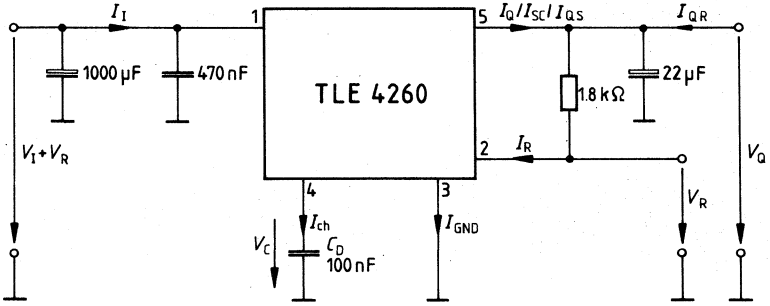
$V_I = 13.5$ V; $T_A = 25$ °C (unless otherwise specified)

Description	Symbol	Test conditions	Test circuit	min	typ	max	Unit
Standby Operation							
Quiescent current $I = I\text{-}I_Q$	I	$10\text{ V} < V_I < 16\text{ V}$; $I_Q = 0$ mA	1		500	600	µA
Current consumption without load; $I = I\text{-}I_Q$	I	$10\text{ V} < V_I < 16\text{ V}$; $I_Q = 5$ mA			700	850	µA
Standby Off/Normal Operation On							
Current consumption without load	$I_{QS\ OFF}$	see diagram	1		1.0	1.2	mA
Current consumption without load	$I_{QN\ ON}$	see diagram	1		1.7	2.2	mA
Normal Operation Off/Standby On							
Current consumption without load	$I_{QN\ OFF}$	see diagram	1		1.55	2.00	mA
Current consumption without load	$I_{QS\ ON}$	see diagram	1		850	1050	µA
Switching threshold	$I_{QN\ OFF}$	see diagram	1	7.5	10	12.5	mA
Switching hysteresis	ΔI_Q	see diagram	1	2.25	3	4	mA
Reset Generator							
Switching threshold	V_{RT}	in % of V_Q $I_Q = 500$ mA; $T_j = 150$ °C $V_I = 6$ V	1	95	95.5	96	%
Switching hysteresis	ΔV_{RT}		1		10		mV
Switching voltage	V_R	$I_R = 3$ mA	1		0.25	0.4	V
Reverse current	I_R	$V_R = 5$ V	1			1	µA
Charge current	I_{ch}		1	22.5	30	37.5	µA
Switching threshold	V_{ST}		1	0.9	1	1.1	V
Delay switching threshold	V_{DT}		1	2.25	2.50	2.75	V
Delay time	t_D	$C_D = 100$ nF	1		10		ms
	t_t	$C_D = 100$ nF	1		5		µs
General Ratings							
Turn-off voltage	$V_{I\ OFF}$	$I_Q < 1$ mA	1	41	43	45	V
Turn-off hysteresis	ΔV_I				3.0		V
Reverse current	I_{QS}	$V_Q = 0$ V $V_I = 45$ V	1		500		µA
Reverse output current	I_{QR}	$V_Q = 5$ V; V_I = open	1			1.5	mA

Application Circuit



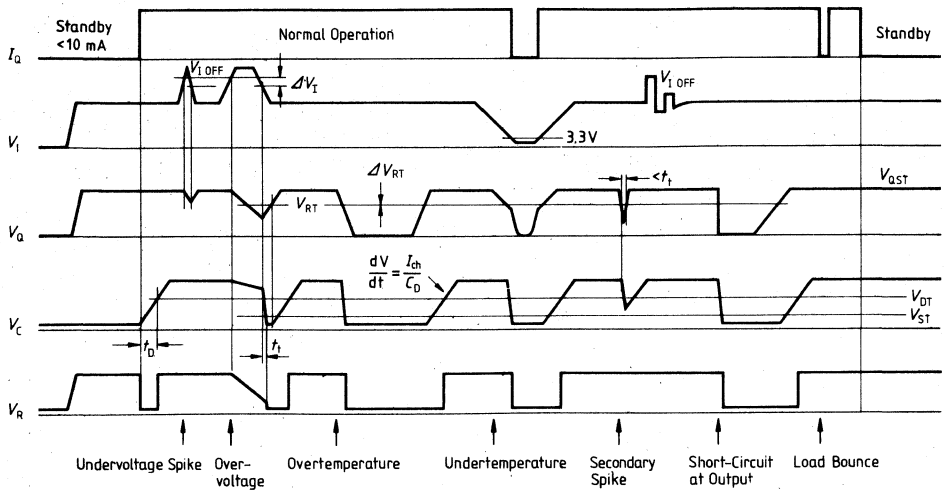
Measurement Circuit



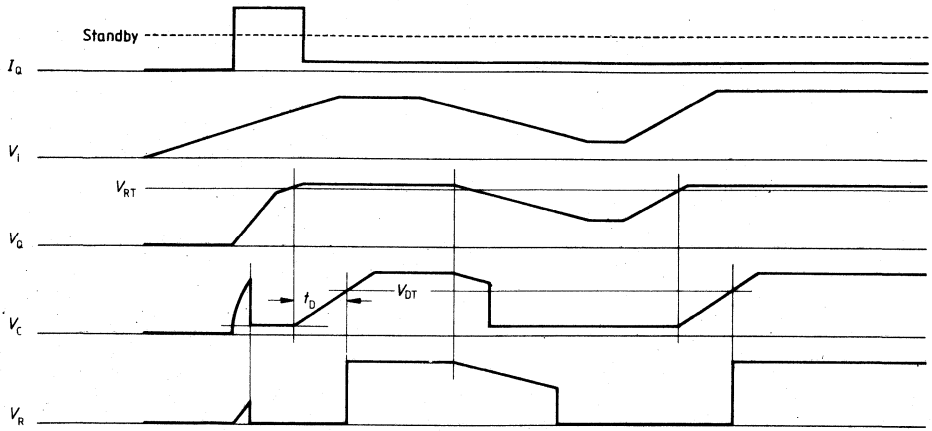
$V_{Dr} = V_I - V_Q$

$SVR = 20 \log \frac{V_R}{\Delta V_Q}$

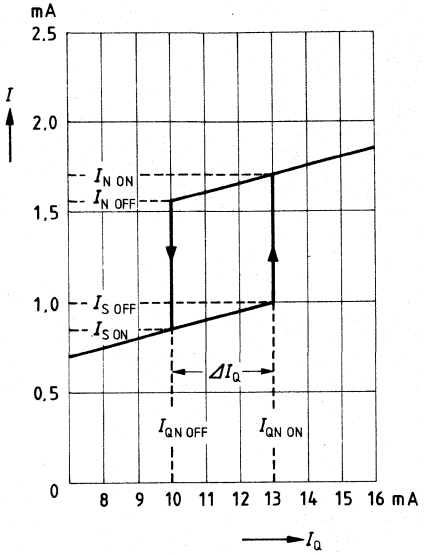
Time Response



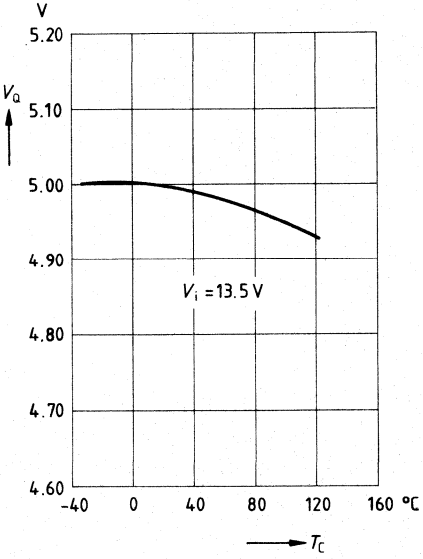
Time Response in Standby Condition



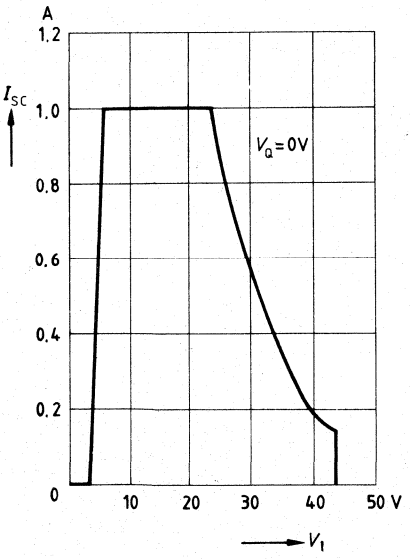
Standby/normal changeover



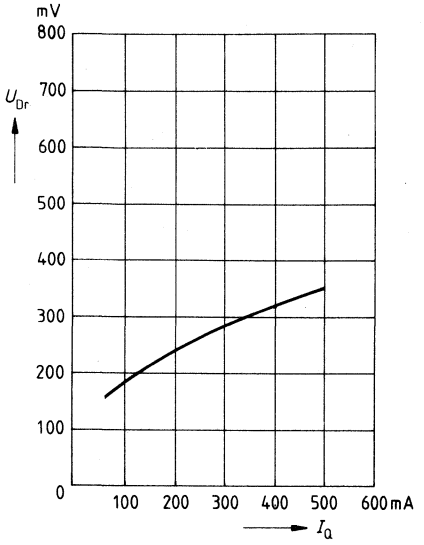
Output voltage versus temperature



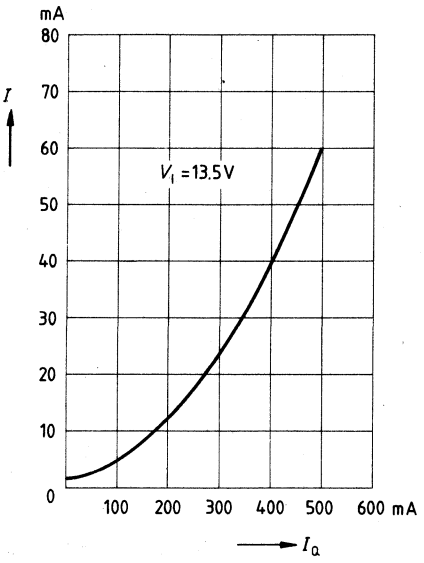
Short-circuit current versus input voltage



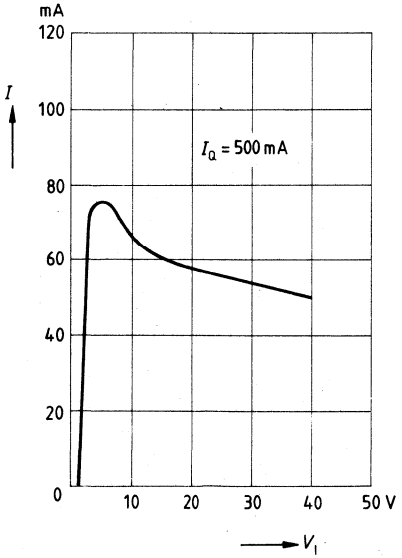
Minimum drop voltage versus output current



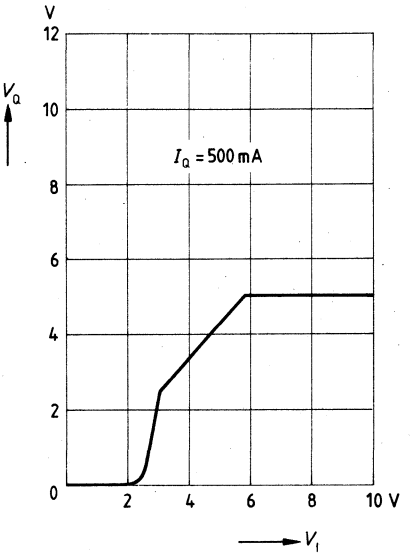
Current consumption without load versus output current



Current consumption without load versus input voltage



Output voltage versus input voltage



Drivers and Interface Circuits, Level Converters, Transistor Arrays

Selector Guide

Type	Package	Function	Supply voltage V_S (V_{CEO}) V	Temperature range T_A °C
Driver and Interface Circuits				
FZL 4141 D	P-DIP-18	Short-circuit proof driver for power transistors with short-circuit signaling output	4.5 to 35	0 to 70
FZL 4145 D	P-DIP-18		4.5 to 35	−25 to 85
Level Converters				
FZH 211 S	P-DIP-16	Driver and level converter for TTL, CMOS and LSL for applications of 5 to 30 V and 150 mA	4 to 30	0 to 70
FZH 215 S	P-DIP-16		4 to 30	−25 to 85
Transistor Arrays				
TCA 671	P-DIP-14	Transistor array 5 NPN transistors	42	−25 to 85
TCA 671 G	P-DSO-14 (SMD)		42	−25 to 85
TCA 871	P-DIP-14		32	−25 to 85
TCA 871 G	P-DSO-14 (SMD)		32	−25 to 85
TCA 971	P-DIP-14		42	−25 to 85
TCA 971 G	P-DSO-14 (SMD)		42	−25 to 85
TCA 991	P-DIP-14		32	−25 to 85
TCA 991 G	P-DSO-14 (SMD)		32	−25 to 85

Type	Ordering Code	Package
FZL 4141 D	Q67000-H8436	P-DIP-18
FZL 4145 D	Q67000-H8437	

Functional Description

The IC is comprised of four driver circuits capable of driving power transistors for high output currents. The output transistors are protected against short-circuit to ground and supply voltage. The input threshold can be adjusted between 1.5 V and 7 V. In the event of overloading or shorting of an output, a signaling process will respond.

Circuit Description

Each driver circuit has one active H input DI and a common enable input ENA (active H) is provided for all stages. The Q outputs are designed to drive the output transistors. The load current is sampled via pin W. If the load current exceeds the preset value, the output stage switches off. Switching-on again is provided by the built-in clock generator. Its operation requires an external capacitor C_T at pin C. If C_T is bridged by a break-key, switching on can only be carried out by operating a key. The duty cycle of the clock generator is 1:50 (e.g. 40 µs/2 ms with $C_T = 33$ nF).

If one of the four output stages is shorted to ground or has overcurrent, the short-signaling output will go L. In clock-governed operation (i.e. when there is automatic switching on by the clock and not by a key), SQ switches on and off at the clock rate as long as a short circuit or overload exists. SQ is an open-collector output.

Unused W pins must be connected to V_S. Open W pins simulate a short circuit and activate the signaling output.

The switching threshold at inputs DI and ENA can be adjusted between 1.5 V and 7 V via connection TS:

$V_{TS} = 0$ V;	input threshold = 1.5 V (for 5 V logic)
$V_{TS} = 0$ to 5 V;	input threshold = V_{TS} +1.5 V
$V_{TS} = V_S$:	input threshold = 7 V (for 12/15 V and 24/28 V logic)

If the output is disabled due to the logic states of inputs DI or ENA this disable is effective over the total supply voltage range between $V_S = 0$ V and $V_S = 35$ V.

The inputs are protected with clamp diodes.

Maximum Ratings

Description	Symbol	min	max	Unit	Notes
Supply voltage	V_S	−0.3	35	V	
Supply voltage	V_S	−0.3	45	V	100 ms duration, 1 s interval
Input voltage at DI and ENA	$V_{DI, ENA}$	−0.3	35	V	1)
Voltage at TS and SQ	$V_{TS, SQ}$	−0.3	45	V	
Output voltage V_Q and voltage at C	V_Q, V_C	−0.3	V_S	V	
Voltage at W	V_W	V_S−5	V_S	V	3)
Input current at DI and ENA	$I_{DI, ENA}$	−3	1	mA	2)
	$I_{DI, ENA}$	−6	2	mA	2) 100 ms duration, 1 s interval
	$I_{DI, ENA}$	−6	5	mA	2) 100 µs duration, 1 ms interval
Output current at SQ	I_{SQ}		8	mA	
Power dissipation of all input diodes	P_{tot}		50	mW	
Storage temperature	T_{stg}	−65	125	°C	
Thermal resistance					
system – air	$R_{th\ SA}$		65	K/W	
system – case	$R_{th\ SC}$		45	K/W	

Operating Range

Supply voltage for					
input threshold 1,5 V	V_S	4.5	35	V	$V_{TS} = 0$ V
input threshold 1.5 V to 6.5 V	V_S	V_{TS}+4.5	35	V	$V_{TS} = 0$ V to 5 V
input threshold 7 V	V_S	10	35	V	$V_{TS} = V_S$
Ambient temperature					
FZL 4141 D	T_A	0	70	°C	
FZL 4145 D	T_A	−25	85	°C	

Notes: 1) $V_{DI, ENA} > 35$ V requires a protective resistor before DI, ENA.
2) $V_{DI, ENA}$ may increase to more than 35 V during current nodes.
3) Unused W connections must be connected to V_S.

Characteristics

Supply voltage $4.5\ V \leq V_S \leq 30\ V$

FZL 4141 D $0\,°C \leq T_A \leq +70\,°C$

FZL 4145 D $-25\,°C \leq T_A \leq +85\,°C$

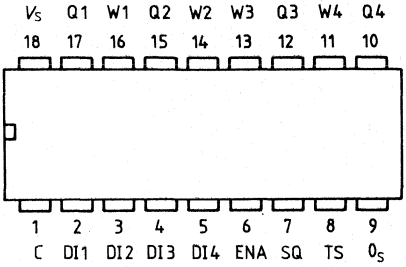
Description	Symbol	Test conditions	min	typ	max	Unit
Supply current	I_S	$V_{ENA} = 0\ V$, $V_W = V_S$		6	8.5	mA
H input voltage at DI, ENA	V_{IH}	$V_{TS} = 0\ V$	2			V
H input voltage at DI, ENA	V_{IH}	$V_{TS} = V_S$	8			V
L input voltage at DI, ENA	V_{IL}	$V_{TS} = 0\ V$			0.7	V
L input voltage at DI, ENA	V_{IL}	$V_{TS} = V_S$			6	V
Input current at DI, ENA	$I_{DI,\,ENA}$	$0.5\ V \leq V_{DI,ENA} \leq 30V$	50		200	µA
L output voltage at SQ	V_{SQL}	$I_{SQ} = 5\ mA$			0.5	V
Output current available[1]	I_Q	$V_Q = V_S - 1.5\ V$	1.5	2.5		mA
	I_Q	$T_A = 0\,°C$, $V_Q = V_S - 1.5\ V$	1.7			mA
Current from TS	$-I_{TS}$	$V_{TS} = 0\ V$		2	10	µA
Switching threshold at W	V_W		$V_S - 0.6$	$V_S - 0.5$	$V_S - 0.4$	V
Current in W	I_W				100	µA
Current from C	$-I_C$	$T_A = 20\,°C$	12	20	34	µA
Current in C	I_C	$T_A = 20\,°C$	0.6	1	1.7	mA
Upper switching threshold at C	V_{CU}	$T_A = 20\,°C$	1.6	2.1	1.7	V
Lower switching threshold at C	V_{CL}	$T_A = 20\,°C$	0.6	0.9	1.2	V
Saturation voltage at T[2]	V_{QR}	$V_W = V_S - 2V$, $I_Q = 0$		$V_S - 0.3$		V
H output voltage	V_{QH}	$V_{ENA} = 0\ V$	$V_S - 0.25$	$V_S - 0.02$		V

[1] The actual output current is typically 0.5 mA higher, a value which is required as current for the short-circuit protection. However, only the value specified above is available to drive the external output transistors.

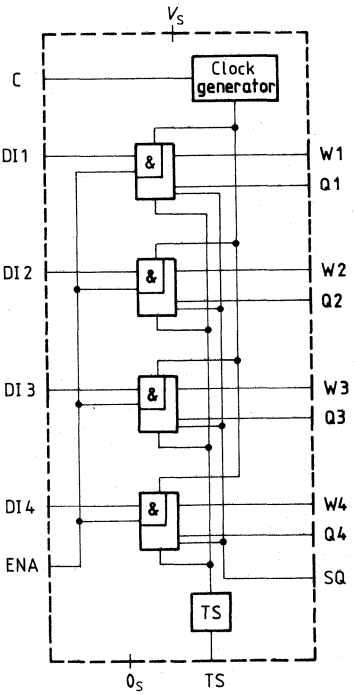
[2] See block diagram

Pin Configuration

top view

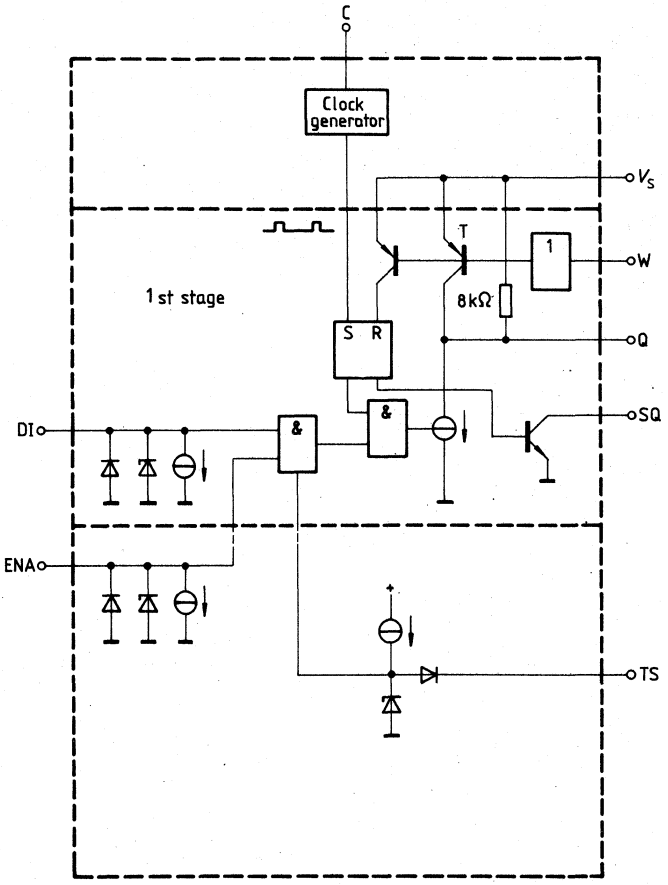


Block Diagram



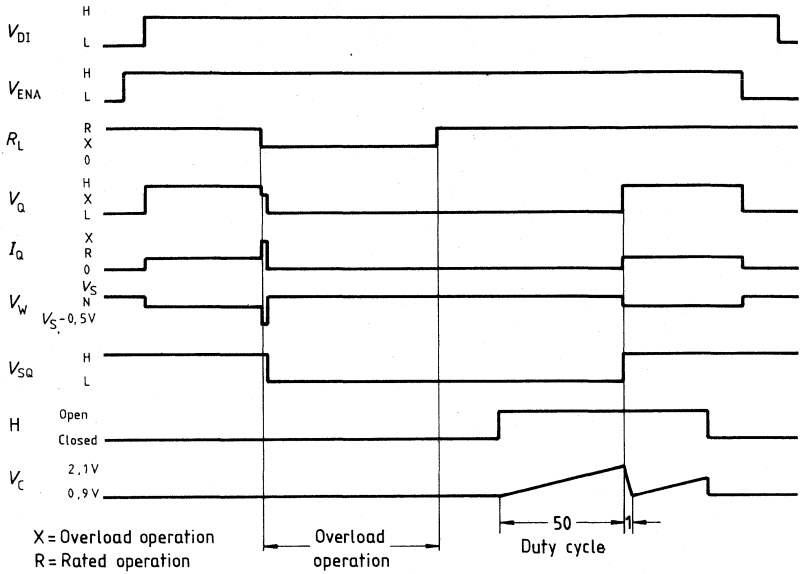
DI Driver input
ENA Enable input
C Clock capacitor
Q Output
TS Input for threshold switching
W Input for output current limiter
SQ Signaling output

Schematic Circuit Diagram of One Stage

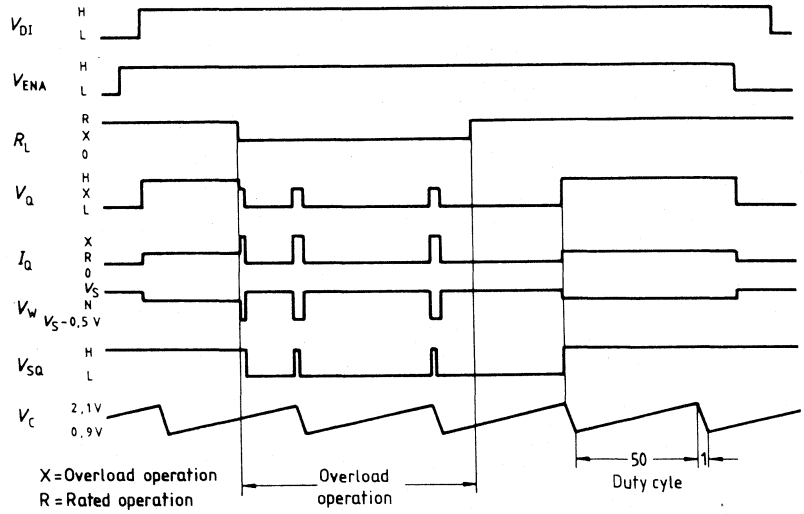


DI Driver input
ENA Enable input
C Clock capacitor
SQ Signaling output
Q Output
TS Input for threshold switching
W Input for output current limiter

Mode of Operation: Switching-On again after Overload with Key H



Mode of Operation: Automatic Switching-On again after Overload



Typical Application Circuits

The load conditions at Q depend on the permissible power dissipation of the power transistors used. The pulsed power dissipation in case of a short circuit must be observed.

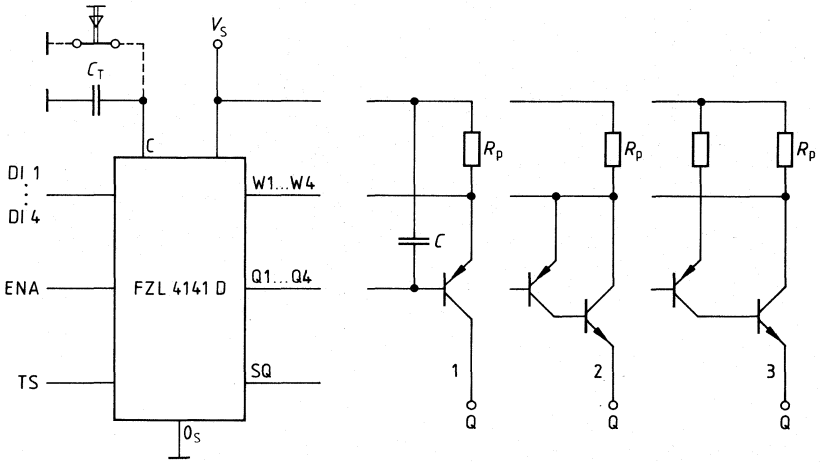
In order to suppress oscillations of the power stage in case of a short circuit, a capacitor C at Q 1 to Q 4 is necessary if e.g., fast switching transistors are used.

Typical value C approx. 20 nF.

The output circuit 1 is suited for currents up to approx. $I_Q = 100$ mA.

The output circuits 2 and 3 are suited for currents up to approx. $I_Q = 2$ A. A minimum power dissipation can be achieved with circuit 3.

A break key in parallel to C_T allows a manual switch-on in case of short circuit.



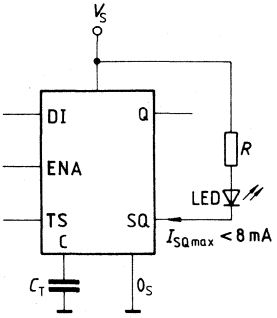
R_P = Precision resistor (current measurement)
$C_T = 0.8 \times t_p$ (nF, µs)
t_p = Short-circuit current pulse length

Note

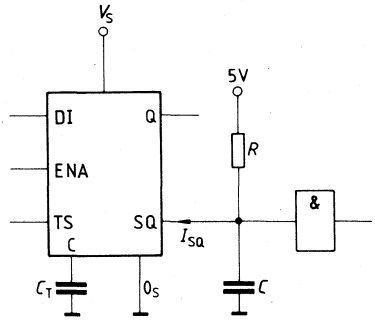
Circuit 1 does not permit a capacitor between Q 1 and Q 4 and the collector.
Circuit 2 does not permit a capacitor between Q 1 and Q 4 and base or emitter, respectively.
Otherwise too high current spikes would arise in case of a short circuit.

Typical Application of Short-Circuit Signaling Output SQ

1. LED Display



2. TTL/CMOS/LSL Driving



If the pulses that appear at SQ during clocked operation disturb the remainder of the circuit, a lowpass filter will be necessary. For a load current of $I_{SQ} = 1$ mA a capacitor C of approx. 10 nF is necessary to limit the output pulses of up to 10 µs (depending on C_T) to 1 V. Signaling occurs after approx. 50 µs.

Type	Ordering Code	Package
SFZH 211 S	Q67000-H639-S1	P-DIP-16
SFZH 215 S	Q67000-H2431	

Four NAND drivers with open collector outputs, 2 inputs, and N input for delay circuits. The input threshold can be switched to LSL, TTL, or CMOS level, depending on the supply voltage used.

Typical Application

Driver up to 30 V/150 mA, relay driver, and level converter.

Calculation of the load resistance for wired AND connection is carried out as described for FZH 161/181 (refer to LSL data book). In the case of wired AND connection and N wiring, the capacitors C_N must have identical values.

Maximum Ratings

Description	Symbol	Test conditions	min	max	Unit
Supply voltage	V_S		0	30	V
Input voltage	V_I		−0.5	30	V
Voltage between 2 inputs	V_{II}			30	V
Voltage at output, output transistor cut off	$V_{Q\,H}$			30	V
Voltage at output, output transistor conducting	$V_{Q\,L}$		0		V
Output current	$I_{Q\,L}$			150	mA
Capacitance at Q	C_L			5	nF
Capacitance between N and Q	C_N			0.1	µF
Voltage at N			−1	0.6	V
Current at N			−10	2	mA
Storage temperature	T_{stg}		−65	125	°C
Thermal resistance system – air	$R_{th\,SA}$			60	K/W

Operating Range

Supply voltage range 1	V_S	TTL threshold at A, B	4	7	V
Supply voltage range 2	V_S	LSL threshold at A, B	9	30	V
Supply voltage	V_S	Switching of threshold at A, B at $V_S = 8$ V, typical	4	30	V
Ambient temperature					
FZH 211 S (range 1)	T_A		0	70	°C
FZH 215 S (range 5)	T_A		−25	85	°C

Characteristics in the 5 V Range

Temperature range 1 and 5

Description	Symbol	Test conditions	min	typ	max	Unit
Supply voltage	V_S		4		7	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	2			V
L-input voltage	V_{IL}	$V_S = V_{SA}$ and V_{SB}			0.8	V
Static noise immunity	V_{sn}		0.4	1.0		V
L-output voltage	V_{QL}	$I_{QL} = 1.6$ mA | $V_{IH} = 8$ V		0.7	0.8	V
L-output voltage	V_{QL}	$I_{QL} = 100$ mA | $V_S = V_{SB}$			1.3	V
L-output voltage[1]	V_{QL}	$I_{QL} = 150$ mA			1.5	V
H-input current	I_{IH}	$U_{IH} = 30$ V | $V_{IH} = V_{SA}$			1	µA
L-input current	$-I_{IL}$	$V_{IL} = 0$ V		5	50	µA
H-output current	I_{QL}	$V_{IL} = 0.8$ V, $V_{QH} = 30$ V, $V_S = V_{SB}$			50	µA
Supply current per package	I_S	$V_S = 7$ V, $V_I = 0$ V	1.5	3	5	mA

Characteristics in the 12 V, 15 V, 24 V Ranges

Temperature range 1 and 5

Supply voltage	V_S		9		30	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	8			V
L-input voltage	V_{IL}	$V_S = V_{SA}$ and V_{SB}			6	V
Static noise immunity	V_{sn}		2.5	5.0		V
L-output voltage	V_{QL}	$I_{QL} = 100$ mA | $V_{IH} = 8$ V		1	1.3	V
L-output voltage[1]	V_{QL}	$I_{QL} = 150$ mA | $V_S = V_{SB}$			1.5	V
H-Input current	I_{IH}	$V_{IH} = 30$ V | $V_S = V_{SA}$			1	µA
L-Input current	$-I_{IL}$	$V_{IL} = 0$ V		5	50	µA
H-output current	I_{QH}	$V_{IL} = 6$ V, $V_{QH} = 30$ V, $V_S = V_{SB}$			50	µA
Supply current per package	I_S	$V_S = 30$ V, $V_I = 0$ V	1.5	3	5	mA

Switching Characteristics at $V_S = 12$ V, $T_A = 25$ °C

Signal propagation time	t_{PLH}	$V_{SC} = 12$ V $R_C = 760\ \Omega$ $C_L = 15$ pF		550		ns
	t_{PHL}			200		ns
Signal transition time	t_{TLH}			90		ns
	t_{THL}			25		ns

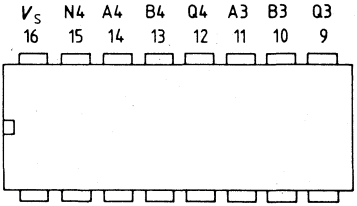
Signal transition times at Q
with C_N wiring between N and Q:

$$\left.\begin{aligned} t_{THL} &= 6 \cdot C_N \cdot (V_{QH} - V_{QL}) \\ t_{TLH} &= 15 \cdot C_N \cdot (V_{QH} - V_{QL}) \end{aligned}\right\} \text{(µs, µF, V)}$$

typical values for $C_N > 0.02$ µF

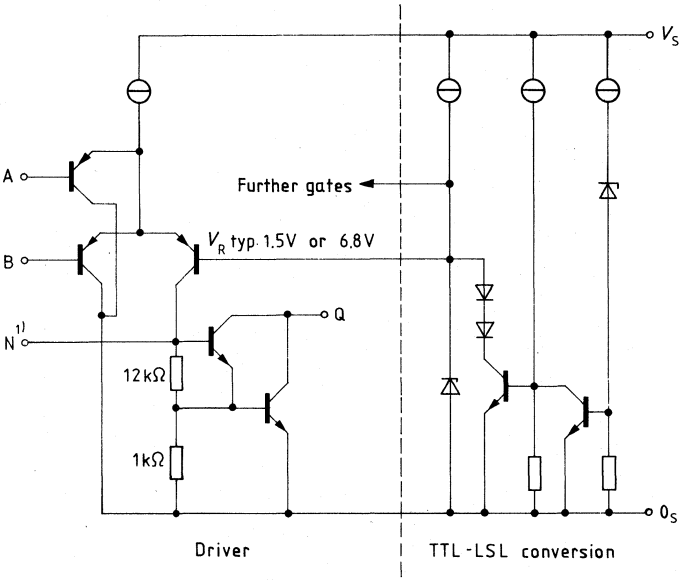
[1]) The sum of all output currents per package may not exceed 400 mA for the FZH 211 S and 350 mA for the FZH 215 S.

Pin Configuration
top view



A, B = inputs
Q = output

Schematic (one gate)



Logic function $Q = \overline{A \wedge B}$

1) only in case of gate 1 and 4

Transistor Array with 5 NPN Transistors

TCA 671
TCA 871
TCA 971
TCA 991

Bipolar IC

Type	Ordering Code	Package
TCA 671	Q67000-T1	P-DIP-14
TCA 671 G	Q67000-A2366	P-DSO-14 (SMD)
TCA 871	Q67000-T2	P-DIP-14
TCA 871 G	Q67000-A2367	P-DSO-14 (SMD)
TCA 971	Q67000-T11	P-DIP-14
TCA 971 G	Q67000-A8075	P-DSO-14 (SMD)
TCA 991	Q67000-T12	P-DIP-14
TCA 991 G	Q67000-A8076	P-DSO-14 (SMD)

TCA 671, TCA 871, TCA 971, and TCA 991 are monolithic integrated transistor arrays each consisting of five NPN transistors. The arrays are well suited for switching and amplifying applications up to approx. 30 MHz. Due to a uniform design, the transistor characteristics show only slight deviations. The arrays are preferably intended for lamp drivers, amplifiers, pulse generators, and types TCA 971 and TCA 991 especially for discrete differential amplifiers.

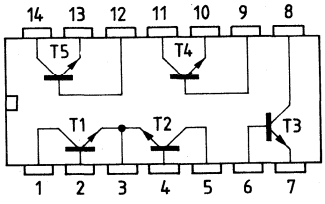
Features

- Versatile use
- Slight V_{BE} and B deviations
- High output current
- Good thermal matching
- TCA 971;G/TCA 991;G compatible with 3045/46/86 and 3146

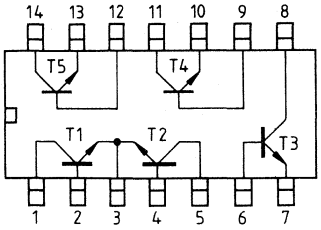
Pin Configurations

(top view)

TCA 671, TCA 871 substrate = pin 3
TCA 971, TCA 991 substrate = pin 13
Substrate connection has to be on the most negative potential.



TCA 671 G, TCA 871 G,
TCA 971 G, TCA 991 G



Maximum Ratings

Description	Symbol	TCA 671 TCA 971	TCA 871 TCA 991	Unit
Collector-base breakdown voltage	V_{CB0}	45	35	V
Collector-emitter breakdown voltage	V_{CE0}	42	32	V
Emitter-base breakdown voltage	V_{EB0}	6	6	V
Collector-substrate voltage ($I_C = 100\ \mu A$)	V_{CS}	70	60	V
Collector current	I_C	200	200	mA
Base current	I_B	10	10	mA
Permissible power dissipation for a single transistor	P_{tot}	300	300	mW
Junction temperature	T_j	150	150	°C
Storage temperature range	T_{stg}	−40 to 125	−40 to 125	°C
Thermal resistance system – air TCA 671 G; TCA 871 G;	$R_{th\ SA}$	85	85	K/W
TCA 971 G; TCA 991 G	$R_{th\ SA}$	145	145	K/W

Operating Range

Ambient temperature	T_A	−25 to 85	−25 to 85	°C

Characteristics

$T_A = 25\,°C$

Description	Symbol	TCA 671 TCA 971 min	typ	max	TCA 871 TCA 991 min	typ	max	Unit
Collector-base breakdown voltage at $I_C = 100\ \mu A$, $I_E = 0$	V_{CB0}	45			35			V
Collector-emitter breakdown voltage at $I_C = 100\ \mu A$, $I_B = 0$	V_{CE0}	42			32			V
Collector-substrate breakdown voltage at $I_C = 100\ \mu A$, $I_{CS} = 0$	V_{CS}	70			60			V
Emitter-base breakdown voltage at $I_E = 100\ \mu A$, $I_C = 0$	V_{EB0}	6			6			V
Collector-emitter saturation voltage at $I_C = 50$ mA; $I_B = 5$ mA	$V_{CE\ Sat}$		200	350		200	350	mV
Collector-base cutoff current at $V_{CB} = 25$ V, $I_E = 0$	I_{CB0}		0.02	1		0.02	10	µA
Collector-emitter cutoff current at $V_{CE} = 25$ V, $I_B = 0$	I_{CE0}			1			10	µA
Static current gain	B							
at $V_{CE} = 3$ V, $I_C = 100\ \mu A$		40	80		40	80		
at $V_{CE} = 3$ V, $I_C = 1$ mA		100	140		100	140		
at $V_{CE} = 3$ V, $I_C = 10$ mA		100	160		100	160		
at $V_{CE} = 3$ V, $I_C = 100$ mA		40	100		40	100		

Characteristics

$T_A = 25\,°C$

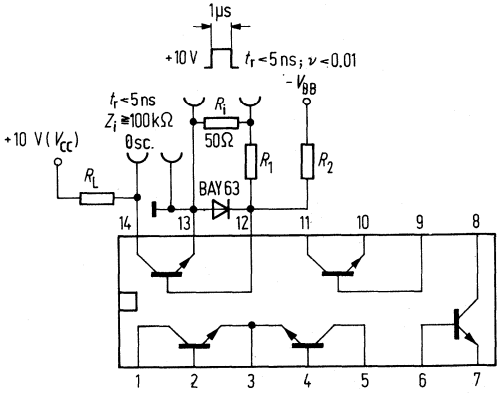
Description	Symbol	TCA 671 TCA 971 min	typ	max	TCA 871 TCA 991 min	typ	max	Unit
Differential base current for transistors T1 = T2 at $V_{CE} = 3$ V, $I_C = 1$ mA	I_{BD}		0.5	1		1		µA
Base-emitter voltage at $V_{CE} = 3$ V, $I_C = 1$ mA	V_{BE}		0.65			0.65		V
Differential base-emitter voltage for transistors T1 + T2 at $V_{CE} = 3$ V, $I_C = 1$ mA	V_{BED}		2	5		4		mV
Differential base-emitter voltage for transistors T3 to T5 at $V_{CE} = 3$ V, $I_C = 1$ mA	V_{BED}		4	10		6		mV
Temperature coefficient of base-emitter voltage at $V_{CE} = 3$ V, $I_C = 1$ mA	$\frac{\Delta V_{BE}}{\Delta T}$		−2			−2		mV/K
Transition frequency	f_T	300	550		300	550		MHz

Switching Times

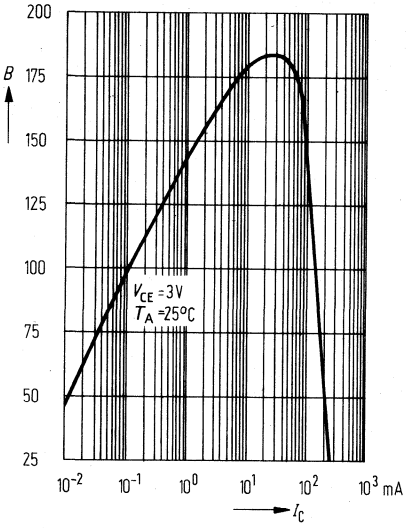
I_C: I_{B1}: $-I_{B2} \approx 10:1:1$ mA; $R_1 = 5$ kΩ; $R_2 = 5$ kΩ; $V_{BB} = 3.5$ V; $R_L = 990$ Ω
t_{ON} 85 (< 150) ns t_{OFF} 480 (< 800) ns

I_C: I_{B1}: $-I_{B2} \approx 100:10:10$ mA; $R_1 = 500$ Ω; $R_2 = 700$ Ω; $V_{BB} = 5$ V; $R_L = 98$ Ω
t_{ON} 55 (< 150) ns t_{OFF} 450 (< 800) ns

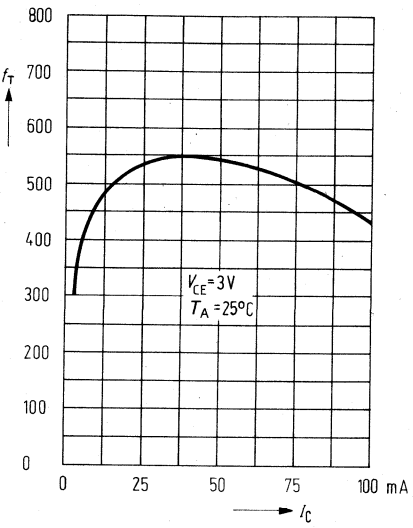
Measurement Circuit for Switching Times



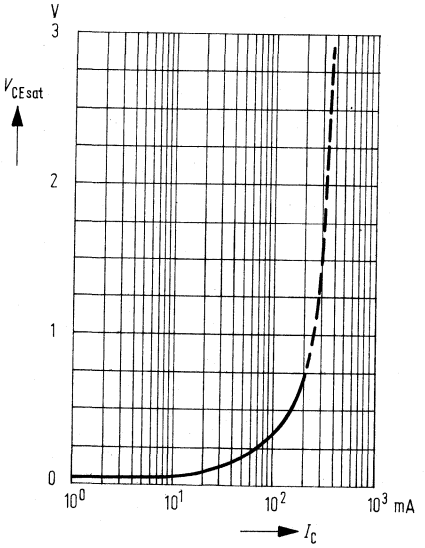
Current gain versus collector current
$V_{CE} = 3$ V; $T_A = 25$ °C



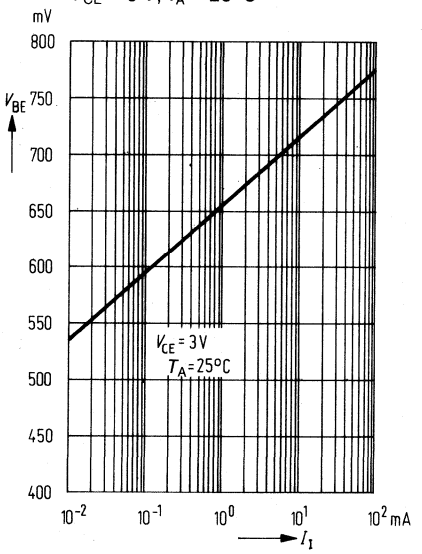
Transition frequency versus collector current
$V_{CE} = 3$ V; $T_A = 25$ °C



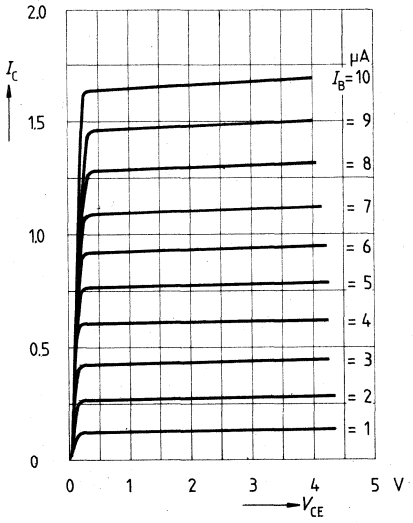
Collector-emitter saturation voltage versus collector current
$B = 20$



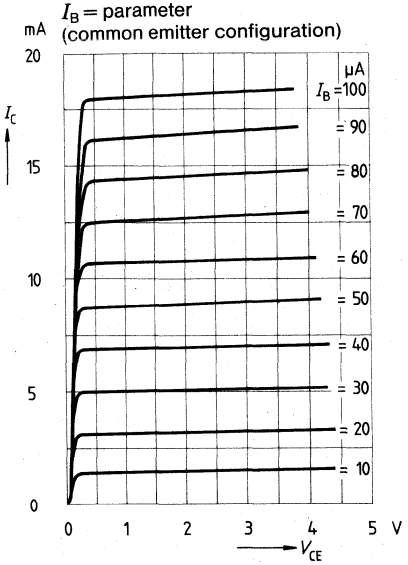
Base-emitter voltage versus input current
$V_{CE} = 3$ V; $T_A = 25$ °C



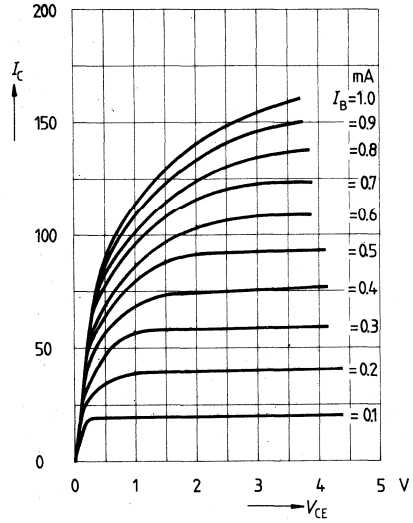
Output characteristics
Collector current versus
collector-emitter voltage
I_B = parameter
(common emitter configuration)



Output characteristics
Collector current versus
collector-emitter voltage
I_B = parameter
(common emitter configuration)



Output characteristics
Collector current versus
collector-emitter voltage
I_B = parameter
(common emitter configuration)



Control ICs for Thyristors and Triacs

Selector Guide

Type	Package	Function	Technical data	
TCA 785	P-DIP-16	Phase control for thyritors, triacs, transistors, 250 mA output current	**Supply voltage** V_S (V_{CEO}) V	**Temperature range** T_A °C
			8 to 18	−25 to 85
TLE 3101 TLE 3102 TLE 3103 TLE 3104	P-DIP-18 P-DIP-14 P-DIP-14 P-DIP-8	Phase control for design of control ICs. Typical applications: motor control for kitchen appliances, brightness and temperature control	V_S = 10 to 30 V I_S = typ. 2.4 mA	
SLB 0586	P-DIP-8	Electronic CMOS brightness control	V_S = −4.8 to −5.8 V	

Bipolar IC

Type	Ordering Code	Package
TCA 785	Q67000-A2321	P-DIP-16

This phase control IC is intended to control thyristors, triacs, and transistors. The trigger pulses can be shifted within a phase angle between 0° and 180°. Typical applications include converter circuits, AC controllers and three-phase current controllers.

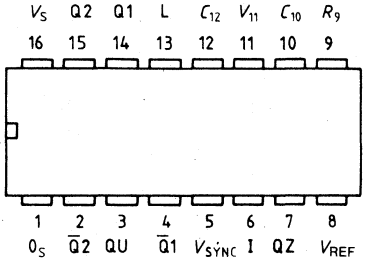
This IC replaces the previous types TCA 780 and TCA 780 D.

Features

- Reliable recognition of zero passage
- Large application scope
- May be used as zero point switch
- LSL compatible
- Three-phase operation possible (3 ICs)
- Output current 250 mA
- Large ramp current range
- Wide temperature range

Pin Configuration

top view



Pin Description

Pin	Symbol	Function
1	0_S	Ground
2	$\overline{Q}$ 2	Output 2 inverted
3	Q U	Output U
4	$\overline{Q}$ 1	Output 1 inverted
5	V_{SYNC}	Synchronous voltage
6	I	Inhibit
7	Q Z	Output Z
8	V_{REF}	Stabilized voltage
9	R_9	Ramp resistance
10	C_{10}	Ramp capacitance
11	V_{11}	Control voltage
12	C_{12}	Pulse extension
13	L	Long pulse
14	Q 1	Output 1
15	Q 2	Output 2
16	V_S	Supply voltage

Functional Description

The synchronization signal is obtained via a high-ohmic resistance from the line voltage (voltage V_5). A zero voltage detector evaluates the zero passages and transfers them to the synchronization register.

This synchronization register controls a ramp generator, the capacitor C_{10} of which is charged by a constant current (determined by R_9). If the ramp voltage V_{10} exceeds the control voltage V_{11} (triggering angle φ), a signal is processed to the logic. Dependent on the magnitude of the control voltage V_{11}, the triggering angle φ can be shifted within a phase angle of 0° to 180°.

For every half wave, a positive pulse of approx. 30 µs duration appears at the outputs Q1 and Q2. The pulse duration can be prolonged up to 180° via a capacitor C_{12}. If pin 12 is connected to ground, pulses with a duration between φ and 180° will result.

Outputs $\overline{Q}1$ and $\overline{Q}2$ supply the inverse signals of Q1 and Q2.

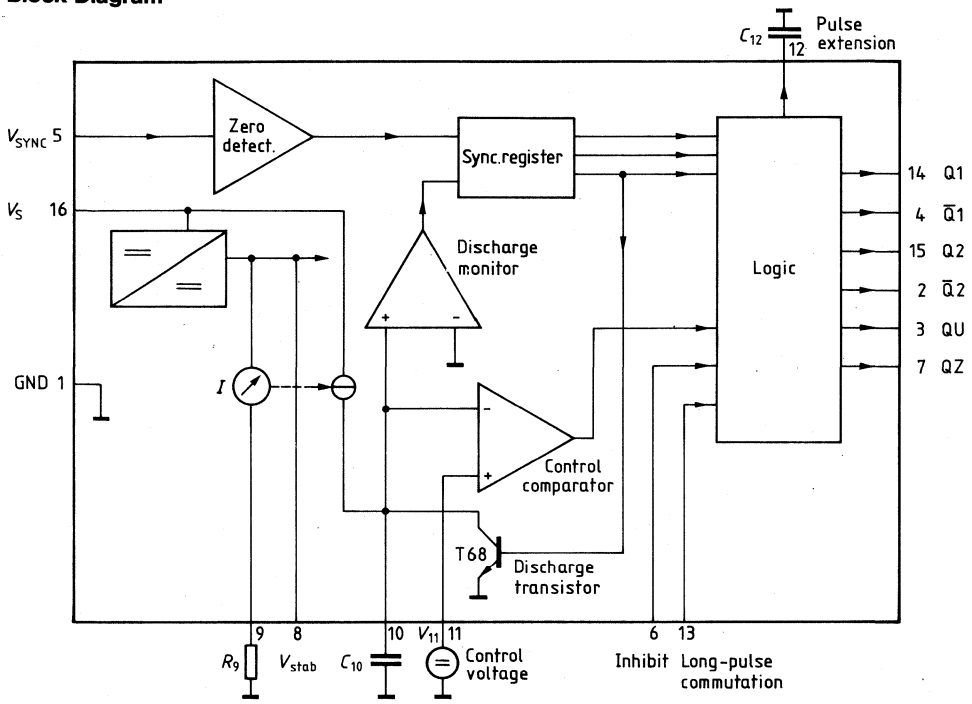
A signal of $\varphi + 180°$ which can be used for controlling an external logic, is available at pin 3.

A signal which corresponds to the NOR link of Q1 and Q2 is available at output QZ (pin 7).

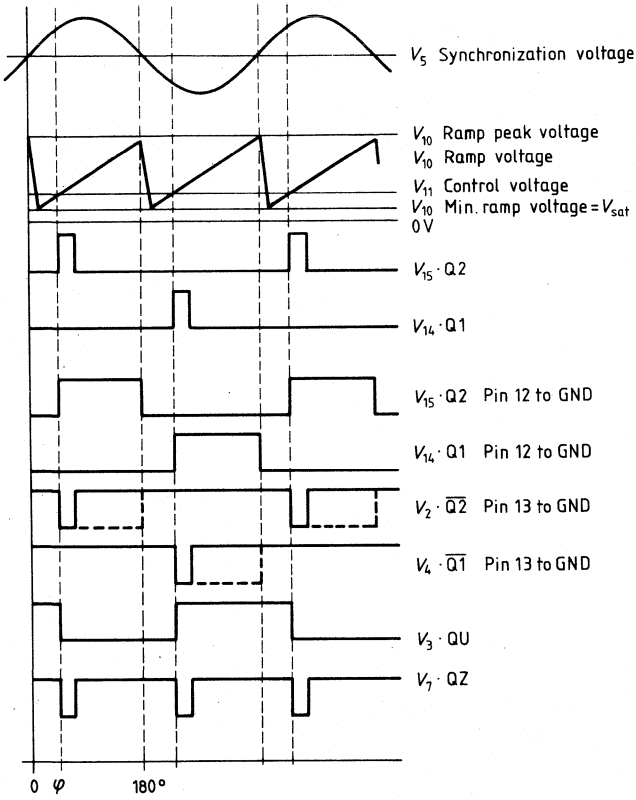
The inhibit input can be used to disable outputs Q1, Q2 and $\overline{Q}1$, $\overline{Q}2$.

Pin 13 can be used to extend the outputs $\overline{Q}1$ and $\overline{Q}2$ to full pulse length (180° – φ).

Block Diagram



Pulse Diagram



Maximum Ratings

Description	Symbol	min	max	Unit
Supply voltage	V_S	−0.5	18	V
Output current at pin 14, 15	I_Q	−10	400	mA
Inhibit voltage Control voltage Voltage short-pulse curcuit	V_6 V_{11} V_{13}	−0.5 −0.5 −0.5	V_S V_S V_S	V V V
Synchronization input current	I_5	−200	±200	µA
Output voltage at pin 14, 15	V_Q		V_S	V
Output current at pin 2, 3, 4, 7	I_Q		10	mA
Output voltage at pin 2, 3, 4, 7	V_Q		V_S	V
Junction temperature Storage temperature	T_j T_{stg}	 −55	125 125	°C °C
Thermal resistance system – air	$R_{th\ SA}$		80	K/W

Operating Range

Supply voltage	V_S	8	18	V
Operating frequency	f	10	500	Hz
Ambient temperature	T_A	−25	85	°C

Characteristics

$8 \leq V_S \leq 18$ V; $-25\,°C \leq T_A \leq +85\,°C$; $f = 50$ Hz

Description	Symbol	Test circuit	min	$f = 50$ Hz $V_S = 15$ V typ	max	Unit
Supply current consumption S1...S6 open $V_{11} = 0$ V $C_{10} = 47$ nF; $R_9 = 100$ kΩ	I_S	1	4.5	6.5	10	mA
Synchronization pin 5 Input current R_2 varied	$I_{5\,rms}$	1	30		200	µA
Offset voltage	ΔV_5	4		30	75	mV
Control input pin 11 Control voltage range Input resistance	V_{11} R_{11}	1 5	0.2	 15	$V_{10\,peak}$	V kΩ
Ramp generator Charge current Max. ramp voltage Saturation voltage at capacitor Ramp resistance Sawtooth return time	I_{10} V_{10} V_{10} R_9 t_f	 1 1.6 1 1	10 100 3	 225 80	1000 V_2-2 350 300	µA V mV kΩ µs
Inhibit pin 6 switch-over of pin 7 Outputs disabled Outputs enabled Signal transition time Input current $V_6 = 8$ V Input current $V_6 = 1.7$ V	 $V_{6\,L}$ $V_{6\,H}$ t_r $I_{6\,H}$ $-I_{6\,L}$	 1 1 1 1 1	 4 1 80	 3.3 3.3 500 150	 2.5 5 800 200	 V V µs µA µA
Deviation of I_{10} $R_9 =$ const. $V_S = 12$ V; $C_{10} = 47$ nF	I_{10}	1	−5		5	%
Deviation of I_{10} $R_9 =$ const. $V_S = 8$ V to 18 V	I_{10}	1	−20		20	%
Deviation of the ramp voltage between 2 following half-waves, $V_S =$ const.	$\Delta V_{10\,max}$			±1		%

Characteristics

$8 \leq V_S \leq 18$ V; $-25°C \leq T_A \leq +85°C$; $f = 50$ Hz

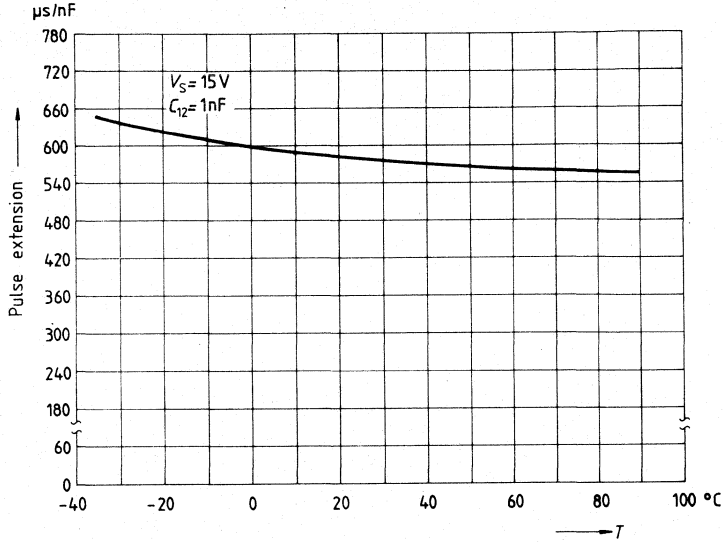
Description	Symbol	Test circuit	min	$f = 50$ Hz $V_S = 15$ V typ	max	Unit
Long pulse switch-over pin 13 switch-over of S 8						
Short pulse at output	$V_{13\,H}$	1	3.5	2.5		V
Long pulse at output	$V_{13\,L}$	1		2.5	2	V
Input current $V_{13} = 8$ V	$I_{13\,H}$	1			10	µA
Input current $V_{13} = 1.7$ V	$-I_{13\,L}$	1	45	65	100	µA
Outputs pin 2, 3, 4, 7						
Reverse current $V_Q = V_S$	I_{CE0}	2.6			10	µA
Saturation voltage $I_Q = 2$ mA	V_{sat}	2.6	0.1	0.4	2	V
Outputs pin 14, 15						
H output voltage $-I_Q = 250$ mA	$V_{14/15\,H}$	3.6	V_S-3	$V_S-2.5$	$V_S-1.0$	V
L output voltage $I_Q = 2$ mA	$V_{14/15\,L}$	2.6	0.3	0.8	2	V
Pulse width (short pulse) S 9 open	t_p	1	20	30	40	µs
Pulse width (short pulse) with C_{12}	t_p	1	530	620	760	µs/nF
Internal voltage control						
Reference voltage	V_{REF}	1	2.8	3.1	3.4	V
Parallel connection of 10 ICs possible						
TC of reference voltage	α_{REF}	1		2×10^{-4}	5×10^{-4}	1/K

Application Hints for External Components

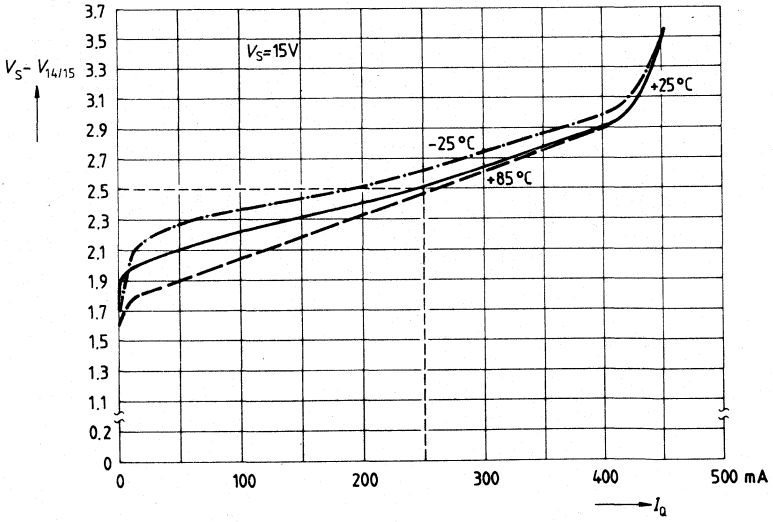
		min	max	
Ramp capacitance	C_{10}	500 pF	1 µF[1]	The minimum and maximum values of I_{10} are to be observed
Triggering point	$t_{Tr} = \frac{V_{11} \times R_9 \times C_{10}}{V_{REF} \times K}$		[2]	
Charge current	$I_{10} = \frac{V_{REF} \times K}{R_9}$		[2]	Ramp voltage $V_{10\,max} = V_S - 2$ V $V_{10} = \frac{V_{REF} \times K \times t}{R_9 \times C_{10}}$ [2]

1) Attention to flyback times
2) $K = 1.10 \pm 20\%$

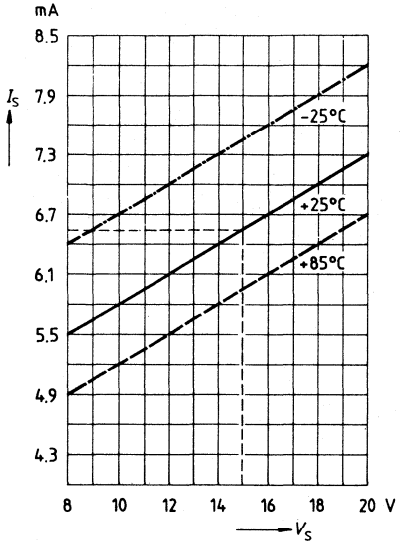
Pulse extension versus temperature



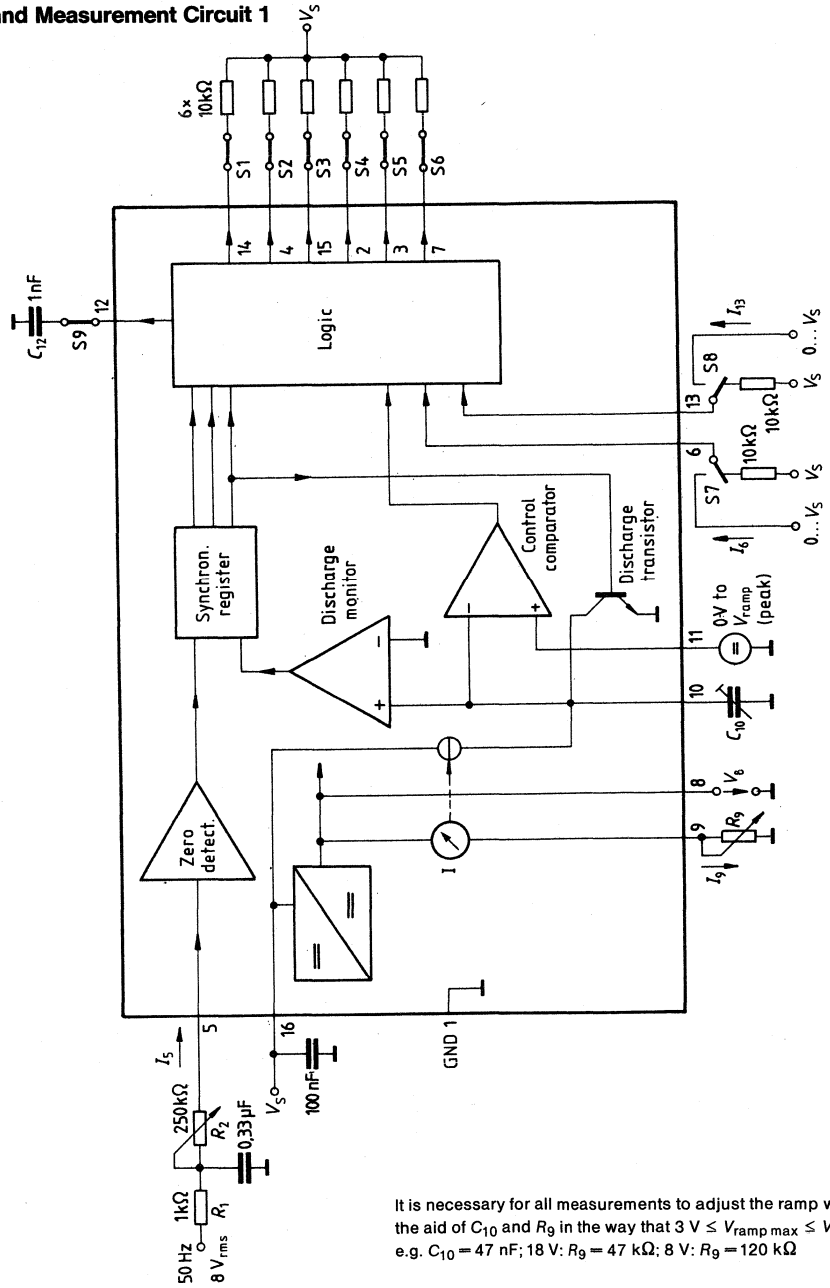
Output voltage measured to $+V_S$



Supply current versus supply voltage



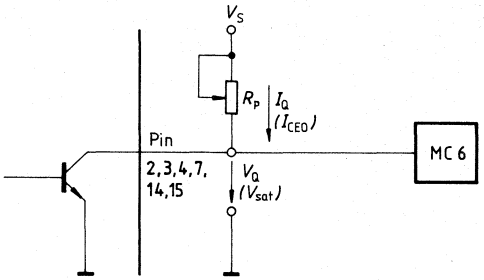
Test and Measurement Circuit 1



It is necessary for all measurements to adjust the ramp with the aid of C_{10} and R_9 in the way that $3\ V \leq V_{ramp\ max} \leq V_S - 2\ V$
e.g. $C_{10} = 47$ nF; 18 V: $R_9 = 47$ kΩ; 8 V: $R_9 = 120$ kΩ

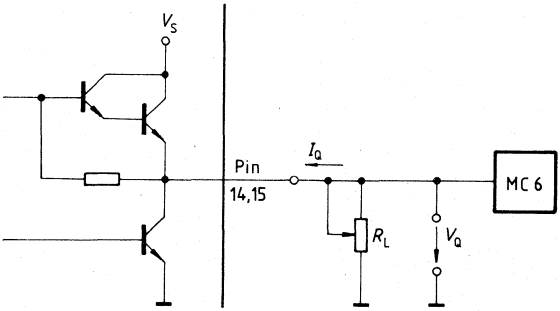
Test and Measurement Circuits

Measurement circuit 2



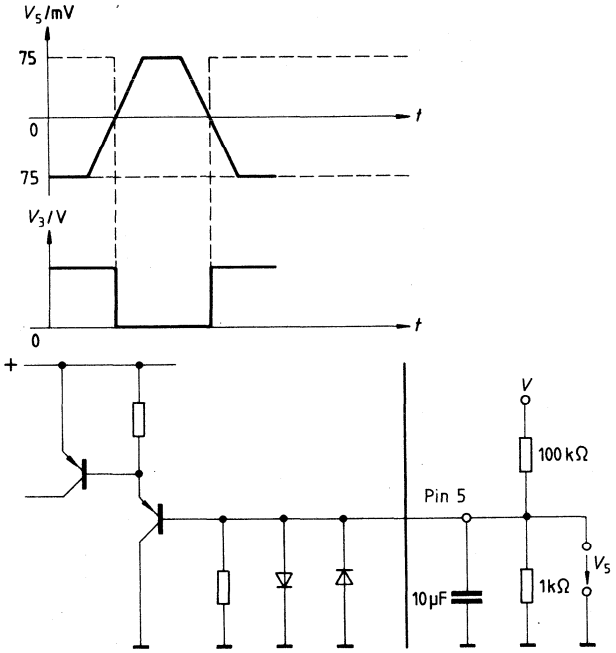
The remaining pins are connected as in measurement circuit 1

Measurement circuit 3



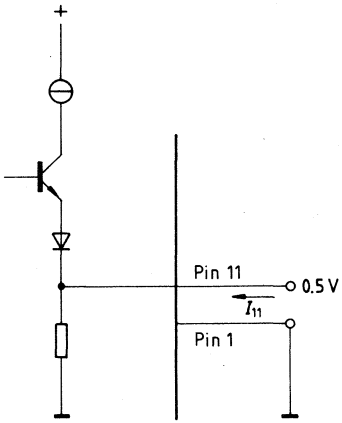
The remaining pins are connected as in measurement circuit 1

Measurement circuit 4

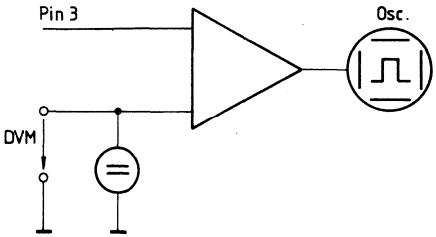


Remaining pins are connected as in measurement circuit 1
The 10 µF capacitor at pin 5 serves only for test purposes

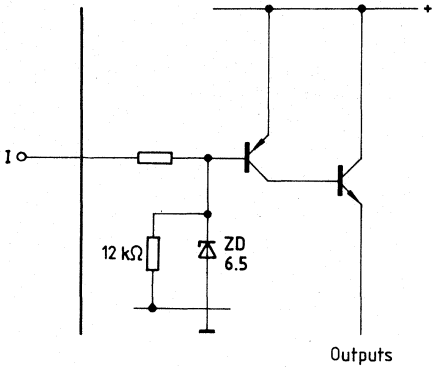
Measurement circuit 5



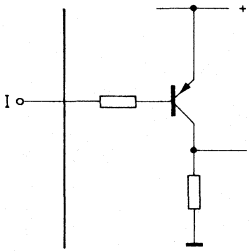
Measurement circuit 6



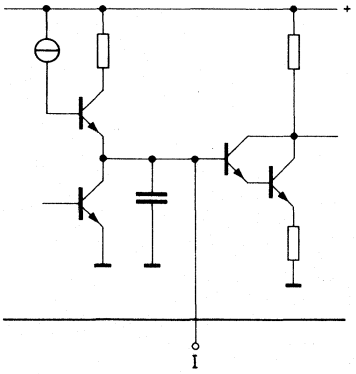
Inhibit 6



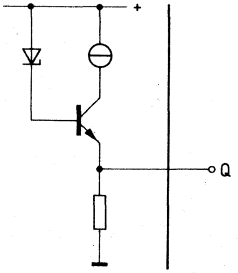
Long pulse 13



Pulse extension 12



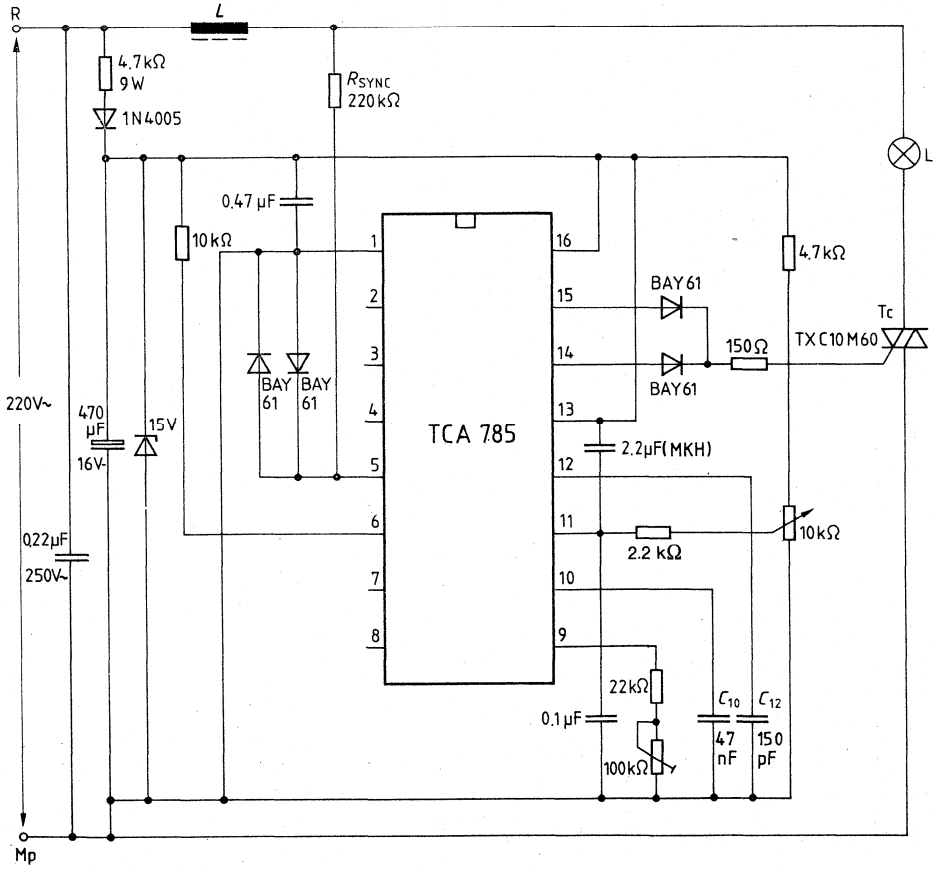
Reference voltage 8



Additional Circuit Description

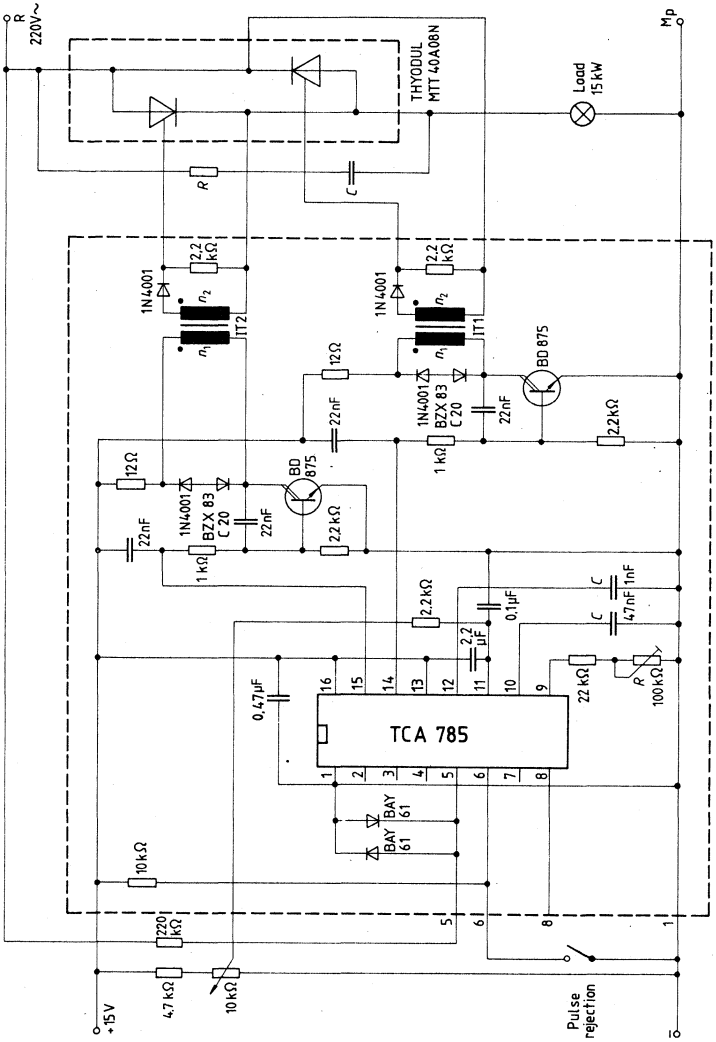
Application Examples

Triac Control for up to 50 mA Gate Trigger Current



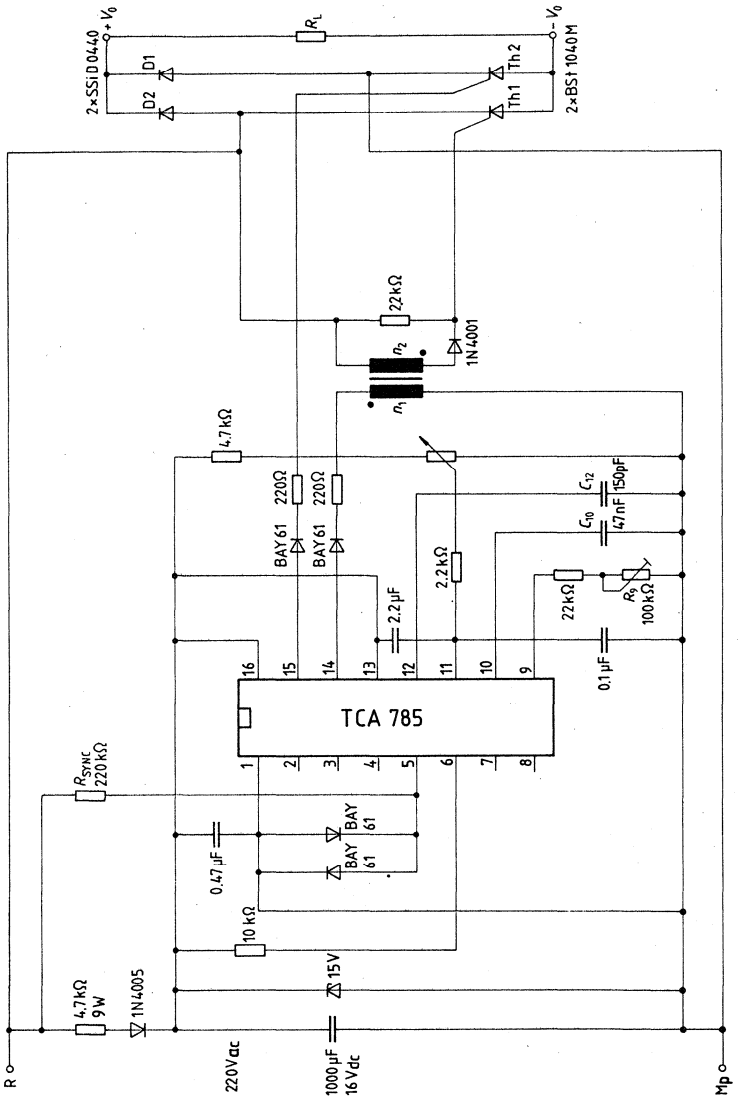
A phase control with a directly controlled triac is shown in the figure. The triggering angle of the triac can be adjusted continuously between 0° and 180° with the aid of an external potentiometer. During the positive half-wave of the line voltage, the triac receives a positive gate pulse from the IC output pin 15. During the negative half-wave, it also receives a positive trigger pulse from pin 14. Trigger pulse width is approx. 100 µs.

Fully Controlled AC Power Controller
Circuit for Two High-Power Thyristors

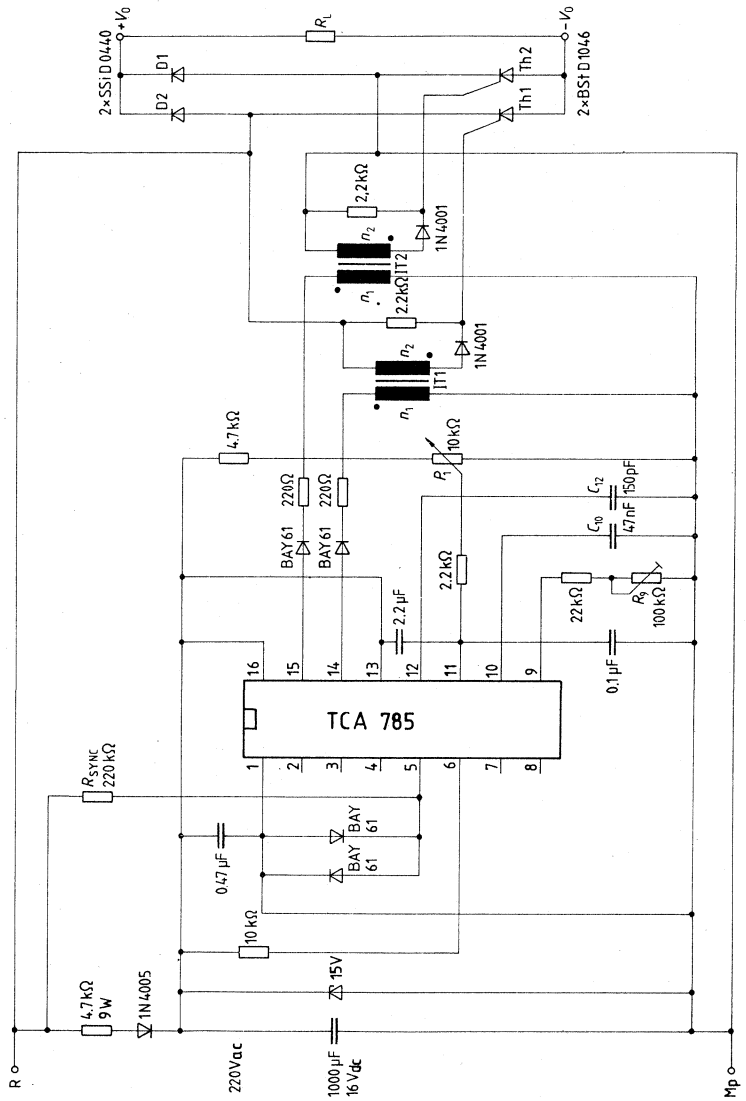


Shown is the possibility to trigger two antiparalleled thyristors with one IC TCA 785. The trigger pulse can be shifted continuously within a phase angle between 0° and 180° by means of a potentiometer. During the negative line half-wave the trigger pulse of pin 14 is fed to the relevant thyristor via a trigger pulse transformer. During the positive line half-wave, the gate of the second thyristor is triggered by a trigger pulse transformer at pin 15.

Half-Controlled Single-Phase Bridge Circuit with Trigger Pulse Transformer and Direct Control for Low-Power Thyristors



Half-Controlled Single-Phase Bridge Circuit with Two Trigger Pulse Transformers for Low-Power Thyristors



Type	Ordering Code	Package
TLE 3101	Q67000-A2337	P-DIP-18
TLE 3102	Q67000-A2338	P-DIP-14
TLE 3103	Q67000-A2339	P-DIP-14
TLE 3104	Q67000-A2340	P-DIP-8

These bipolar phase control ICs require, for most applications, only a minimum number of external components. Typical applications are motor control, brightness control, temperature control, cos φ optimization for squirrel-cage motors, and starting current limitation.

Thanks to their high efficiency, the TLE 310x ICs are particularly suitable for consumer goods, such as kitchen appliances and washing machines, vacuum cleaners, electric irons and hobbyist appliances.

A special feature is the soft start which requires only straightforward wiring, and is e.g. used in portable drills for center punching.

Features

- Direct supply from ac line possible
- Low power consumption, typically 2.4 mA
- Only one capacitor for trigger pulse width and phase angle
- Highly stabilized reference voltage
- Negative triac gate trigger current, 100 mA max.
- No triac drive pulses during supply undervoltage
- Optional voltage or current synchronization

- TLE 3101 with independent on-chip op amp OP and comparator K3

The following versions were produced from that basic IC:

- TLE 3102 without comparator K3
- TLE 3103 without op amp
- TLE 3104 without K3, enable input E/A, control input $V_{control}$, and without Z diode output.

These simplified versions are provided for less complex low cost applications.

Functional Description

The following is a description of the individual functional units (refer to block diagram) and their interactions:

Operational Amplifier op amp

Two inputs and the output are available. The op amp is internally compensated and has a push-pull output. Should the op amp not be required, the +input must be connected to ground (the TLE 3101 and TLE 3102 then consume minimum current).

Comparator K 3

Comparator K3 is not frequency-compensated. The output is an open NPN collector which in switching operation may drive an LED, for example. Should the comparator not be required, the −input must be connected to ground. K3 then has minimum current consumption.

Reference Voltage Source

A temperature-stabilized voltage source is available for control and regulating circuits.

Sawtooth Generator

In this unit, a sawtooth synchronized to the line is generated by the external R_S and C_S. The phase angle of the triac is determined by comparison of the sawtooth voltage and the control voltage. The trigger pulse width for the driver is provided by the falling edge of the sawtooth generator. The charge of C_S determines the trigger pulse width. A special circuit ensures the release of only one trigger pulse per line half period.

Comparators K1, K2

Sawtooth voltage and control voltage are compared by means of comparators K1 and K2. Comparator K2 receives only half the sawtooth voltage. The phase angle limit can be adjusted within the complete phase angle range by applying a reduced reference voltage to input "$V_{\varphi max}$". Comparator K2 provides starting current limitation and/or phase angle limitation for inductive loads. Both comparator outputs are fed to the logic and driver unit.

The comparator with the smaller conduction angle is the dominating one. With $V_{\varphi max}$ dominating, the trigger pulse width is doubled – compared with the trigger pulse width in case of a dominating $V_{control}$.

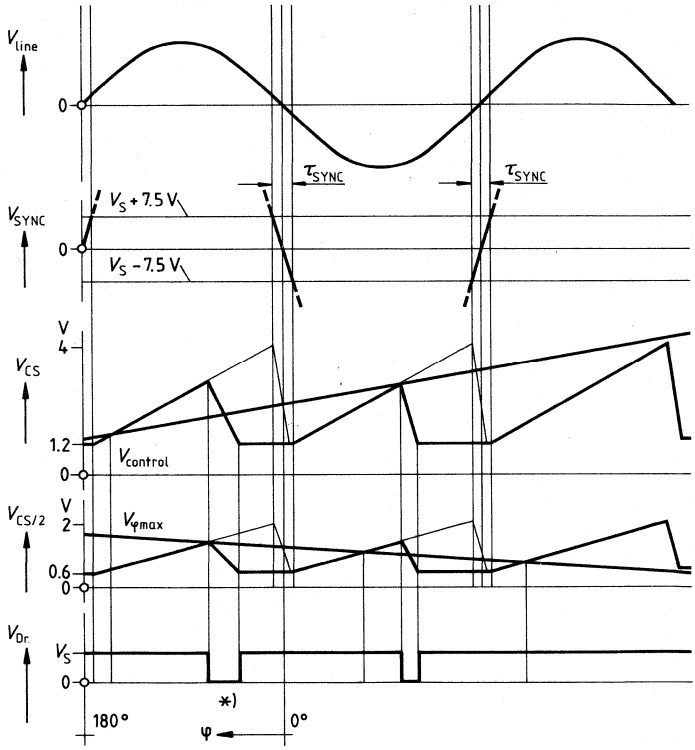
Logic + Driver

The logic and driver unit for triac triggering is controlled by comparators K1, K2, and the enable input E/A. The E/A input is TTL-compatible and may disable or enable the trigger pulse. Logic +driver obtain information on the trigger pulse width from the sawtooth. The undervoltage monitoring enables the driver output only if the IC's supply voltage has reached the permissible minimum value. The driver output to the triac supplies negative pulses.

Synchronization

At the sync input, the phase angle is synchronized to the zero crossing point of the line voltage. The sync pulse width τ_{SYNC} has to be twice as large as the trigger pulse width.

Pulse Diagram



Conduction angle (with resistive load)

*) With $V_{\varphi max}$ dominating, the trigger pulse width is doubled.

Maximum Ratings

$T_A = -25$ to $+85$ °C

Description	Symbol	min	max	Unit
Supply voltage	V_S	−0.3	33	V
Inputs op amp K3	V_I	−0.3	33	V
Output op amp	V_{Q1}	−0,3	V_S	V
	I_{Q1}	−5	3	mA
Output K3 (disabled)	V_{Q2}	−0.3	33	V
(enabled)	I_{Q2}	0	40	mA
Output V_{REF}	V_{REF}	−0.3	5	V
Z diode	I_Z	−35	35	mA
Input SYNC	I_{SYNC}	−10	10	mA
Input R_S	V_{RS}	−0.3	5	V
Input C_S	V_{CS}	−0.3	5	V
Input $V_{control}$	$V_{control}$	−0.3	V_S	V
Input $V\varphi_{max}$	$V\varphi_{max}$	−0.3	V_S	V
Enable input E/A	$V_{E/A}$	−0.3	33	V
Output driver (disabled)	$V_{Q\,dr}$	−0.3	33	V
(enabled)	$I_{Q\,dr}$	0	120	mA
Total power dissipation (time integral)	P_{tot}		700	mW
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance				
system – air P-DIP- 8 – TLE 3104	$R_{th\,SA}$		100	K/W
P-DIP-14 – TLE 3102, TLE 3103	$R_{th\,SA}$		70	K/W
P-DIP-18 – TLE 3101	$R_{th\,SA}$		70	K/W

Operating Range

Supply voltage	V_S	10	30	V
Ambient temperature	T_A	−25	85	°C
Input SYNC	I_{SYNC}	−3.5	3.5	mA

Characteristics

$V_S = 10$ to 30 V, $T_V = -25$ to $+85$ °C

Description	Symbol	Test conditions	min	typ	max	Unit
Current Consumption without output load at op amp, K3, driver, V_{REF}, without R_{SYNC} current	I_S	$V_S = 14.5$ V		2.4	3.2	mA
Reference voltage	V_{REF}		1.8	2.0	2.2	V
Load current	$-I_L$		0		3	mA
Stability $V_S = 10$ to 30 V	ΔV_{REF}				10	mV
$I_{REF} = 0$ to 3 mA	ΔV_{REF}				20	mV
Temperature coefficient	$\Delta V_{REF}/\Delta T$		−0.5		0.5	mV/K
Operational Amplifier op amp						
Open-loop voltage gain	G_{V0}		60	90		dB
Input offset voltage	V_{IO}		−10		10	mV
Input current	$-I_I$				2	µA
Common-mode input input voltage range	V_{IC}		0		$V_S - 3$	V
Output current	I_{Q1}		−3		1.5	mA
Transition frequency	f_T			2		MHz
Transition phase	φ_T			120		deg.
Output voltage	V_{Q1}		1.0		$V_S - 3$	V
Comparator K3						
Input current	$-I_I$				2	µA
Input offset voltage	V_{IO}		−20		20	mV
Output enabled	V_{Q2}	$I_{Q2} = 20$ mA		1.0	1.5	V
disabled	I_{Q2}	$V_{Q2} = 30$ V			5	µA
Common-mode input voltage range	V_{IC}		0		$V_S - 3$	V
Input K1 ($V_{control}$)						
Input current	$-I_S$				2	µA
Control range:						
Conduction angle = 0°				4		V
(dependent on R_S and C_S)						
Conduction angle = 175°				1.2		V
Max. perm. conduction angle					SYNC pulse end −5	deg.
Input K2 ($V\varphi_{max}$)						
Input current	$-I_S$				2	µA
Control range:						
Conduction angle = 0°				2		V
(dependent on R_S and C_S)						
Conduction angle = 175°				0.6		V
Max. perm. conduction angle					SYNC pulse end −5	deg.

Characteristics

$V_S = 10$ V to 30 V, $T_A = -25$ to $+85$ °C

Description	Symbol	Test conditions	min	typ	max	Unit
Z Diode						
Z voltage	V_Z	$I_Z = 5$ mA	13	14.5	16	V
Enable Input E/A						
Input current	$-I_I$				2	µA
H input voltage for driver output, active	V_{IH}		2.8			V
L driver output disabled	V_{IL}				0.8	V
Triac Trigger Output						
Output, enabled	V_L	$I_Q =$ 10 mA	1.4	2	2.5	V
		20 mA	1.4	2	2.5	V
		50 mA	1.4	2	3.0	V
		100 mA	1.4	4	6.0	V
Output, disabled	I_Q	$V_Q = 30$ V			10	µA
Input SYNC						
Switching current	I_{SYNC}			±20		µA
Switching threshold	V_{SYNC}			$V_S \pm 7.5$		V
Output disconnection at V_S undervoltage	V_S		7.5	8	10	V
Input R_S, C_S (refer to calculation formulae)						
Limit value C_S	C_S		5		100	nF
Limit value R_S	R_S		33			kΩ

Dimensioning notes and calculation formulae

1. Select trigger pulse width according to triac type and load.

2. **Calculate** C_S (for a $V_{control}$ domination)
   C_S (nF) = trigger pulse width (µs) x 0.2
   The formula yields the typical value
   e.g. T = 50 µs results in C_S = 10 nF

3. **Calculate** R_S (for 4 V max. sawtooth voltage)

$$R_S\ (k\Omega) = \frac{1}{\text{trigger pulse width } (\mu s)} \times 2 \times 10^4$$

   The formula yields the typical value
   e.g. T = 50 µs results in R_S = 400 kΩ

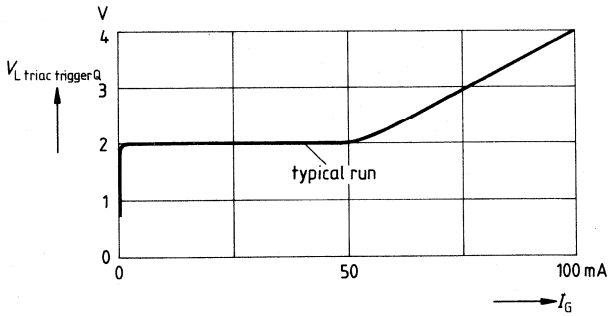
4. **Select R_{SYNC} resistance at SYNC input**
   The sync pulse width (from V_S ± 7.5 V, I_{SYNC} = ± 20 µA) has to be twice as large as the trigger pulse width.

4.1 Sync pulse width ≥ 2 x trigger pulse width x safety factor (according to component deviation and line voltage variation).

4.2 R_{SYNC} (kΩ) = [sync pulse width (µs) x line voltage (V rms) x 2.23×10^{-4} – 7.5] x 50
e.g. 560 µs sync pulse width and 220 V rms result in R_{SYNC} = 1 MΩ.
With 220 V rms line voltage, the minimum permissible resistance R_{SYNC} is 100 kΩ corresponding to a pulse width of 195 µs.

5. **Calculate** R_G

$$R_G = \frac{V_S - \text{triac gate voltage} - \text{low-voltage triac trigger output}}{I_G}$$



6. **Calculate** R_S

6.1 Calculation of R_S requires first of all the determination of the total current consumption. Insert the arithmetic mean values of the currents for one line cycle.

6.2 $\bar{I}_{tot} = \bar{I}_S = 3.2\ mA + \bar{I}(V_{ref}) \pm \bar{I}_{Q1}$ (OP) $+ \bar{I}_{Q2}$ (K3) $+ \bar{I}$(driver output) $+ \bar{I}$ (additional external circuit currents) $+ |\bar{I}|$ (R_{SYNC}).

6.3 $R_S\ (k\Omega) = \dfrac{\text{rms line voltage (V)}}{\bar{I}_{tot}\ (mA)} \times 0.455 \times$ safety factor

(corresponding to component deviation and line voltage variation)

e.g. $\bar{I}_{tot} = 5$ mA und $V_{line} = 220$ V result in $R_S = 20\ k\Omega$.

Employing the internal Z diode reduces the IC's V_S voltage to 14.5 V.

7. **Calculate** C_G

7.1 Selection of the maximum permissible ripple at the V_S input, based on the desired functional quality and the special external components.

7.2 The ripple amplitude at the V_S input of the unit should not exceed $V_{pp} = 2$ V.

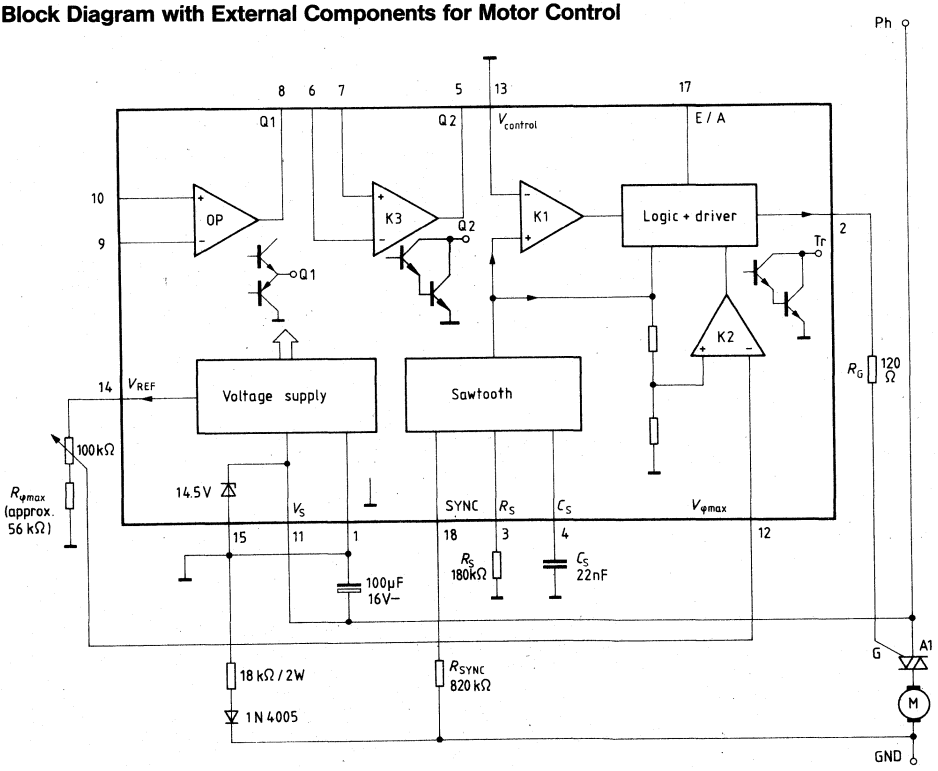
7.3 $C_G\ (\mu F) \geq \dfrac{\bar{I}_{tot}\ (mA)}{V_{pp}} \times 15$

e.g. ripple $V_{pp} = 0.75$ V; $\bar{I}_{tot} = 5$ mA results in $C_G = 100\ \mu F$

Pin Description for TLE 3101

Pin	Function	Pin	Function
1	Ground	10	+input op amp
2	Triac trigger output	11	V_S
3	R_S	12	$V_{\varphi max}$
4	C_S	13	$V_{control}$, K1
5	Output Q2, K3	14	V_{REF}
6	−input K3	15	Z diode
7	+input K3	16	N.C.
8	Output Q1, op amp	17	Enable input E/A
9	−input op amp	18	Synchronization input (SYNC)

Block Diagram with External Components for Motor Control

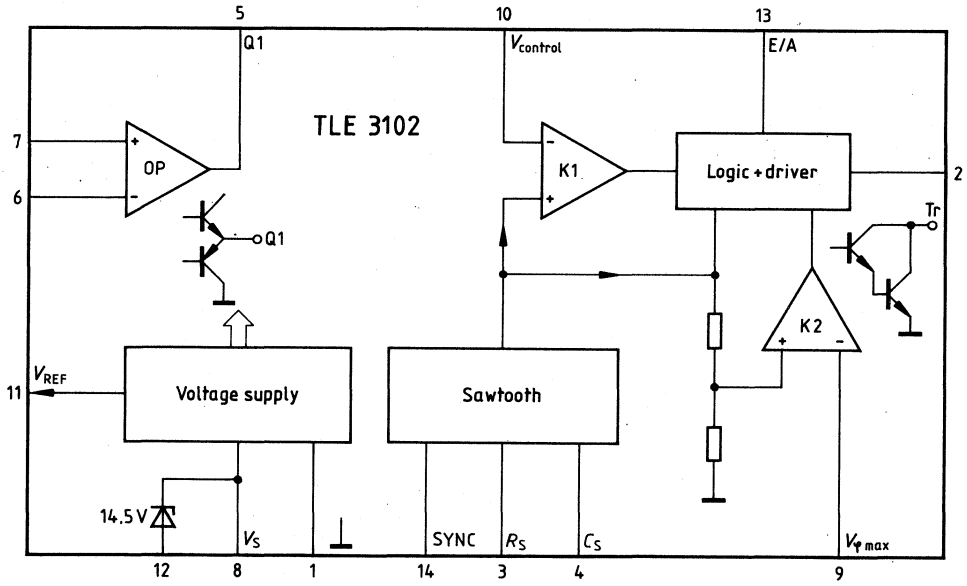


The **TLE 3102** with on-chip op amp for external use is particularly suitable as a speed controller with P, PI, or PID characteristic; the op amp serves as adjustable gain amplifier. An actual value which is proportional to speed can be formed by rectification of the tacho amplitude.

Pin Description

Pin	Function	Pin	Function
1	Ground	8	V_S
2	Triac trigger output	9	$V_{\varphi max}$
3	R_S	10	$V_{control}$, K1
4	C_S	11	V_{REF}
5	Output Q1, op amp	12	Z diode
6	−input op amp	13	Enable input E/A
7	+input op amp	14	Synchronization input (SYNC)

Block Diagram

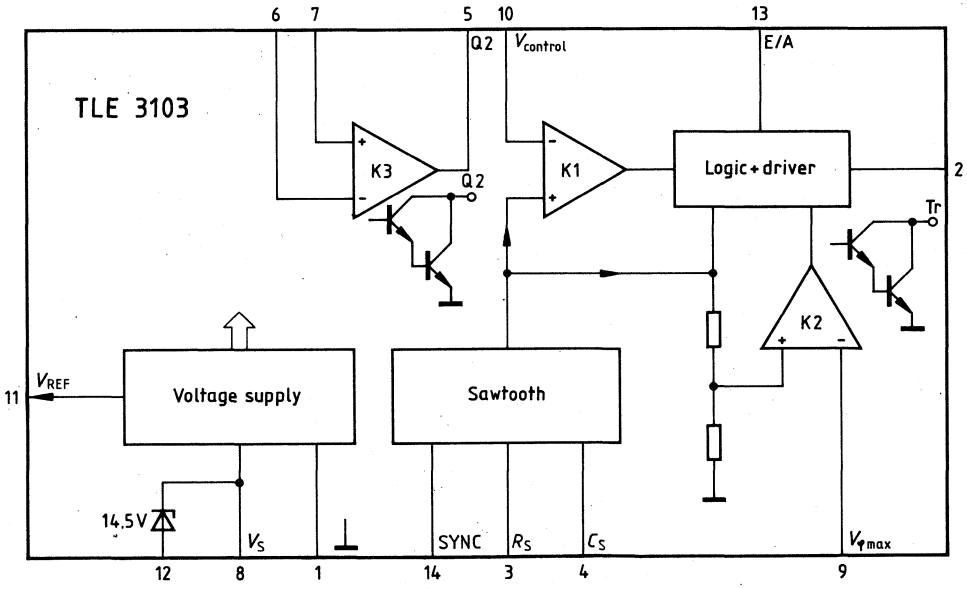


The **TLE 3103** with on-chip comparator for external use is particularly suitable for phase control systems in which special functions, such as blocking protection or overtemperature protection, are required.

Pin Description

Pin	Function	Pin	Function
1	Ground	8	V_S
2	Triac trigger output	9	$V\varphi_{max}$
3	R_S	10	$V_{control}$, K1
4	C_S	11	V_{REF}
5	Output Q2, K3	12	Z diode
6	−Input K3	13	Enable input E/A
7	+Input K3	14	Synchronization input (SYNC)

Block Diagram

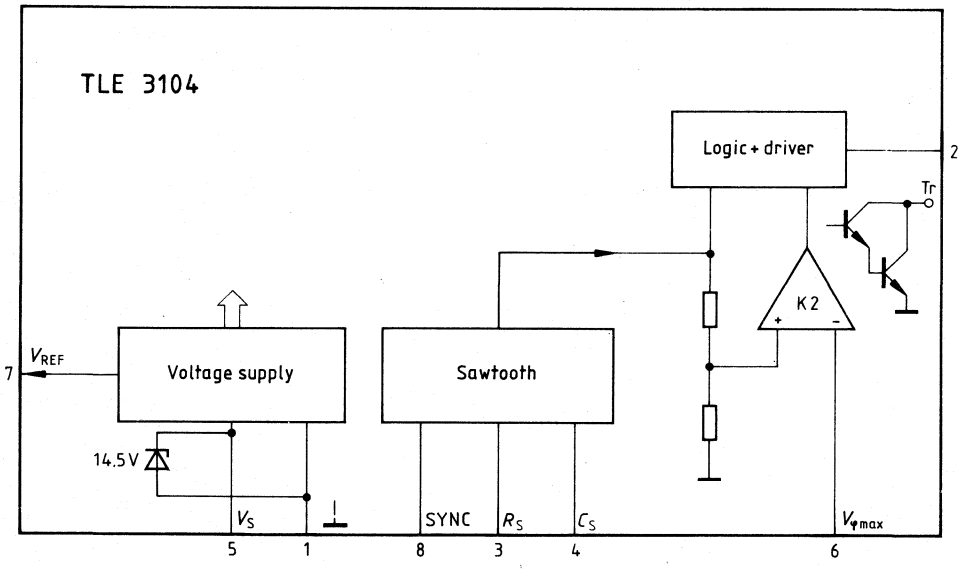


The **TLE 3104** is particularly suitable for simple, low-cost phase control and motor control systems, in which the actual value is formed by rectification of the tacho amplitude.

Pin Description

Pin	Function	Pin	Function
1	Ground	5	V_S
2	Triac trigger output	6	$V\varphi_{max}$
3	R_S	7	V_{REF}
4	C_S	8	Synchronization input (SYNC)

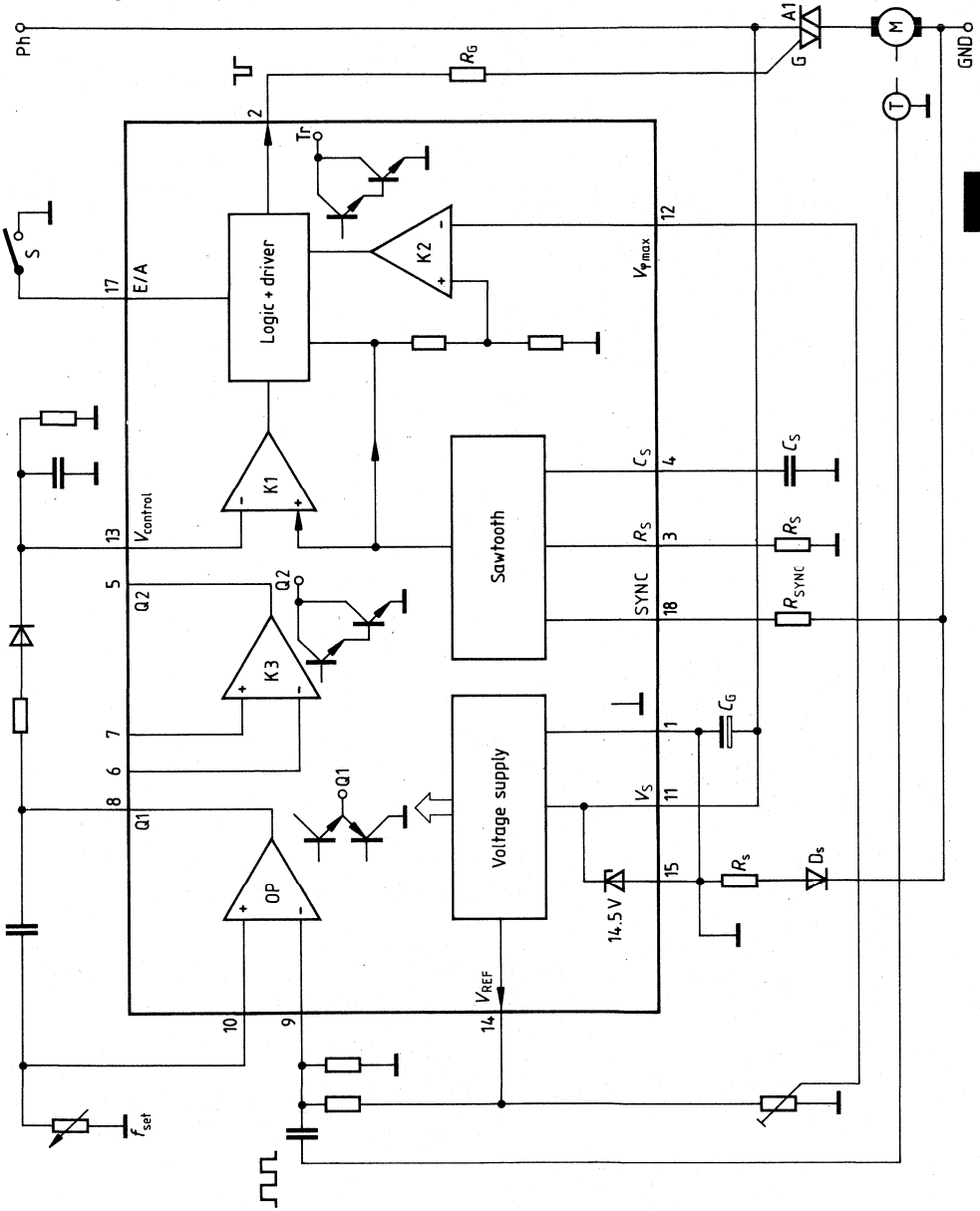
Block Diagram



Application Examples

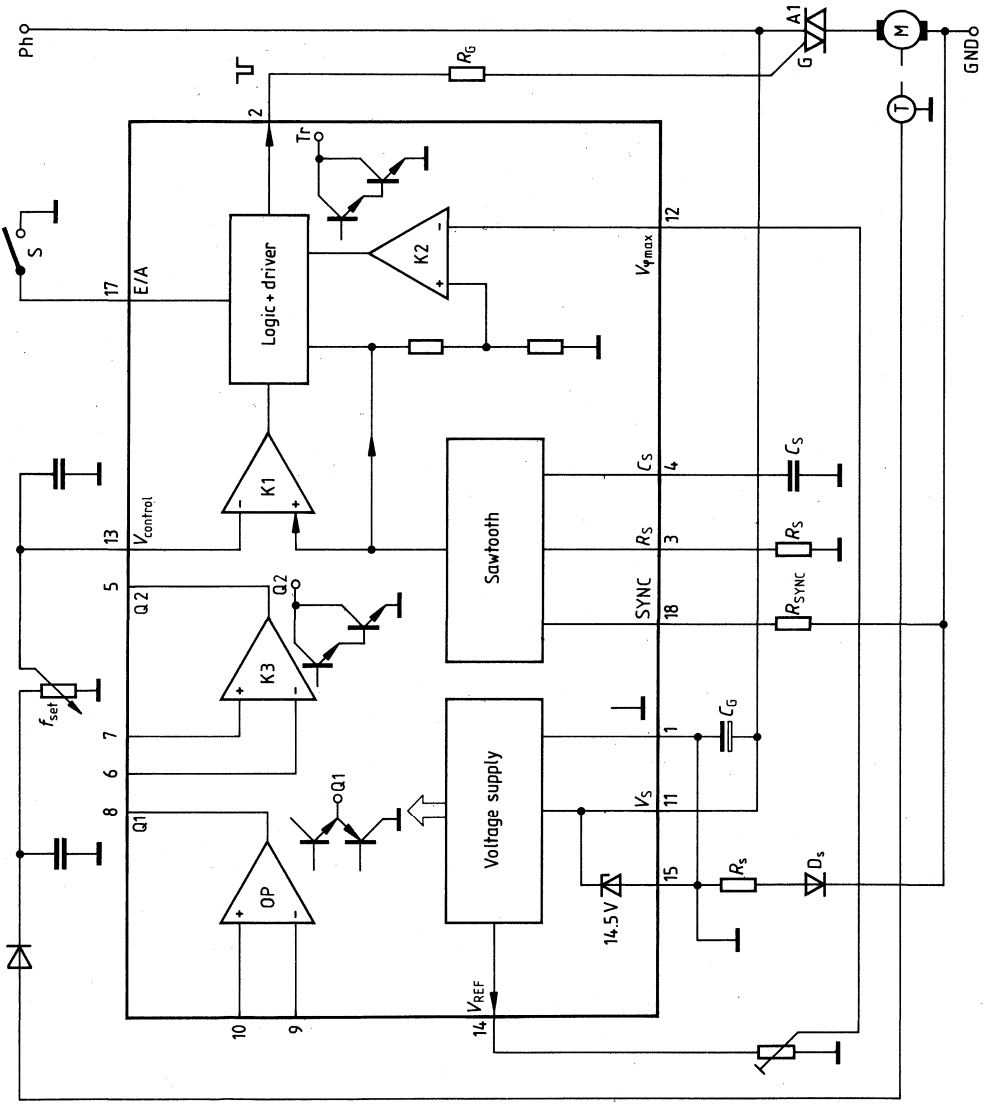
Schematic Circuit Diagram for Motor Control Using TLE 3101

The tachogenerator provides a **frequency** processed by the op amp (monoflop).

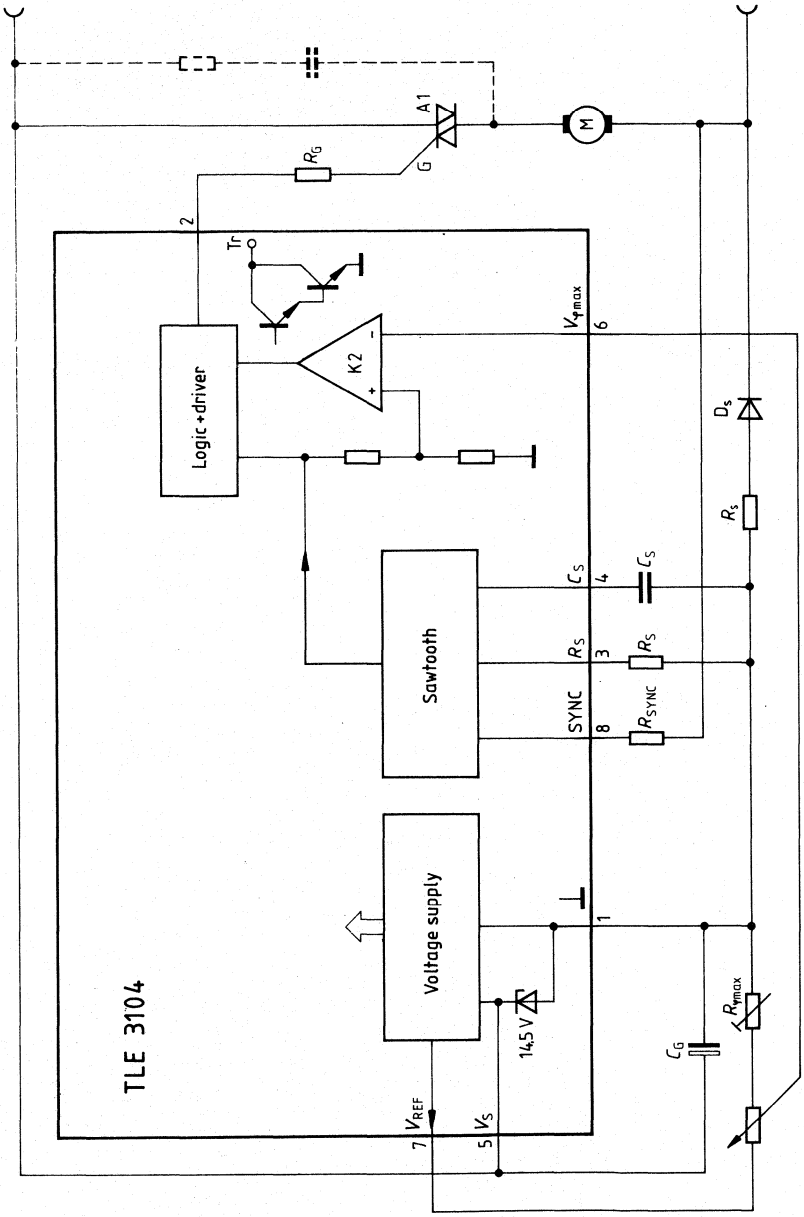


Schematic Circuit Diagram for Motor Control Using TLE 3101

The tachogenerator provides a **voltage** which is rectified and stabilized, and then fed to input $V_{control}$.

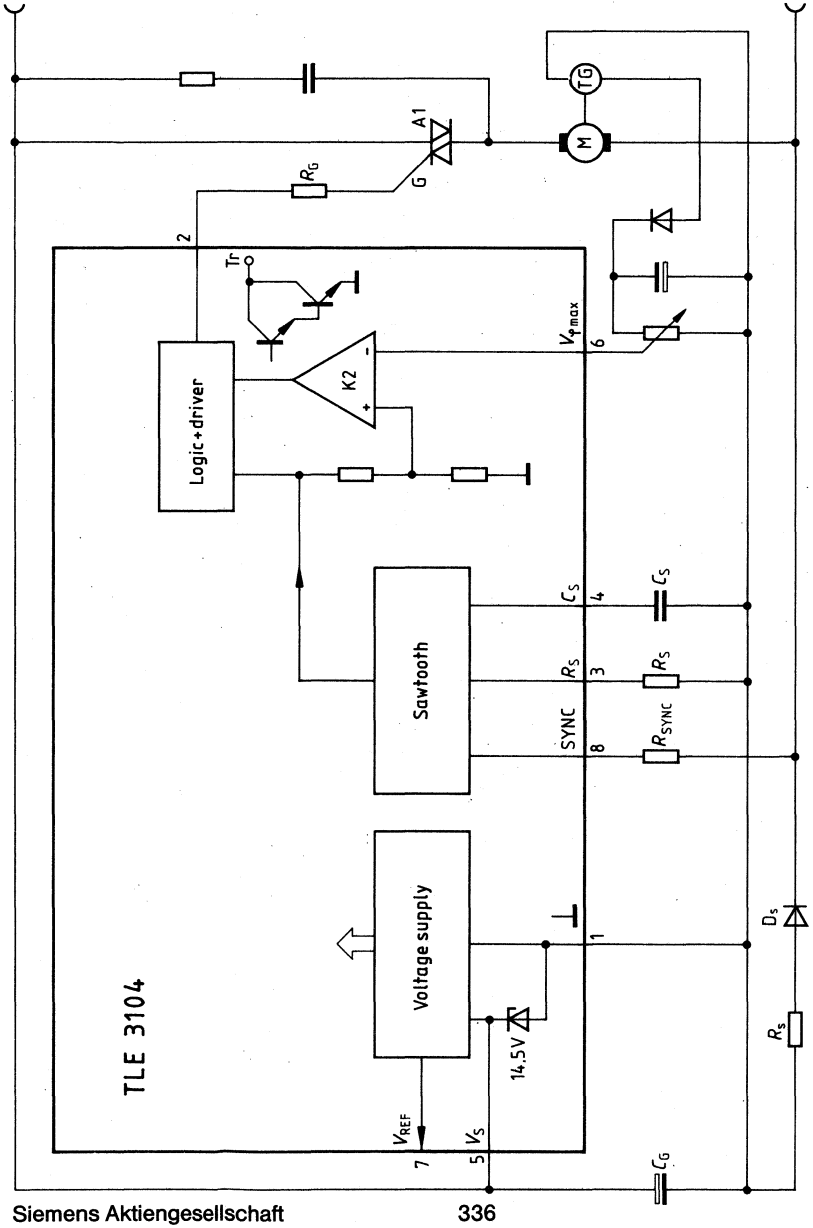


Schematic Circuit Diagram for Motor Control Using TLE 3104



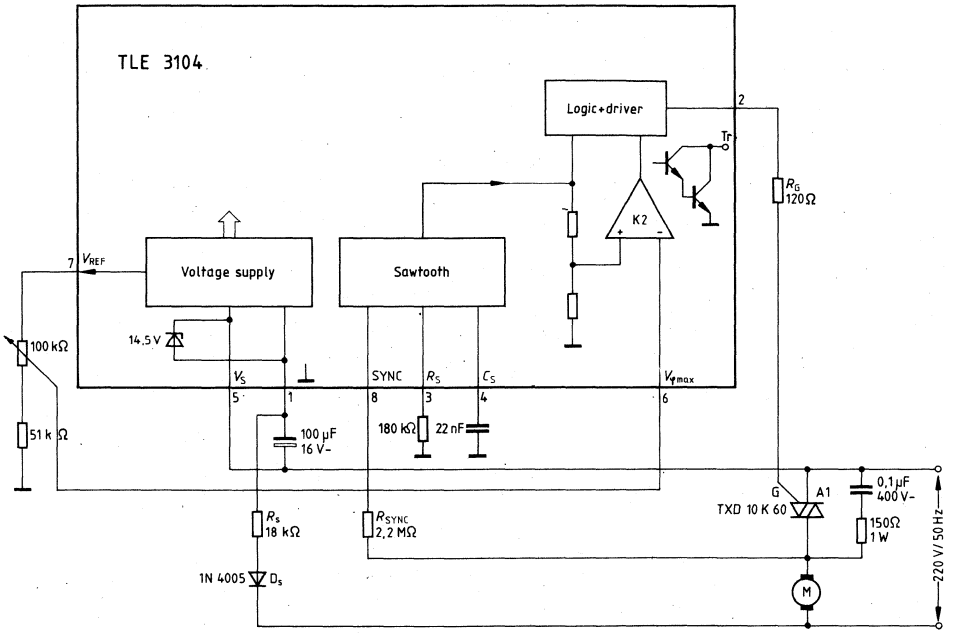
Schematic Circuit Diagram for Motor Control Using TLE 3104

The tachogenerator supplies a **voltage,** which is rectified and stabilized and then fed to input $V_{control}$



Current Synchronization in Case of Inductive Load Control Using TLE 3104

Particularly in case of phase control of inductive loads, such as transformers and shaded-pole motors, there is a risk of half-wave operation as a result of the phase shift between voltage and current. In order to avoid this condition, the synchronization resistor is connected to A 2 of the triac (this method cannot be applied in the event of severe brush sparking of the motor).



Notes

The pulse width selected for the trigger pulse must be so great that the triac reaches its holding current, even with a great phase angle (critical: positive half-wave). For this reason, it may be necessary to select a lower value for the ac line series resistor.

The sync pulse must be at least twice as wide as the trigger pulse (see also page 323 and page 327/para. 4).

Preliminary Data **CMOS IC**

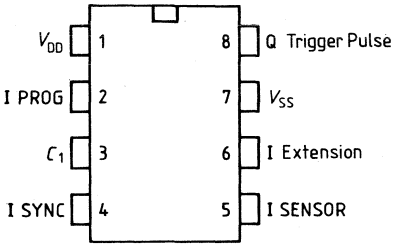
Typ	Ordering Code	Package
SLB 0586	Q67100-H8605	P-DIP-8

The IC SLB 0586, constructed in CMOS technology, permits the design of a digital, electronic dimmer. Turning on and off as well as the setting of the required brightness are carried out via a single sensor or via an equivalent extension input, respectively.
(The SLB 0586 replaces the S 576 A/B/C family of types).

Features

- Sensor operation – no mechanically moveable switching elements.
- Operation is also possible from several extensions by means of sensors or push-buttons.
- Can be interchanged with electromechanic wall switches in conventional light installations.
- Brightness control with a physiologically approximated linear characteristic.
- Very high interference immunity, also from ripple-control signals.
- Very few peripheral components.
- Programming input for optionally determining 3 dimmer versions (type A/B/C).
- "Soft start" with type A and C.

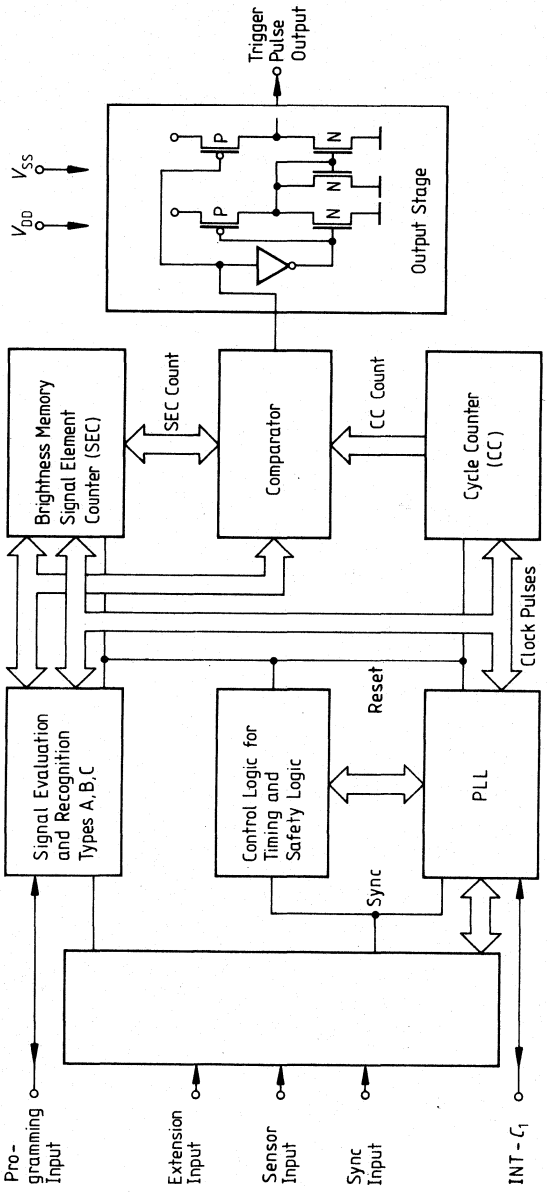
Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	V_{DD}	Reference point (0 V)
2	I PROG	Programming input
3	C_1	Integrator
4 5	I SYNC I SENSOR	Sync input Sensor input
6	I EXTENSION	Extension input
7	V_{SS}	Supply voltage
8	Q trigger pulse	Output trigger pulse

Figure 1
Block Diagram



Functional Description

The SLB 0586 permits the design of fully electronic dimmers for light bulbs (resistive loads) which are operated in each case via a single sensor.

In conventional lighting circuit installations it is possible to interchange this component with mechanic wall switches as well as to operate all functions from several switching points (extensions).

The brightness is set by phase control. Its digital logic is synchronized with the line frequency **(see block diagram, figure 1).**

It is possible to supply the IC via a two-wire-connection as the conduction angle is limited to a maximum of 152° of the half-wave.

Operation (see figure 2)

The integrated circuit can distinguish the instructions "turning ON/OFF" and "dimming" due to the duration of the control input operation.

Turning ON/OFF

Short touch (50 to 400 ms) of the sensor area turns the lamp on or off, depending on its preceding state. The switching process is activated at the end of touching.

Setting of the Brightness (Dimming)

If the sensor is touched for a longer period (> 400 ms), the conduction angle will be varied continuously. It runs across its control loop in 7.6 s (e.g. bright-dark-bright) and continues this sequence until the finger is removed from the sensor.

The following process is carried out to enable an easy operation also in the lower brightness range: the phase control angle is controlled such that during the run across the control loops the lamp brightness varies approximately physiological-linearly with the operating time, and rests for a short period when a minimum brightness is reached.

The conduction angle can be controlled in the half-wave range between 45° and 152° by means of the sync input circuitry (R_2, C_4) specified in the application example.

Control Behavior

The three dimmer versions A, B and C differ in their control behavior. Depending on the required function, the version is determined via the programming input (see characteristics).

Type A With turning on, the maximum brightness is always set; with dimming, control is started from the minimum brightness. With repeated dimming, control is carried out in the same direction (e.g. "brighter").

Type B With turning off, the selected brightness is stored and again set when the switch is turned on. Dimming starts at that stored value and the control direction is reversed with repeated dimming.

Type C With turning on, the maximum brightness is always set; with dimming, control is started from the minimum brightness. The control direction is reversed with repeated dimming.

Programming of the Different Versions

Type A: $V_{I2} = V_{SS}$ (L)

Type B: V_{I2} = open (tristate)

Type C: $V_{I2} = V_{DD}$ (H)

V_{I2} = Level at pin 2

Maximum Ratings

$V_{DD} = 0$ V (without external protective circuitry)

Description	Symbol	min	max	Unit
Supply voltage	V_{SS}	−7.5	0.3	V
Input voltage	V_I	V_{SS}−3	0.3	V
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Total power dissipation $T_A = 25$ °C			10	mW
Thermal resistance system – air	$R_{th\ SA}$		135	K/W

Operating Range

Supply voltage	V_{SS}	−4.8	−5.8	V
Ambient temperature	T_A	0	80	°C

Characteristics

$T_A = 25$ °C, $V_{SS} = -5$ V ($V_{DD} = 0$ V)

Description	Symbol	Test conditions	min	typ	max	Unit
Supply current	I_{SS}	$f_{SYNC} = 50/60$ Hz		0.45/0.46	0.6	mA
Supply current with missing sync signal	I_{SS}	$f_{SYNC} = 0$			0.45	mA
Input reverse current	I_I			0.5		nA
Input capacitance	C_I	$V_I = 0$ V, $f = 1$ MHz		5		pF

Sensor Input (Pin 5)

H input voltage	V_{IH}	with series resistor 10 MΩ from 220 V line	1/2 V_{SS}+1.1			V
L input voltage	V_{IL}				1/2 V_{SS}−1.1	V
Peak input current	I_{IH}			33	37	µA
HL transition time (trigger transition)	t_{THL}			line sine wave		
LH transition time	t_{TLH}					
Frequency with active signal	f	synchronized with 50/60 Hz clock at sync input		50/60		Hz

Extension Input (Pin 6)

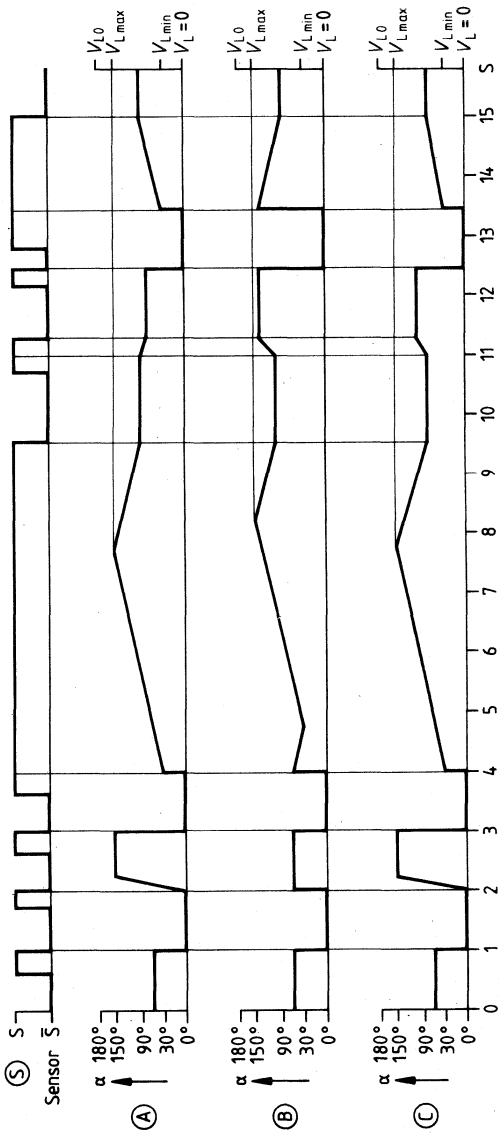
H input voltage	V_{IH}		1/2 V_{SS}+1.1			V
L input voltage	V_{IL}				1/2 V_{SS}−1.1	V
Input current	I_{IH}	V_{SS} −0.3 V (or V_{DD} +0.3 V)		0.5		µA

Characteristics

$T_A = 25\,°C$, $V_{SS} = -5\,V$ ($V_{DD} = 0\,V$)

Description	Symbol	Test conditions	min	typ	max	Unit
Sync Input (Pin 4)						
H input voltage	V_{IH}	with series resistor 1.5 MΩ from 220 V line and diode to V_{DD}	1/2 V_{SS}+1.1			V
L input voltage	V_{IL}				1/2 V_{SS}−1.1	V
Input current	$-I_{IH}$			207	240	µA
Input current	I_{IH}				20	µA
HL transition time (trigger transition)	t_{THL}			line sine		
LH transition time	t_{TLH}			wave		
Frequency	f			50/60		Hz
Programming Input (Pin 2)						
Input capacitance to V_{SS}	C_I			7		pF
Load capacitance through PCB with tristate Programming of different versions (see page 342)	C				7	pF
Integrator (Pin 3)						
Application circuit	C_5	compare with fig. 3	68	100	330	nF
	R_{10}		82	100	120	kΩ
Output (Pin 8)						
L output current	I_Q	$V_{SS} = -5\,V$ $V_{QL} = -3\,V$	25			mA
L pulse width	t_{QL}	50 Hz line			39.0	µs
		60 Hz line			32.6	µs
L output voltage	V_L			V_{DD}−0.6		V
HL transition time	t_{HLQ}				20	µs
LH transition time	t_{LHQ}				20	µs

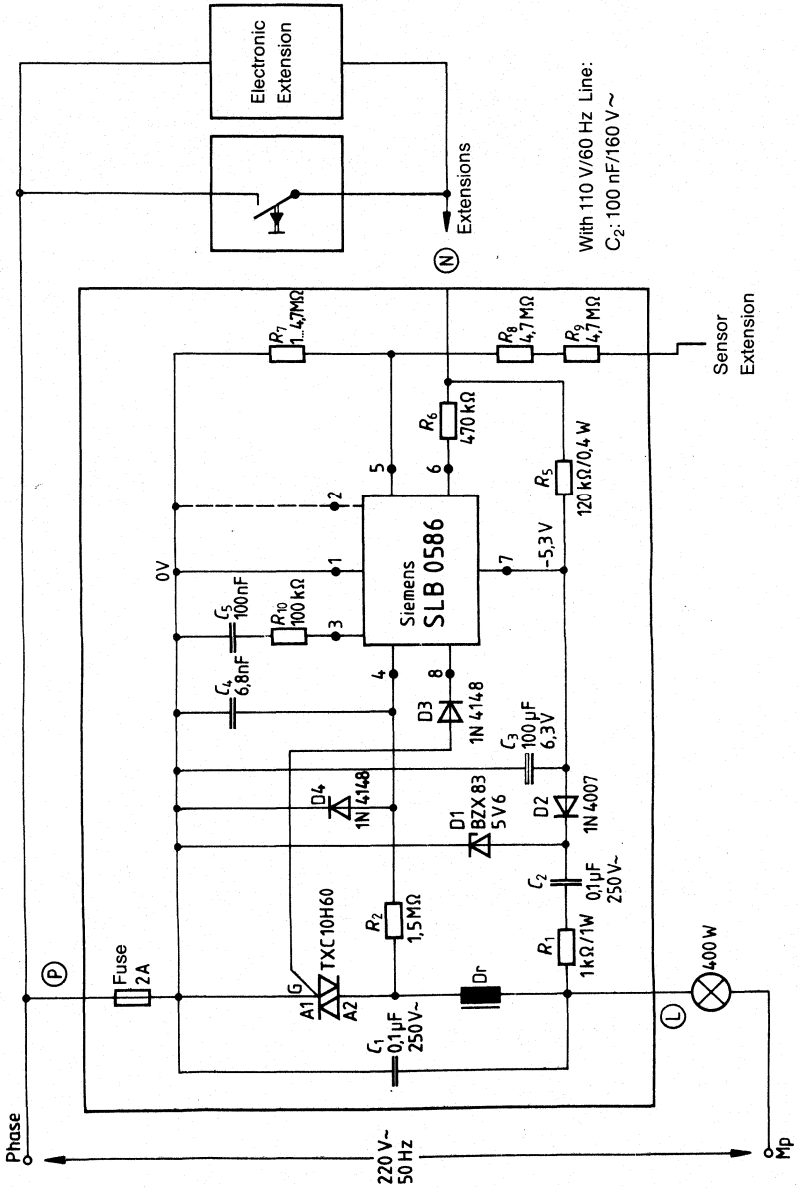
Figure 2
Control Behavior of the Different Versions
(schematic)



α Conduction Angle
V_L Lamp Voltage
S Control Signal : S Sensor touched
(=<0,4s, ->0,4s)
S̄ Sensor not touched

Turning on of type A and C is "soft", i.e. the brightness is controlled from 0 to maximum within 380ms.

Figure 3
Application Circuit SLB 0586

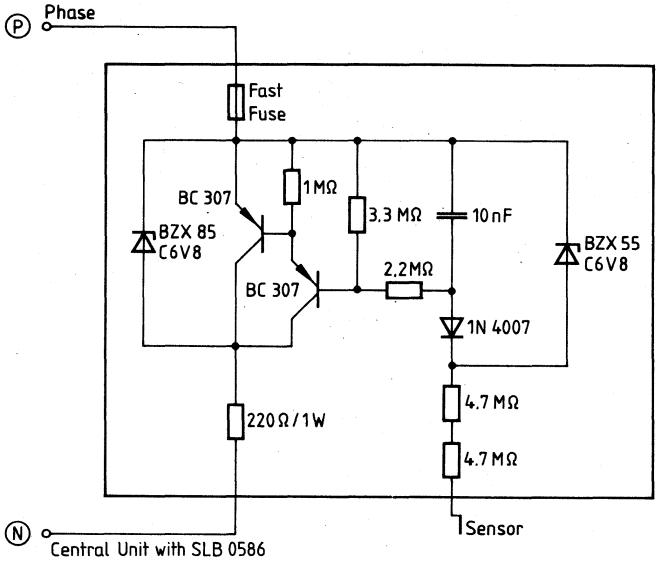


Description of the Application Circuit (see Figure 3)

The suggested circuit design of SLB 0586 performs the following functions

- Current supply for the circuit (R_1, C_2, D1, D2, C_3).
- Filtered signal for synchronization of the internal time base (PLL circuit) with line frequency (R_2, C_4).
  For specific applications C_4 can be increased up to 15 nF, however, only at the expense of the lamp brightness so that the lamp gets darker (control range shifts to the left).
- Integration unit for internal PLL circuit (C_5, R_{10}).
- Protection of the user (R_8, R_9)
- Sensitivity setting of the sensor (R_7)
- Current limitation in the case of reverse polarity of the extension (R_5, R_6)
  Both resistors can be omitted if no extension is connected. In this case, pin 6 must be interconnected with V_{SS} (pin 7).
- D3: reduction of positive voltages which may arise during the triggered state at the gate of some triacs, to values below $V_{DD}+0.3$ V (refer to maximum ratings). If suitable triacs are used, diode D3 can be omitted. (This feature of the triac depends on the anode current and on the internal resistance between G and A1, and can be measured and specified by the manufacturer).
- Dr: The choke and the capacitor C_1 are used for EMI suppression.
  Depending on the application, the EMI suppression is to be dimensioned in acc. with
  VDE 0875/part 1 (general)
  VDE 0550/part 6 (chokes)
  or corresponding to national regulations
  e.g. 1.4...2 mH, Q = 11...24.

Figure 4
Application Circuit: Electronic Extension



Wireless Remote Control

The connection of a wireless remote control to the extension is very easy. All functions of the SLB 0586 can be performed with the aid of a single transmission channel.

Interference Immunity

A digitally determined immunity period of approximately 50 ms ensures a high interference immunity against electrical variations on the control inputs, and additionally allows an almost delay-free operation.

Due to the special logic of the extension input, even large ground capacitances of the control line will not lead to interference.

In the case of short line interruption, the set switching state with the recommended external circuitry remains stored. After line interruptions for longer periods the circuit turns into the OFF-state.

The control characteristic of the line-synchronous oscillator (PLL circuit) is designed such that interference by ripple-control signals cause only slight changes in brightness. This does not cause a malfunction of the dimmer.

General Information

All stated time specifications refer to a line frequency of 50 Hz. In the case of a line frequency of 60 Hz, the periods are shortened accordingly.

Extensions

All switching and control functions can also be performed from extensions which are connected to an extension input reserved for this purpose. The central unit and the extensions are equivalent. Electronic sensor switches or mechanical pushbutton switches can be connected to the extensions. During operation, H potential must be applied to the extension input for both line half-waves.

An electronic circuit suitable for this purpose, is shown in the application example **(figure 4)**. The circuit operates as return delay and takes over the triggering of the switching transistors during the negative line half-wave.

- Response time approx. 2 ms
- Return delay time approx. 30 ms
- Protection against reverse polarity (R_1, D 1, Si)

Note

The extension input should be switched to V_{SS}, if the input is not used.

Operation of Control Inputs

Input potential during both the half-waves of the line phase

Function	Line half-wave	Sensor input	Extension input		
operated	positive	L	H		
	negative	0	H		
not operated	positive	H	L	or	0
	negative	0	0		L

A/D Converters; D/A Converters, High-Speed Data Acquisition

Selector Guide

Type	Package	Resolution Bit	Conversion time	Strobe frequency max MHz	Supply voltage V	Analog Multiplex	Linearity LSB
Ultra-Fast ADC							
SDA 6020	C-DIP-16	6	20 ns	50	+5, −5.2		± 1/2
SDA 5200	C-DIP-16	6	10 ns	100	+5, −5.2		± 1/2
SDA 8200	C-DIP-40	6	4 ns	300	+5, −4.5		± 1/4
SDA 8010	C-DIP-24	8	10 ns	100	+5, −4.5		± 1/2
µP-Compatible ADC							
SDA 0808 A; B	C-DIP-28	8	15 µs	1.5*)	5	8 x	± 1/2
SDA 0808 N	PL-CC-28	8	15 µs	1.5*)	5	8 x	± 1/2
SDA 1808 N	PL-CC-28	8	15 µs	2.5*)	5	8 x	± 1/2
SDA 0810 A; B	C-DIP-28	10	20 µs	1.5*)	5	8 x	± 1/2
SDA 0810 N	PL-CC-28	10	20 µs	1*)	5	8 x	± 1/2
SDA 1810 N	PL-CC-28	10	20 µs	2*)	5	8 x	± 1/2
DAC							
SDA 8005	C-DIP-16	8	7 ns	150*)	−5.2	–	± 1/2
High-Speed Data Acquisition							
SDA 8020	PL-CC-68	100 MHz/4 x 25 MHz shift register					

*) Clock frequency

Bipolar IC

Type	Ordering Code	Package
SDA 6020	Q67000-Y584	C-DIP-16

The SDA 6020 is an ultra-fast A/D converter with 6 bit resolution. In addition to a strobe frequency of 50 MHz and excellent linearity, it offers the following features:

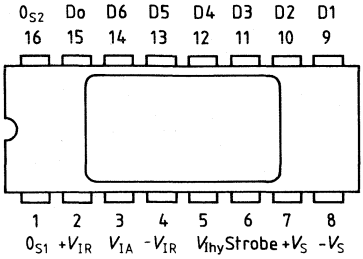
- Conversion up to Nyquist frequency (25 MHz)
- 6-bit resolution (1.6%), simple extension to 8 bits
- ± 1/4 LSB linearity
- No sample and hold required
- Dynamic driving of reference inputs for analog addition and multiplication
- ECL-compatible (ECL → TTL matching possible, e.g. with SH 100.255)
- Low power dissipation of 450 mW
- Logic-compatible supply voltage +5 V; −5.2 V

Maximum Ratings

Description	Symbol	min	max	Unit
Supply voltage	$+V_S$	−0.3	6.0	V
Supply voltage	$-V_S$	−6.0	0.3	V
Input voltages	$V_{I\,A}$, $+V_{I\,R}$ $-V_{I\,R}$	−3.0	3.0	V
Strobe	V_{Strobe}	$-V_S$	0	V
Hysteresis control	$V_{I\,hy}$	0	3.0	V
Voltage difference	$0_{S1} - 0_{S\,2}$	−0.5	0.5	V
Ambient temperature	T_A	0	70	°C
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance System – air	$R_{th\,SA}$		70	K/W

Pin Configuration

top view



Pin Description

Pin	Symbol	Function
1	0_{S1}	Digital ground
2	$+V_{IR}$	Positive reference voltage (< 2.5 V)
3	V_{IA}	Analog signal input (max. ± 2.5 V)
4	$-V_{IR}$	Negative reference voltage (> −2.5 V)
5	V_{Ihy}	Hysteresis control (0 V to +2.5 V)
6	Strobe	Strobe input (ECL)
7	$+V_S$	Positive supply voltage (+5 V)
8	$-V_S$	Negative supply voltage (−5.2 V)
9 to 14	D1 to D6	Data outputs, bits 1 to 6 (ECL)
15	D o	Overflow
16	0_{S2}	Digital ground of output stages

Characteristics

Description	Symbol	min	typ	max	Unit
Power supply					
Positive supply voltage	$+V_S$	4.5	5.0	5.5	V
Negative supply voltage	$-V_S$	−5.7	−5.2	−4.7	V
Current consumption					
at $+V_S = +5.0$ V; $V_{IA} \leq -V_{IR}$	I_S		30	60	mA
at $-V_S = -5.2$ V; $V_{IA} \leq -V_{IR}$	I_S		55	80	mA
Analog Section $T_A = 25\,°C$; $+V_S = 5$ V; $-V_S = 5.2$ V					
Signal Input					
Maximum input voltage	$V_{IA\,max}$	$-V_{IR\,min}$		$+V_{IR\,max}$	V
$V_{IA\,max} = \lvert(+V_{IR\,max}) - (-V_{IR\,min})\rvert$				5	V
V_{IA} for 6-bit resolution	V_{IA}		0.3		V
V_{IA} for 1/2 LSB linearity	V_{IA}	1.2	0.6		V
V_{IA} for 1/4 LSB linearity	V_{IA}	2.4	1.2		V
Input current					
at $V_{IA} = +V_{IR}$ in sample mode	I_{IA}		200	800	µA
at $V_{IA} < -V_{IR}$ in sample mode	I_{IA}	−10		10	µA
$-V_{IR} < V_{IA} < +V_{IR}$ in hold mode	I_{IA}	−10		10	µA
Input capacitance					
at $V_{IA} < -V_{IR}$	C_{IA}			35	pF
Reference Input					
Positive reference voltage	$+V_{IR}$	−2		2.5	V
Negative reference voltage	$-V_{IR}$	−2.5		2	V
Reference resistance	64 R	96	128	256	Ω
Digital Section					
Strobe Input					
H input voltage	V_{IH}	−1.1	−0.9	−0.6	V
L input voltage	V_{IL}	−2.0	−1.7	−1.5	V
H input current	I_{IH}	5	30	100	µA
L input current	I_{IL}	5	30	100	µA
Data Outputs 100 Ω to −2 V					
H output voltage	V_{QH}	−1.1	−0.9	−0.6	V
L output voltage	V_{QL}	−2.0	−1.7	−1.5	V

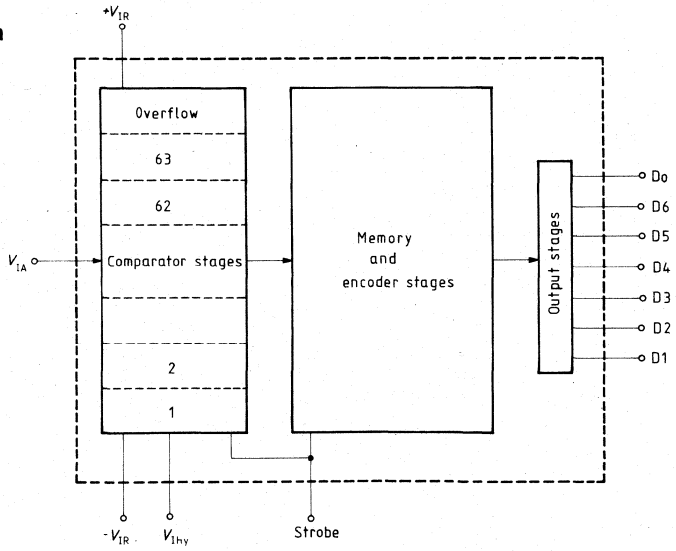
Description	Symbol	min	typ	max	Unit
Dynamic Parameters					
Aperture time	t_D		2		ns
Aperture jitter			25		ps
Strobe	t_{strobe}		8	10[1])	ns
Signal transition time[2])	$t_{TLH\ Qmax}$		9		ns
Signal transition time[2])	$t_{THL\ Qmin}$		11		ns
Strobe frequency	f_{strobe}	50			MHz

1) Exceeding this value at strobe frequencies of less than 50 MHz is quite permissible as long as the remaining hold time is adequate for reliable data transfer.

2) The data transfer into the following circuit should occur with a delay t_D referred to the rising strobe edge in the range:

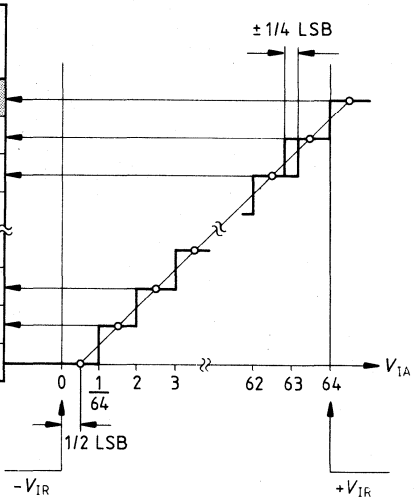
$$t_{TLH\ Qmax} + t_{hold/2} < t_D < t_{hold} + t_{THL\ Qmin}$$

Block Diagram

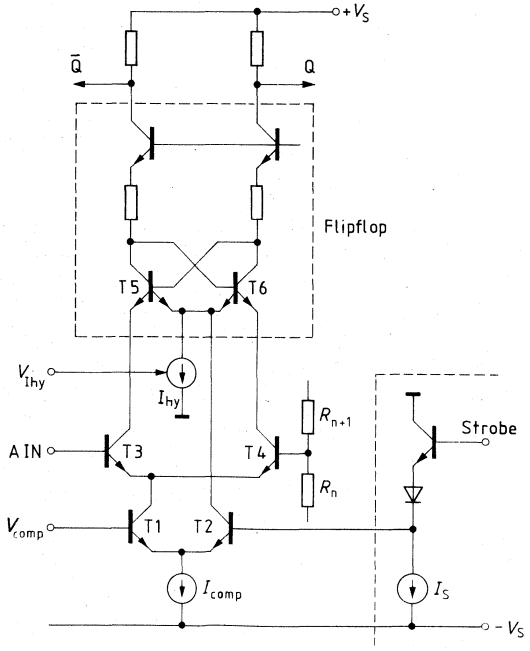


Transfer Characteristic and Truth Table

Do	D6	D5	D4	D3	D2	D1
H	L	L	L	L	L	L
L	H	H	H	H	H	H
L	H	H	H	H	H	L
≈						≈
L	L	L	L	L	H	L
L	L	L	L	L	L	H
L	L	L	L	L	L	L

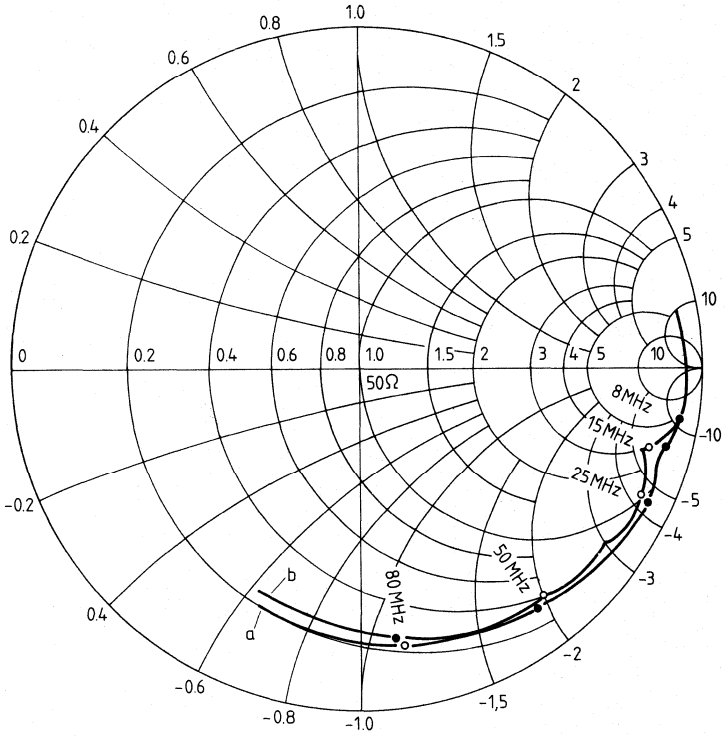


Input Stage

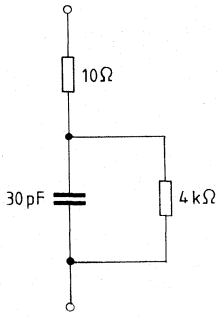


Smith Diagram

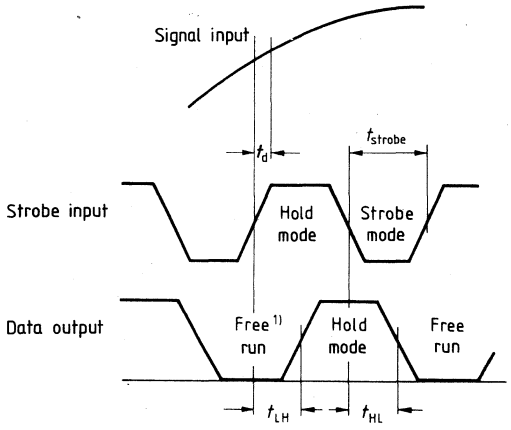
a) Nyquist plot of input impedance
b) Nyquist plot of equivalent circuit



Equivalent Circuit

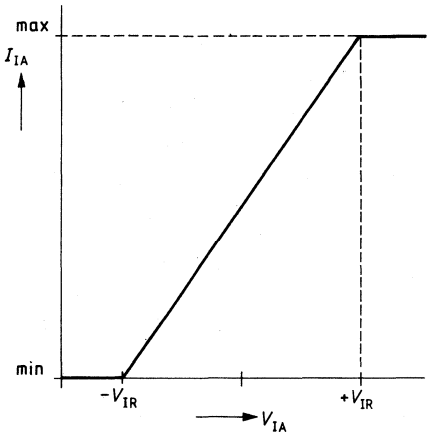


Pulse Diagram of Strobe Input and Data Outputs

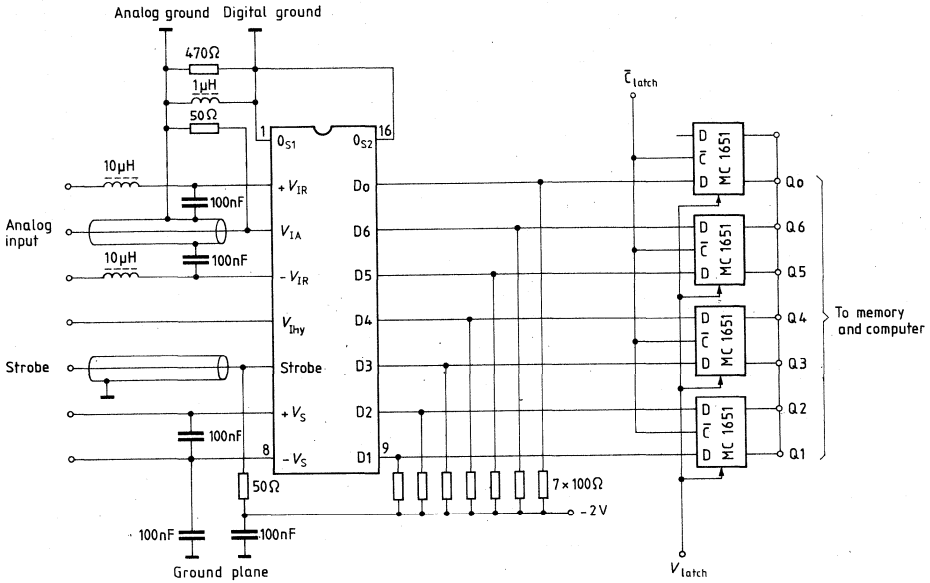


1) undefined output levels

Input Current versus Input Voltage



Measurement Circuit



Bipolar IC

Type	Ordering Code	Package
SDA 5200 N	Q67000-A2242	C-DIP-16
SDA 5200 S	Q67000-A2243	C-DIP-16
SDA 5200 AN	Q67000-A8231	C-DIP-16
SDA 5200 AS	Q67000-A8232	C-DIP-16

The SDA 5200 is an ultrafast A/D converter with 6 bit resolution and overflow output. After cascading, it enables straightforward construction of 7 or 8 bit A/D converters, respectively (refer to application circuit).

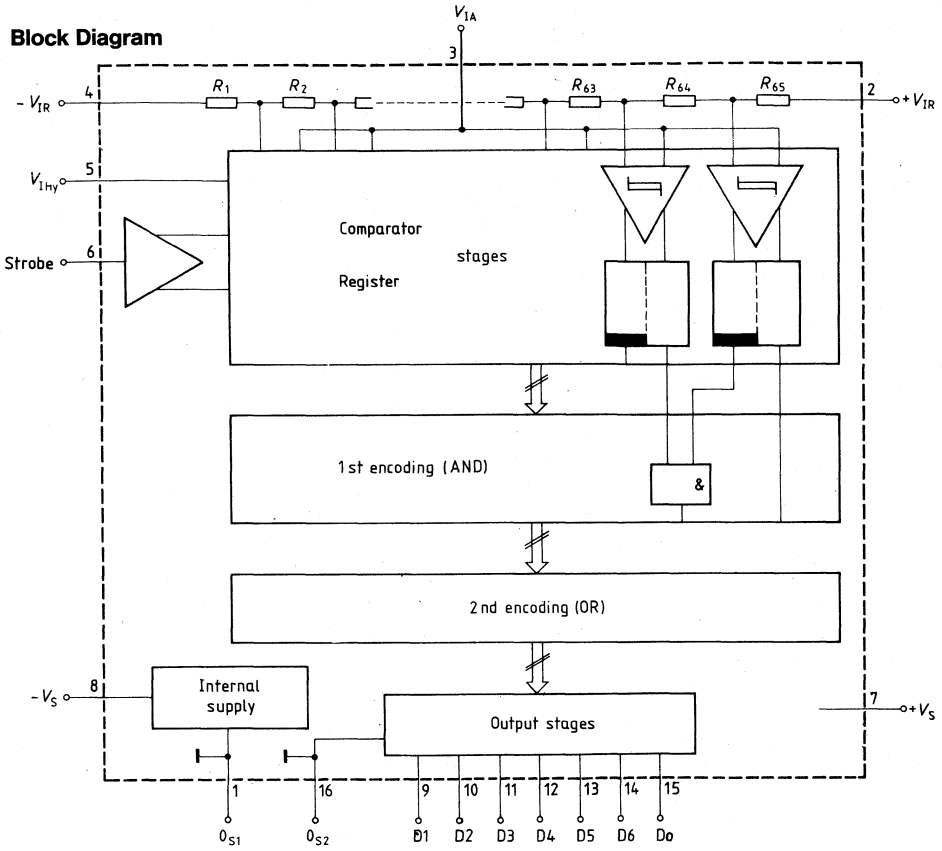
Apart from a guaranteed strobe frequency of 100 MHz or 75 MHz (A version) and an excellent linearity, the SDA 5200 is outstanding for a broad analog bandwidth which – from the analog side – enables application up to the limit of the Nyquist theorem.

The SDA 5200 is pin-compatible with the SDA 6020.

Features

- Strobe frequency 100 MHz or 75 MHz (A version)
- 6 bit resolution (1.6%)
- Overflow output (7th bit) at simultaneous blocking of the remaining outputs (SDA 5200 N; AN), thus simple cascading for 7 bit or 8 bit A/D converters
- Broad analog bandwidth (140 MHz)
- High slew rate of the input stages (typ. 0.5 V/ns)
- Processing of analog signals up to the Nyquist limit
- Linearity ± 1/4 LSB
- No sample and hold required
- Dynamic driving of reference inputs for analog addition and multiplication
- Power dissipation 550 mW
- ECL compatible
- Logic-compatible supply voltage +5 V; −5.2 V

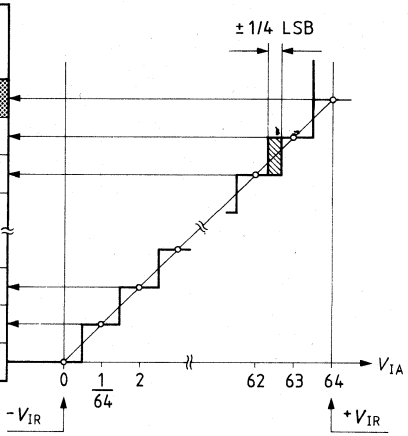
Block Diagram



Transfer Characteristic and Truth Table

SDA 5200 N, SDA 5200 AN

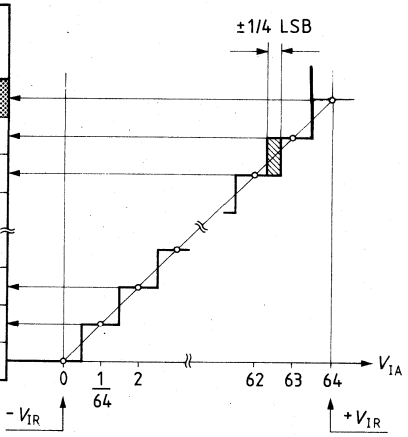
Do	D6	D5	D4	D3	D2	D1
H	L	L	L	L	L	L
L	H	H	H	H	H	H
L	H	H	H	H	H	L
L	L	L	L	L	H	L
L	L	L	L	L	L	H
L	L	L	L	L	L	L



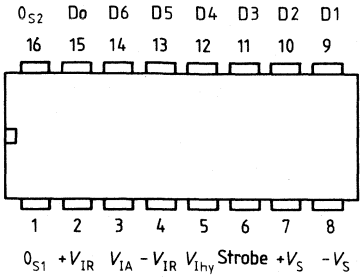
Transfer Characteristic and Truth Table

SDA 5200 S, SDA 5200 AS

Do	D6	D5	D4	D3	D2	D1
H	H	H	H	H	H	H
L	H	H	H	H	H	H
L	H	H	H	H	H	L
L	L	L	L	L	H	L
L	L	L	L	L	L	H
L	L	L	L	L	L	L



Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	0_{S1}	Digital ground 1
2	$+V_{IR}$	Positive reference voltage (+2 V)
3	V_{IA}	Analog signal input (max. +2 V; −3 V)
4	$-V_{IR}$	Negative reference voltage (−3 V)
5	V_{Ihy}	Hysteresis control (0 V to +2.5 V)
6	Strobe	Strobe input (ECL)
7	$+V_S$	Positive supply voltage (+5 V)
8	$-V_S$	Negative supply voltage (−5.2 V)
9 to 14	D1 to D6	Data outputs, bits 1 to 6 (ECL)
15	D o	Overflow output
16	0_{S2}	Digital ground 2

Maximum Ratings

Description	Symbol	min	max	Unit
Supply voltage	$+V_S$	−0.3	6.0	V
Supply voltage	$-V_S$	−6.0	0.3	V
Input voltages	$V_{I\,A} + V_{I\,R}, -V_{I\,R}$	−3.5	2.5	V
Strobe	V_{strobe}	$-V_S$	0	V
Hysteresis control	$V_{I\,hy}$	0	3.0	V
Voltage difference	$0_{S1} - 0_{S2}$	−0.5	0.5	V
Ambient temperature	T_A	0	70	°C
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance System – air	$R_{th\,SA}$		70	K/W

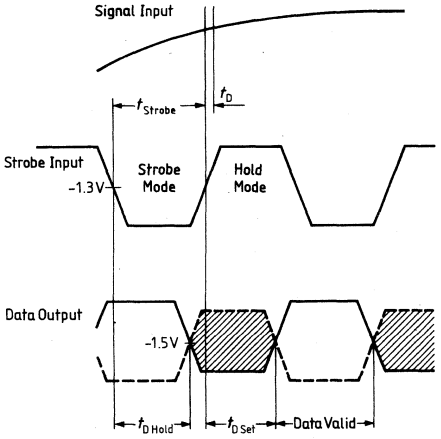
Characteristics

Description	Symbol	min	typ	max	Unit
Power Supply					
Pos. supply voltage	$+V_S$	4.5	5.0	5.5	V
Neg. supply voltage	$-V_S$	−5.7	−5.2	−4.7	V
Current consumption					
at $+V_S = +5.0$ V, $V_{I\,A} \leq -V_{I\,R}$	I_{S+}		50	80	mA
at $-V_S = -5.2$ V, $V_{I\,A} \leq -V_{I\,R}$	I_{S-}		55	80	mA
Analog Section					
Signal Input					
Max. input voltage	$V_{I\,Amax}$	$-V_{I\,Rmin}$		$+V_{I\,Rmax}$	V
$V_{I\,Amax} = \lvert(+V_{I\,Rmax}) - (-V_{I\,Rmin})\rvert$				5	V
$V_{I\,A}$ for 6 bit resolution			0.3		V
$V_{I\,A}$ for 1/2 LSB linearity		1.2	0.6		V
$V_{I\,A}$ for 1/4 LSB linearity		2.4	1.2		V
Input current					
at $V_{I\,A} = +V_{I\,R}$	$I_{I\,A}$		150	500	µA
at $V_{I\,A} < -V_{I\,R}$	$I_{I\,A}$	−500		500	nA
Input capacitance					
at $V_{I\,A} < -V_{I\,R}$	$C_{I\,A}$		25		pF
Reference input					
Pos. reference voltage	$+V_{I\,R}$	−2,5		2	V
Neg. reference voltage	$-V_{I\,R}$	−3.0		1.5	V
Reference resistance	R_{REF}	96	128	195	Ω

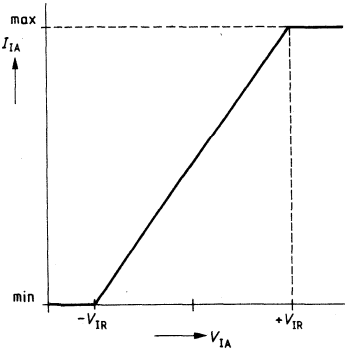
Characteristics (cont'd)

Description	Symbol	min	typ	max	Unit
Digital Section					
Strobe Input					
H input voltage	V_{IH}	−1.1	−0.9	−0.6	V
L input voltage	V_{IL}	−2.0	−1.7	−1.6	V
H input current	I_{IH}		6	50	µA
L input current	I_{IL}		6	50	µA
Data Outputs 100 Ω to −2 V					
H output voltage	V_{QH}	−1.1	−0.9	−0.7	V
L output voltage	V_{QL}	−2.0	−1.7	−1.5	V
Dynamic Parameters					
Aperture time	t_D		2		ns
Aperture Jitter			25		ps
Strobe	t_{strobe}		5		ns
Signal transition time SDA 5200 N; S	$t_{D\,Hold}$		12	17	ns
Signal transition time SDA 5200 AN; AS	$t_{D\,Hold}$		13	20	ns
Signal transition time SDA 5200 N; S	$t_{D\,Set}$		12	17	ns
Signal transition time SDA 5200 AN; AS	$t_{D\,Set}$		14	20	ns
Max. strobe frequency SDA 5200 N; S	f_{strobe}	100			MHz
Max. strobe frequency SDA 5200 AN; AS		75	80		MHz
Max. slew rate	SR		0.5		V/ns
Bandwidth (−3 dB)	B		140		MHz

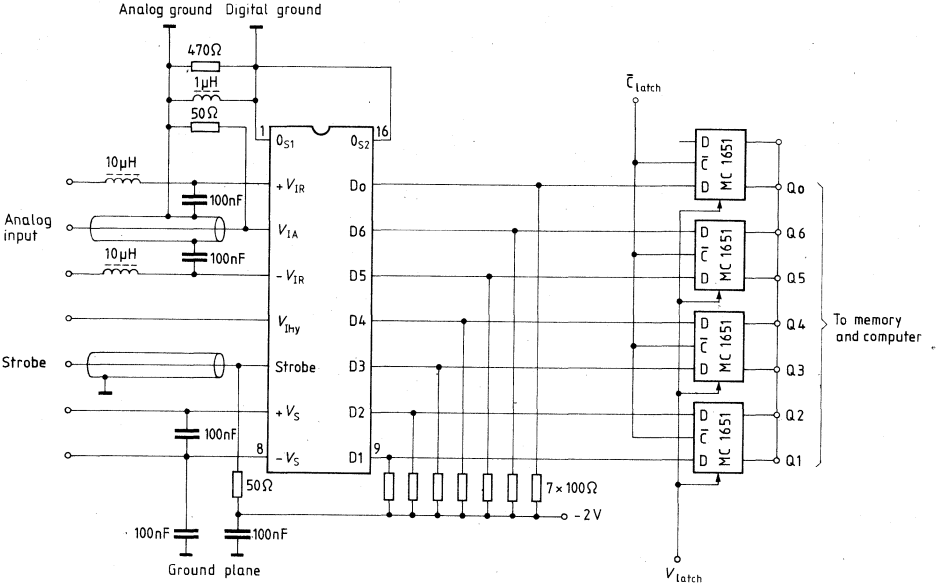
Pulse diagram of strobe input and data outputs



Input current versus input voltage

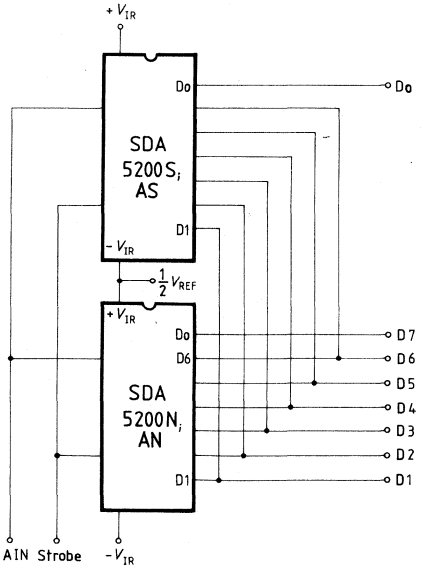


Measurement Circuit



Application Circuit

7 bit A/D converter with SDA 5200 S; AS and SDA 5200 N; AN



Preliminary Data **Bipolar IC**

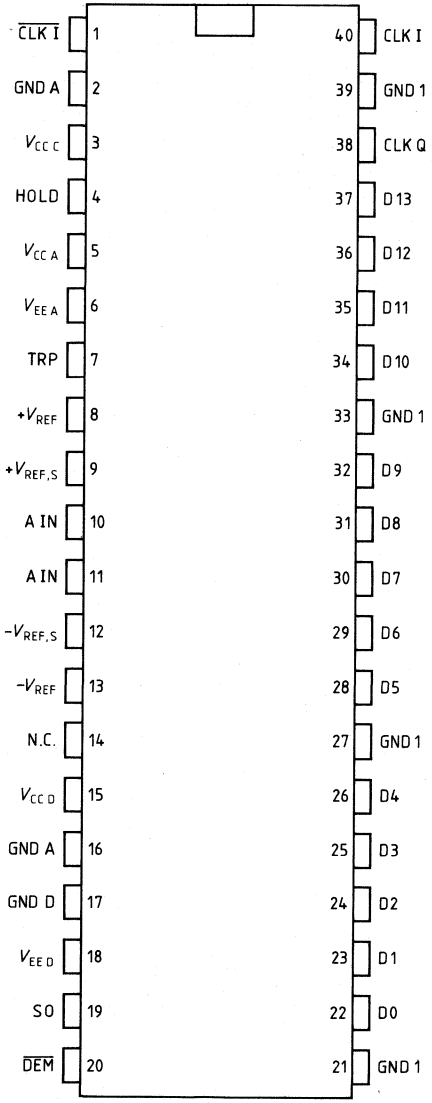
Type	Ordering Code	Package
SDA 8200	Q67000-A8164	C-DIP-40

The SDA 8200 is an ultrafast A/D converter operating according to the parallel principle with a resolution of 6 bits, a guaranteed clock frequency of 300 MHz and high performance up to 150 MHz full scale input.

Features

- 300 MHz conversion rate
- 5.4 effective bits ($f_{analog} = 100$ MHz)
- ± 0.25 LSB max. linearity error
- ± 1 V input voltage range
- 12 pF input capacitance
- Optionally 2:1 demultiplexed output data
- No pipelining in "Transparent Mode"
- Data ready clock output
- Overflow output

Figure 1
Pin Configuration
(top view)



Pin Description

Pin	Name	Symbol	Function
10, 11	Analog input	A IN	Input for the signal to be digitalized. To lower parasitic inductance two pins are used for this input.
13, 12 8, 9	Reference inputs	$-V_{REF}$ $-V_{REF,S}$ $+V_{REF}$ $+V_{REF,S}$	Bottom and top of the reference-resistor string. GThe inputs may either be used as sense and force for a Kelvin connection or connected in parallel to minimize parasitic resistance.
40, 1	Conversion clock	CLK I, $\overline{\text{CLK I}}$	Every rising edge of a signal applied to CLK I initiates sampling of the analog signal. Either ECL (differential or single-ended) or sinewave clock inputs may be used.
38	Clock output	CLK Q	Provides an ECL signal which can be used to control the transfer of the digital outputs into subsequent circuits (not available in the transparent mode). In the demultiplexing mode the frequency of CLK Q is half the sampling frequency (see "Modes of Operation").
22, 23 24, 25 26, 28 29	Output word 1	D0...D6	ECL outputs including overflow bit (D6) valid only in the demultiplexing mode. In this mode every first digital word of a pair of subsequent samples is delivered with a clock rate of half the sampling frequency. In the direct modes these outputs are undefined.
30, 31 32, 34 35, 36 37	Output word 2	D7...D13	ECL outputs (D13 overflow) delivering the second word of a pair in the demultiplexing mode. In the direct modes the digital data at these outputs appear with a clock rate equal to the sampling rate.

Pin Description (cont'd)

Pin	Name	Symbol	Function
19	Set Overflow	SO	A logic H at this ECL input or strapping the pin to GND D causes the overflow bit to be H and the data bits to be L when the analog signal exceeds the uppermost comparator threshold. If the pin is not connected or L is applied the data bits remain H in case of overflow.
20	Demultiplexing	$\overline{DEM}$	Setting this pin to H or strapping it to GND D sets the device in the direct mode.
7	Set transparent	TRP	A logic H (or GND D) at this input sets the device in the transparent mode (no pipelining). In this mode both DEM and HOLD inputs become ineffective. Besides, no clock output is provided.
4	Hold	HOLD	H active ECL input that immediately stops data transfer to the outputs (D0...D13) and inhibits the clock output. The last data word remains at the output and CLK Q is forced Low. In the direct mode the first valid output data together with the output clock appear one clock cycle after HOLD is released. In the demultiplexing mode clock and valid data appear after two conversion clock cycles with the first data word (corresponding to the first sampled value after HOLD is set to L) always present on D0...D6. HOLD is inactive in the transparent mode.
5, 6, 2, 16,	Analog supply	$V_{CC\,A}$, $V_{EE\,A}$, GND A	} Supply voltages
15, 18, 17,	Digital supply	$V_{CC\,D}$, $V_{EE\,D}$, GND D	
3	Clock supply	$V_{CC\,C}$	
21, 27 33, 39	Output ground	GND 1	Return path for the emitter-follower current in the ECL output stages.

Circuit Description

The A/D conversion is carried out in an array of 64 comparators connected in parallel to the analog input A IN. The signal is compared simultaneously with 64 equally spaced reference voltages provided by the resistor string $R_1 \ldots R_{65}$. With the rising edge of the conversion clock CLK I the result of the comparison is stored in the first comparator latch and afterwards passed to the second latch in a pipelining operation. Then the digital result of the comparison is pending at the comparators' output in a so-called thermometer code. Three subsequent encoding stages form the binary representation of the sampled value and a demultiplexer optionally divides the 300-MHz output data stream into two 150-MHz channels which are converted to ECL levels by two parallel output driver blocks. All clock signals for the pipelining and demultiplexing stages are formed internally by a clock driver circuit connected to the external conversion clock via CLK I. A clock signal for transferring the output data into subsequent circuitry is provided at CLK Q. If, however, the pipelined operation is disadvantageous (e.g. in subranging converter applications), all internal latches following the comparators may be set transparent via the programming input TRP. So any encode command directly causes the appearance of the respective output data after a short delay.

Clock Input (CLK I)

The clock inputs are designed to be driven differentially with ECL levels **(figure 3a).** Since CLK I is internally biased to −1,32 V, it is also possible to use CLK I single-ended. With this configuration a bypass capacitor from CLK I to GND C is recommended.

In this case the clock has to be stable with regard to the internal reference voltage to ensure the specified timing ($t_{WH,\ CLK\ I}$, $t_{WL,\ CLK\ I}$) over the operating range. For a continuously applied input clock the configuration shown in **figure 3b** is recommended. A capacitively coupled sinewave clock input (300 V_{pp} typ.) can then be employed without degradation in performance **(figure 3c)**.

Analog and Reference Inputs

The input voltage range is determined by the voltages applied to the top ($+V_{REF}$) and bottom ($-V_{REF}$) of the resistor string. Two pins for each voltage allow a Kelvin connection (sense, force) if very high precision is required. Otherwise the parallel connection of these pins ensures low parasitic resistances. The analog input can be driven from a customary 50 Ω source since the input capacitance is a very low 12 pF, independent of input voltage, and the input voltage range may be set symmetric to ground.

Supply System

The supply system breaks down into three parts. The analog supply $V_{CC\ A}$, $V_{EE\ A}$ is connected to the first comparator stages, the digital supply $V_{CC\ D}$, $V_{EE\ D}$ serves for encoding, demultiplexer and output stages, and a special clock supply $V_{CC\ C}$ is provided to separate the high and noisy driver currents from the other supply systems. Additionally, a separate return path for the currents of the output emitter followers is established via GND 1.

Modes of Operation

The analog signal is sampled with every rising edge of the clock signal CLK I. By programming the TRP and DEM inputs three different output modes can be chosen:

a) Direct modes (figure 4):

The output data appear at the outputs D7...D13 with a word rate equal to the sampling rate. The logic state of the outputs D0...D6 is not defined.

One of two submodes can be chosen:

(I) Normal Mode (TRP low, DEM high)
Due to internal pipelining the output data appear one clock cycle after the rising edge of CLK I (sampling moment). CLK Q delivers a clock signal with the same frequency as CLK I.

(II) Transparent Mode (TRP high)
After a sampling command the associated output data appear directly with a delay of less than 7 ns. No output clock is available.

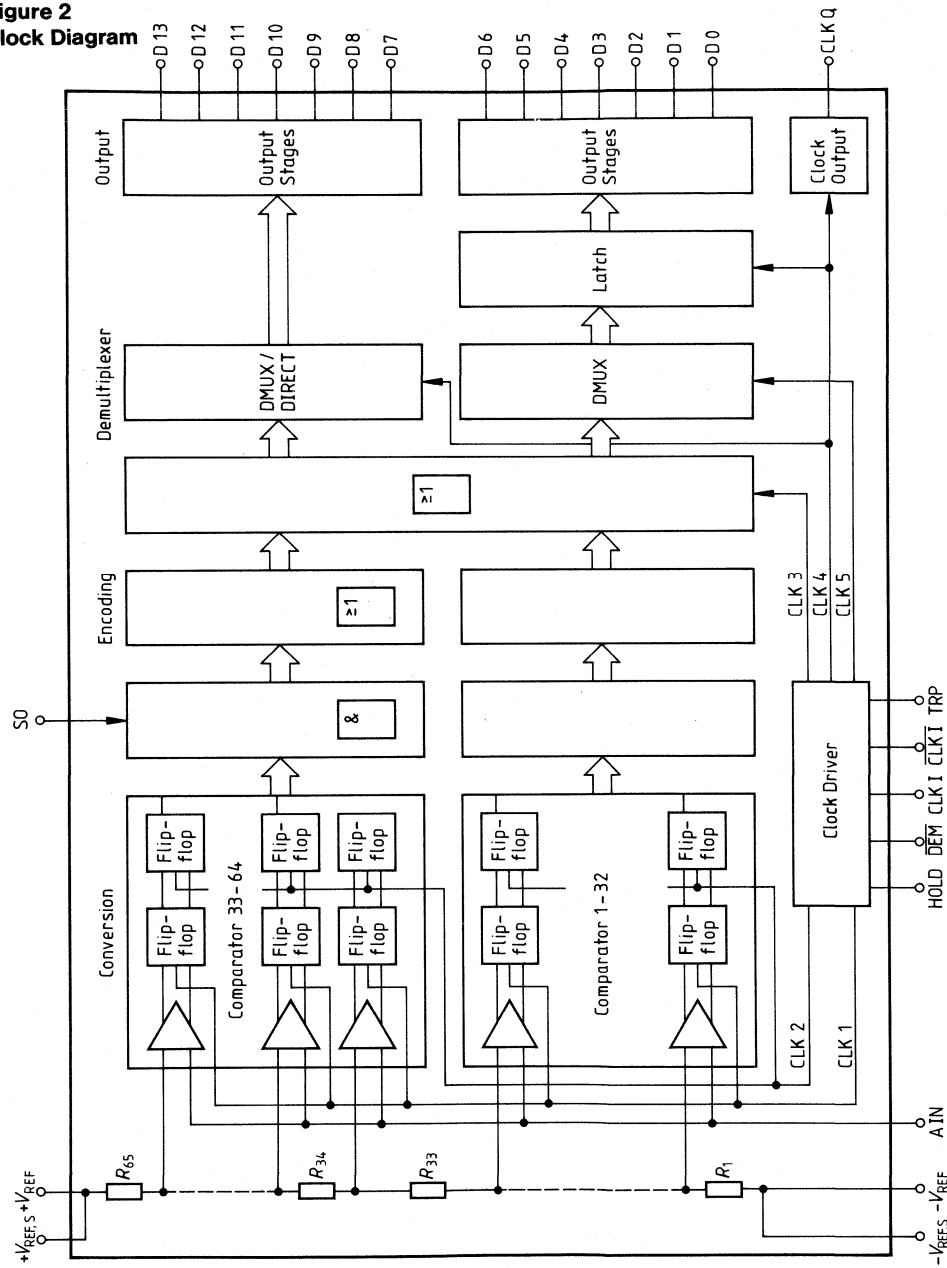
b) Demultiplexing mode (TRP low, DEM low; figure 5)

The output words corresponding to two subsequent samples appear simultaneously at the outputs D0...D6 and D7...D13, respectively, with half the clock rate of the conversion clock CLK I. After a HOLD pulse the word belonging to the first sample is always shown at D0...D6 and the delay between the first sample and output is two cycles of the conversion clock CLK I. At CLK Q a clock signal with half the frequency of the conversion clock, synchronous to the output data, is provided.

In all modes the output format in the overflow status can be programmed via the SO input. Setting SO to H causes the overflow bits (D6 and D13, respectively) to remain H and the data bits (D0...D5 and D7...D12, respectively) to go to L when the analog signal exceeds the threshold of comparator 64. If SO is set to L or not connected all data and overflow bits remain H in case of overflow **(figure 6).**

The HOLD input allows the output digital data stream to be stopped and restarted with defined output conditions. It is disabled in the transparent mode.

Figure 2
Block Diagram



Maximum Ratings

Description	Symbol	min	max	Unit
Pos. supply voltages	$V_{CC\,A}$ $V_{CC\,D}$ $V_{CC\,C}$	−0.3	6.0	V
Neg. supply voltages	$V_{EE\,A}$ $V_{EE\,D}$	−6.0	0.3	V
Analog input voltages	$+V_{REF}$ $-V_{REF}$ V_{AIN}	−2.5[1]	1.5	V
Digital input voltages	V_{CLKI} $V_{\overline{CKLI}}$ V_{DEM} V_{SO} V_{TRP}	−3.0	0.3	V
Output current	$I_{D0}\,...\,I_{D13}$		20	mA
Junction temperature	T_j		125	°C
Ambient temperature (without heat sink)	T_A	−25	50	°C
Storage temperature	T_{stg}	−40	125	°C
Thermal resistance Junction – ambient (without heat sink)	$R_{th\,JA}$		45	K/W

[1]) Reference voltages below −2 V must not be applied without the negative supply voltage.

Characteristics

$V_{CC\,A}$, $V_{CC\,D}$, $V_{CC\,C} = 5\ V \pm 5\%$, $V_{EE\,A}$, $V_{EE\,D} = -4.5\ V \pm 5\%$,
$T_j = 25\,°C$ to $125\,°C$

Description	Symbol	min	typ	max	Unit
Supply					
Pos. supply currents	$I_{VCC\,A}$		50		mA
	$I_{VCC\,D}$		65		mA
	$I_{VCC\,C}$		35		mA
Total pos. supply current	I_{CC}			170	mA
Neg. supply currents	$I_{VEE\,A}$		45		mA
	$I_{VEE\,D}$		125		mA
Total neg. supply current	I_{EE}			180	mA
Power dissipation	P_D		1.5	1.8	W
Permissible supply voltage difference	ΔV_{CC}, ΔV_{EE}			100	mV
Analog Section					
Signal input					
Voltage range	V_{AIN}	−2		1	V
Max. input current $V_{AIN} = +V_{REF}$	I_{AIN}		500	700	µA
Input capacitance	C_I		12		pF
Reference Inputs					
Reference voltages[1])	$+V_{REF}$, $-V_{REF}$	−2		1	V
Reference resistance	R_{REF}		120		Ω
Temperature coefficient of reference resistor	TC		1.7		10^{-3}/K
Digital section					
Logic Levels					
H input voltage[2])	V_{IH}	−1.165			V
L input voltage[2])	V_{IL}			−1.475	V
H output voltage[3]) $R_L = 100\ \Omega$	V_{QH}	−1.025		−0.88	V
L output voltage[3]) $R_L = 100\ \Omega$	V_{QL}	−1.810		−1.620	V
Clock Inputs[4])					
Input current	I_{CLKI}			20	µA
Max. clock frequency	$f_{c,\,max}$	300	350		MHz
Aperture delay	t_A		1		ns
Hold time	$t_{WH,\,CLKI}$	1.2			ns
Strobe time	$t_{WL,\,CLKI}$	1.2			ns

[1]) $+V_{REF}$ has to be more positive than $-V_{REF}$.
[2]) applies to DEM, SO, HOLD, TRP
[3]) applies to CLKQ, D0...D13
[4]) see "Circuit Description"

Characteristics

$V_{CC\,A}$, $V_{CC\,D}$, $V_{CC\,C} = 5\ V \pm 5\%$, $V_{EE\,A}$, $V_{EE\,D} = -4.5\ V \pm 5\%$,
$T_j = 25\,°C$ to $125\,°C$

Description	Symbol	min	typ	max	Unit
Programming Inputs[1])					
H input current	I_{IH}		80		µA
L input current	I_{IL}		60		µA
Hold Input					
Setup time	$t_{S,\,HOLD}$	0.5			ns
Release time	$t_{r,\,HOLD}$	2			ns
High pulse width	$t_{W,\,HOLD}$	1			ns
Data Outputs[2])					
Data valid range					
normal mode $f_c = 250$ MHz	$t_{V,\,N}$	3	3.5		ns
transparent mode $f_c = 250$ MHz	$t_{V,\,T}$	2.5			ns
demultiplexing mode $f_c = 300$ MHz	$t_{V,\,D}$	5	5.8		ns
Output delay					
normal mode	$t_{d,\,N}$	0.5			ns
transparent mode	$t_{d,\,T}$			9	ns
demultiplexing mode	$t_{d,\,D}$	0			ns
Clock Output					
Max. frequency[3])	$f_{Q\,max}$		250		MHz
Clock delay LH	t_{dLH}		6		ns
Clock delay HL	t_{dHL}		5.5		ns

[1]) applies to DEM, SO, HOLD, TRP
[2]) applies to CLK Q, D0...D13
[3]) see "Circuit Description"

Characteristics

$V_{CC\,A}$, $V_{CC\,D}$, $V_{CC\,C} = 5\ V \pm 5\%$, $V_{EE\,A}$, $V_{EE\,D} = -4.5\ V \pm 5\%$, $T_A = 25\,°C$

Description	Symbol	min.	typ.	max.	Unit
Static Nonlinearity					
Integral nonlinearity	*INL*			0.25	LSB
Differential nonlinearity	*DNL*			0.25	LSB
Dynamic Performance[1]					
Large signal bandwidth	f_{3dB}		250		MHz
Effective resolution[2]					
$f_c = 300$ MHz, $V_{AIN} = 2\ V_{pp}$					
$f_{AIN} = 10$ MHz			5.9		bit
$f_{AIN} = 50$ MHz		5.6	5.8		bit
$f_{AIN} = 100$ MHz		5.3	5.4		bit
$f_{AIN} = 150$ MHz			5.0		bit
Signal-to-noise ratio[3]	*SNR*				
$f_c = 300$ MHz, V_{AIN} =e 2 V_{pp}					
$f_{AIN} = 50$ MHz		36	37.5		dB
$f_{AIN} = 100$ MHz		35	36.5		dB
$f_c = 300$ MHz, $V_{AIN} = 1\ V_{pp}$					
$f_{AIN} = 50$ MHz			37		dB
$f_{AIN} = 100$ MHz			36		dB
Total harmonic distortion	*THD*				
$f_{AIN} = 50$ MHz, $V_{AIN} = 2\ V_{pp}$			−44		dB
$f_{AIN} = 100$ MHz, $V_{AIN} = 2\ V_{pp}$			−39		dB

1) measured in a 50 Ω analog system at 300 MHz sampling rate (300 mV_{pp} sinewave clock)
2) includes both noise and harmonic distortions
3) without the effect of harmonics;
thus b_{eff}, *SNR* [dB] and *THD* [dB] are related by $b_{eff} = \{-10 \log -(10^{-SNR/10} + 10^{THD/10}) - 1.8\}/6$

Clock input
Figure 3a

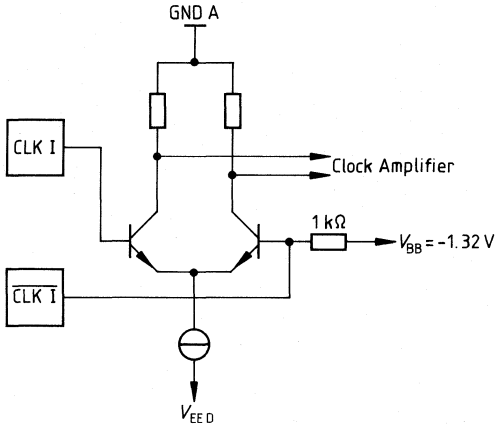


Figure 3b

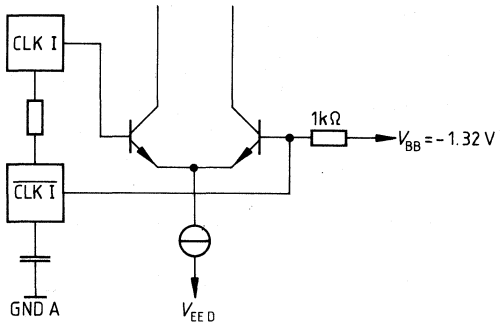


Figure 3c

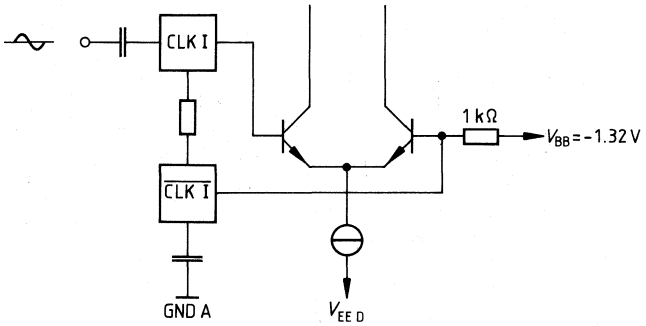


Figure 4
Timing Diagram
Direct Modes

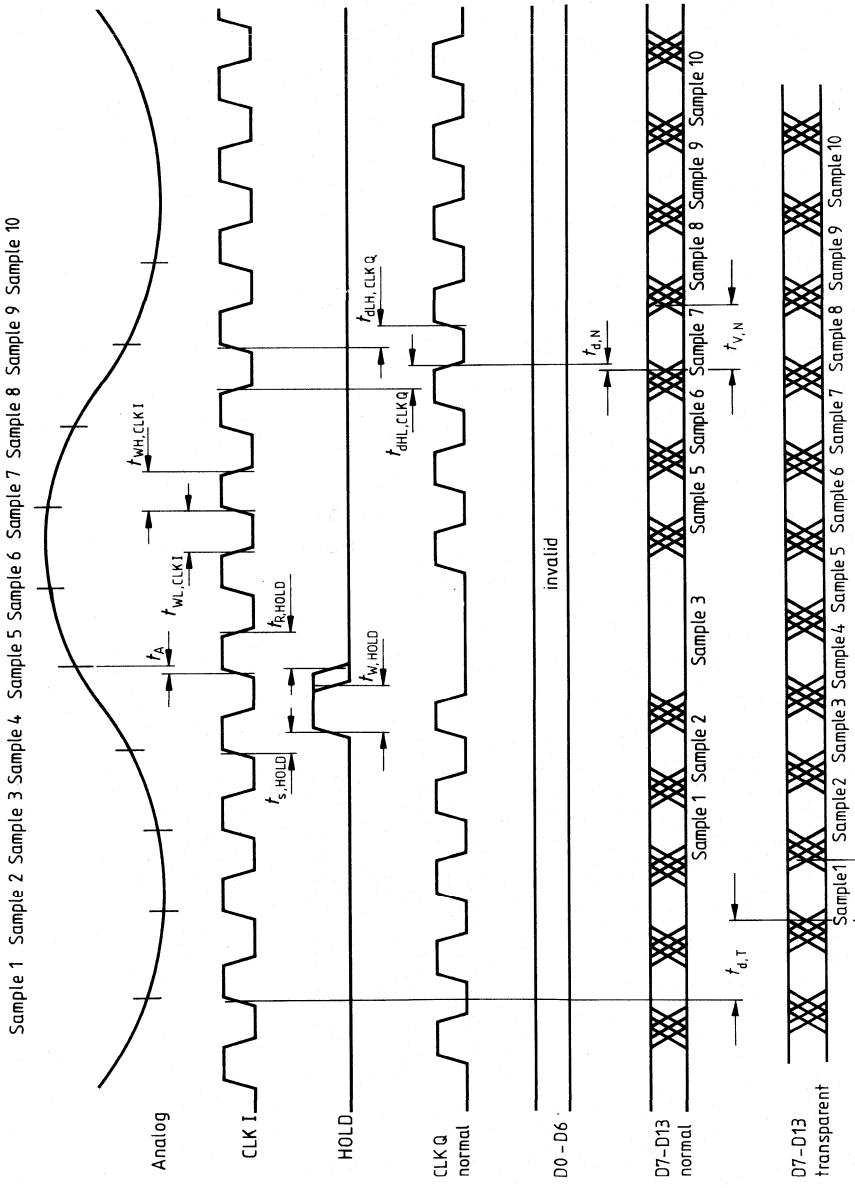


Figure 5
Demultiplexing Mode

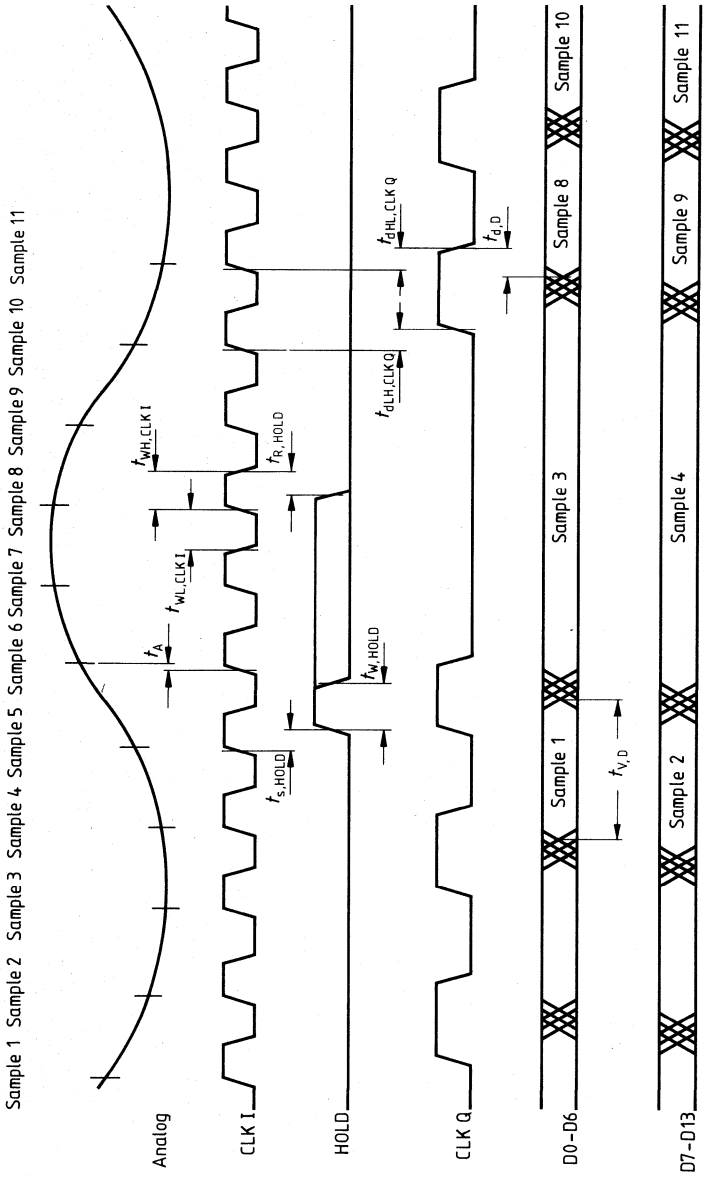
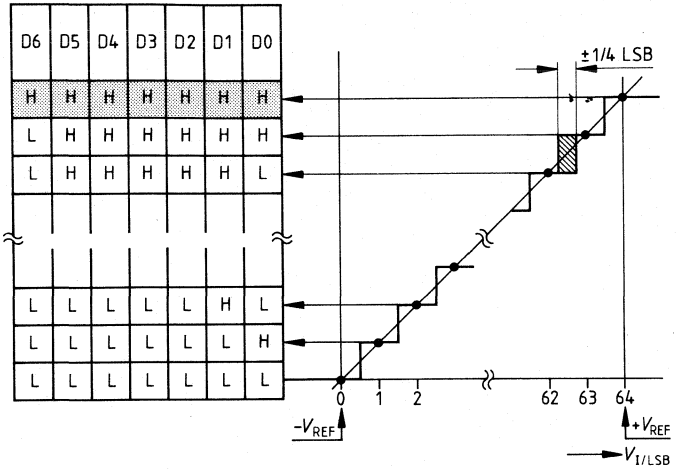
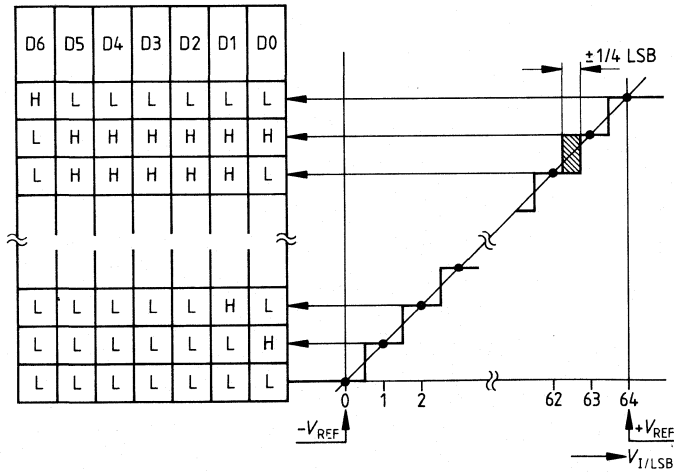


Figure 6
Transfer Characteristic and Truth Table

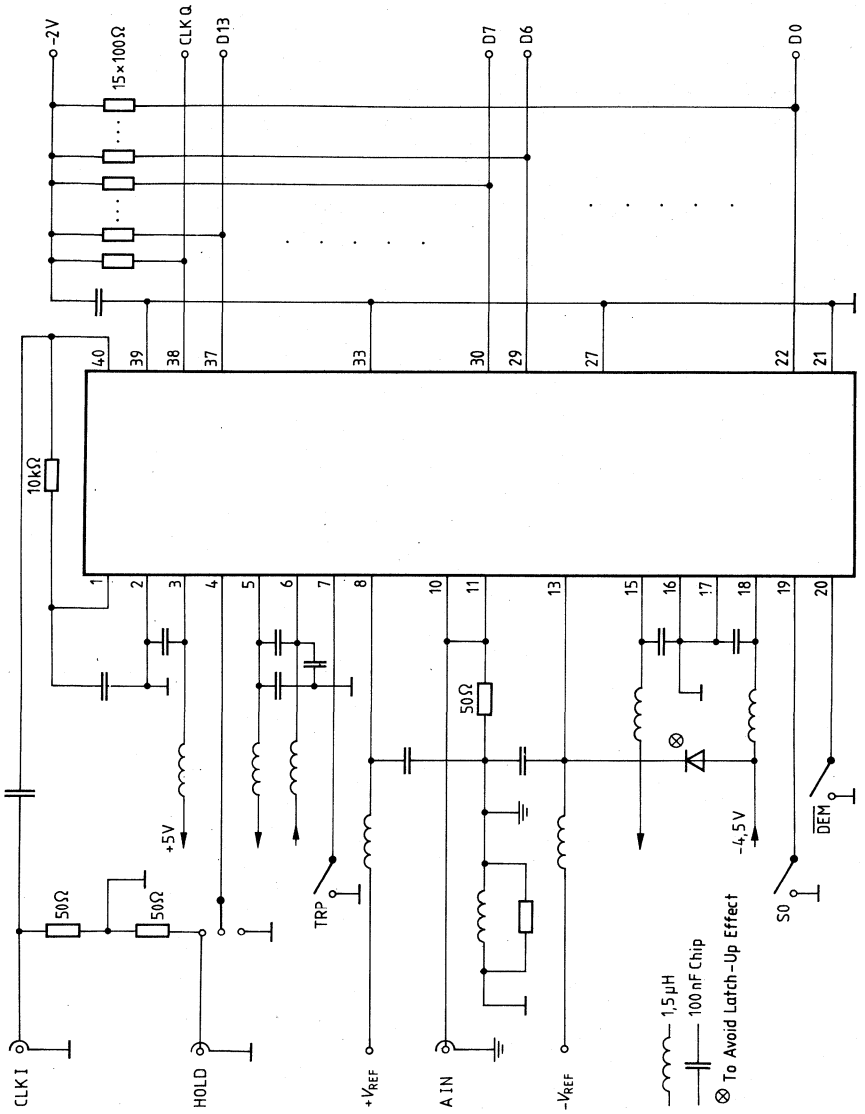


a) SO set to "L" or not connected

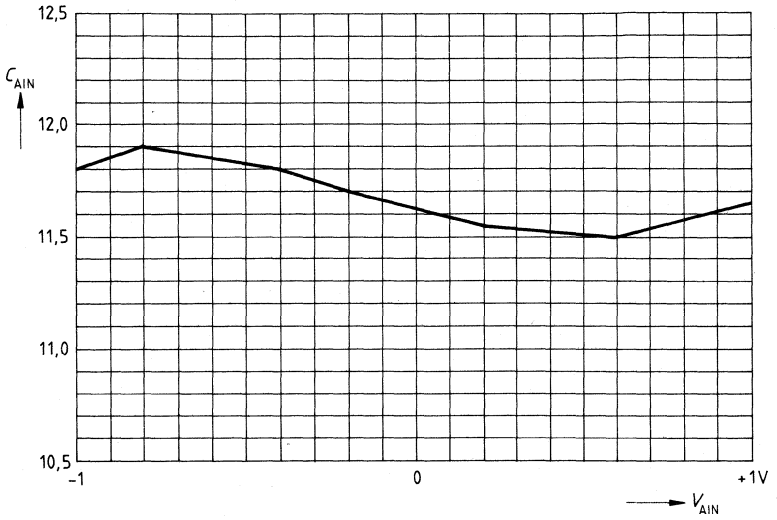


b) SO set to "H" or strapped to ground

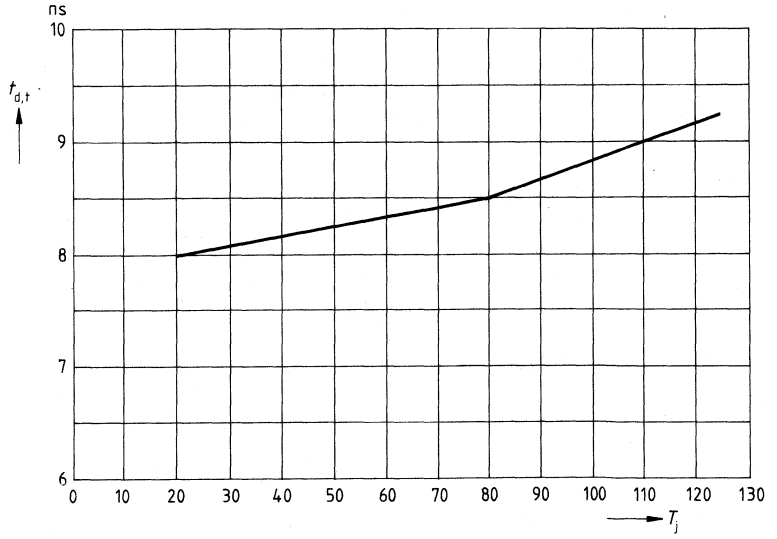
Figure 7
Test Circuit



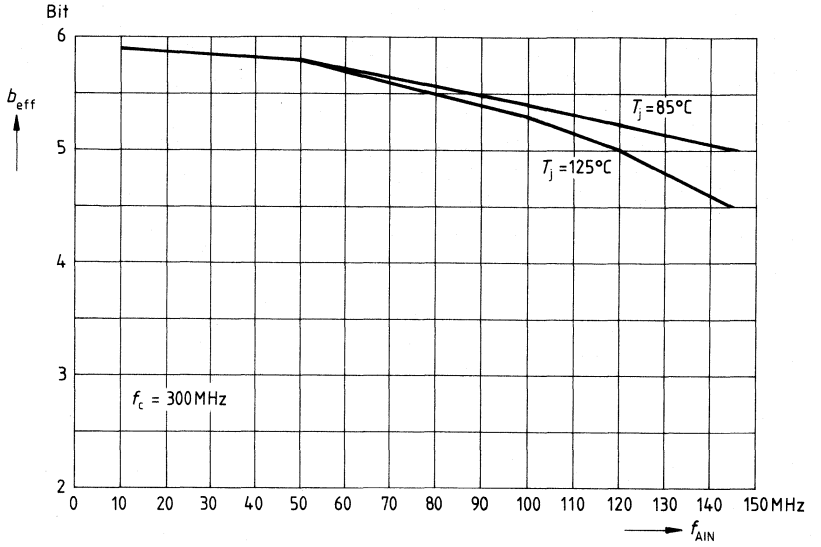
Analog Input Capacitance C_{AIN} versus Input Bias Voltage



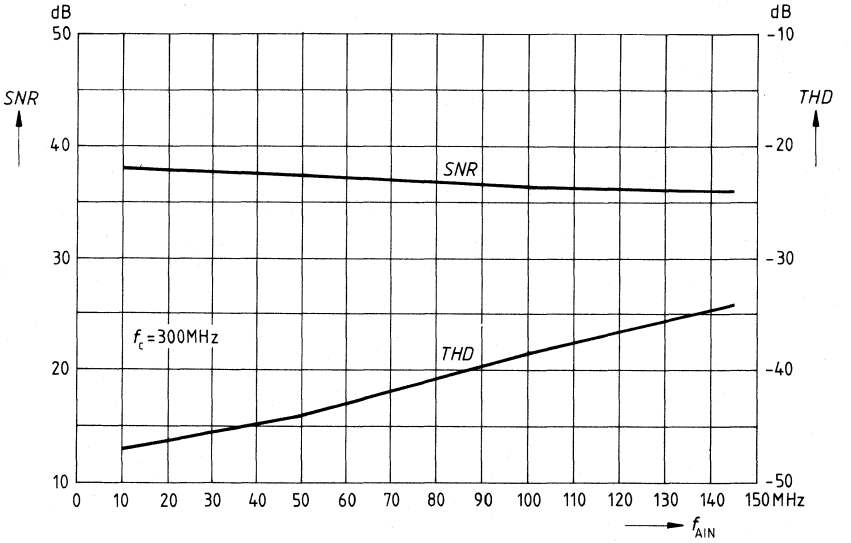
Output Delay (Transparent Mode) $t_{d,T}$ versus Junction Temperature



Effective Resolution b_{eff} versus Analog Frequency



Signal-to-Noise-Ratio *SNR* and Harmonic Distortion *THD* versus Analog Frequency



Preliminary Data **Bipolar IC**

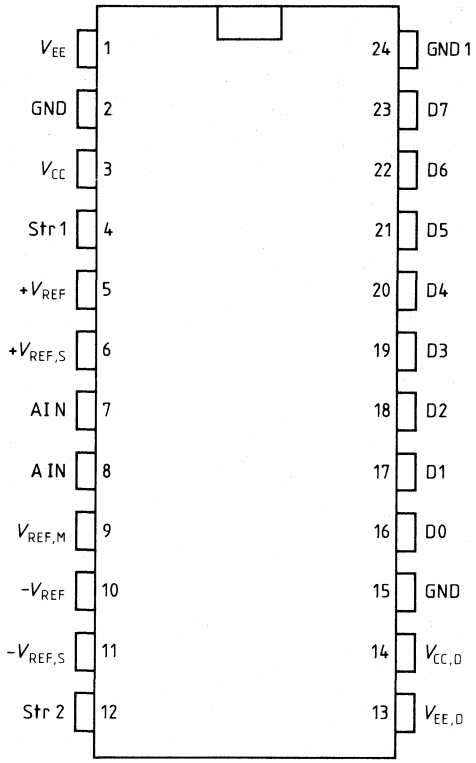
Type	Ordering Code	Package
SDA 8010	Q67000-A2566	C-DIP-24

The SDA 8010 is an ultrafast A/D converter operating according to the parallel principle, with a resolution of 8 bits and a guaranteed strobe frequency of 100 MHz. The device is capable of digitizing full scale (±1 V) analog signals with frequency components up to 50 MHz at a power consumption of 1.3 W. Due to the symmetric input voltage range it can be driven directly by a customary 50-Ω source.

Features

- 100 MHz min. conversion rate
- 6.3 effective bits at 30-MHz input frequency
- Excellent large-signal bandwidth
- Nonlinearity lower than 1/2 LSB
- Balanced input voltage range
- ECL-100-K compatible output data
- Low power dissipation
- Small (C-DIP-24) ceramic package

Figure 1
Pin configuration
(top view)



Pin Description

Pin	Symbol	Function
1	V_{EE}	Neg. supply voltage, analog section
2	GND	Ground
3	V_{CC}	Pos. supply voltage, analog section
4	Str 1	Strobe signal 1
5 6	$+V_{REF}$ $+V_{REF,\,s}$	Pos. reference voltage Pos. reference voltage sense
7 8	A IN A IN	Analog input Analog input
9	$V_{REF,\,M}$	Center tap of voltage divider
10 11	$-V_{REF}$ $-V_{REF,\,s}$	Neg. reference voltage Neg. reference voltage sense
12	Str 2	Strobe signal 2
13 14	$V_{EE,\,D}$ $V_{CC,\,D}$	Neg. supply voltage, digital section Pos. supply voltage, digital section
15	GND	Ground
16 to 23	D0 to D7	Digital output signals
24	GND 1	Ground connection for output emitter follower

Functional Description

The SDA 8010 is an ultrafast A/D converter operating according to the "flash" or parallel principle: a field of 255 comparators simultaneously compares the analog signal with 255 reference voltages spread linearly over the input voltage range. The result of this comparison, delivered in the so-called thermometer code, is converted into binary representation by three encoding stages and is then available as a digital signal with ECL levels at the outputs **(see block diagram)**.

An individual comparator consists of a differential amplifier and a master/slave register stage. They are activated alternately by means of two strobe signals STR1 and STR2, thereby sampling the analog signal and holding the corresponding logical state. The sequence of the conversion process is given in the pulse diagram.

During the L phase of STR1, the analog signal is compared with the reference voltages. With the rising edge of STR1 the result of the comparison is passed into the first register stage and held there until the falling edge of STR 1. Towards the end of this hold period the signal is accepted into the second flipflop with the L phase of the second strobe STR2 and stored with the rising edge. After a delay $t_{d,\,Q}$ this data appears at the output and remains valid for the period $t_{v,\,Q}$.

Driving the converter's analog input is an easy task. Due to the ground-symmetrical input voltage range and the low input capacitance, the converter can be operated in a customary 50-Ω system without any preamplifiers or level shifters. Nevertheless, lower impedance driving would be a means for further improving the device's specified dynamic parameters. Two input pins AIN ensure low lead inductance. The internal reference voltages are generated by an on-chip resistor string. The potential at its end points, $+V_{REF}$ and $-V_{REF}$, respectively, determine the input voltage range which is resolved with an accuracy of 8 bits. Additional sense pins $+V_{REF,\,S}$ and $-V_{REF,\,S}$ allow compensation of voltage drops across parasitic resistances at the top and bottom of the string. The assignment of the digital output code to the input voltage is shown in the transfer characteristic. As no overflow function is provided, the output will remain at a value of 255 when the reference voltage range is exceeded.

Connection $V_{REF,\,M}$ only serves for RF decoupling; no additional adjustment is required for maintaining the specified accuracy of ± 0.5 LSB.

The use of two supply systems, V_{CC} V_{EE} and $V_{CC,\,D}$, $V_{EE,\,D}$ and an additional ground line GND 1 for the output stages reduces the mutual influence of analog and digital signals. Additionally, the separate return of the analog signal ground line is recommended **(see test circuit)**.

Figure 2
Block Diagram

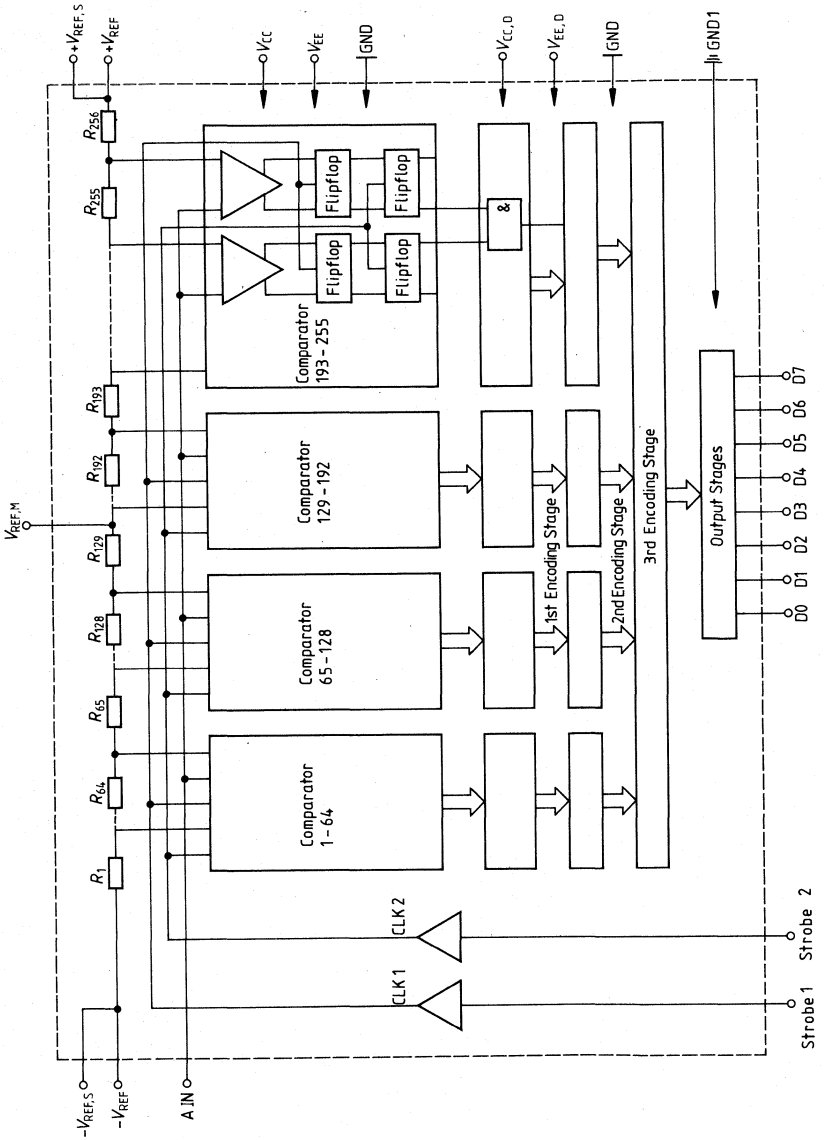
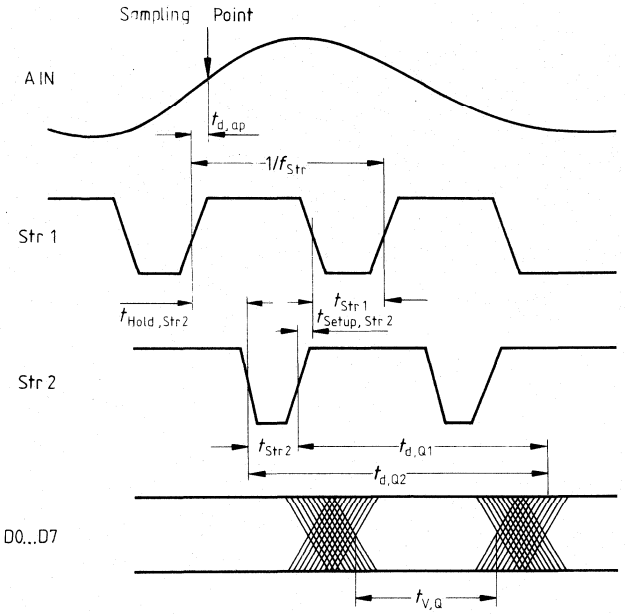


Figure 3
Pulse Diagram



Strobe Timing[1)]

	min.	typ.	Unit
$t_{Str\ 1}$	4	5	ns
$t_{Str\ 2}$	3	3.5	ns
$t_{Set\ up,\ Str\ 2}$	−2.0[2)]	−1.5[2)]	ns
$t_{Hold,\ Str\ 2}$	2	3	ns

1) This is recommended strobe setting for operation at 100 MHz. At lower strobe frequencies the timing becomes more and more uncritical. Below 75 MHz complementary strobe signals with a duty cycle of 50% may be used.

2) Negative values of $t_{Setup,\ Str\ 2}$ indicate that the rising edge of Str 2 should appear after the falling edge of Str 1.

Maximum Ratings

Description	Symbol	min	max	Unit
Pos. supply voltage	V_{CC}, $V_{CC,\,D}$	−0.3	6.0	V
Neg. supply voltage	V_{EE}, $V_{EE\,D}$	−6.0	0.3	V
Reference voltage[1])	$+V_{REF}$, V_{REF}	−2.5	1.5	V
Analog input voltage	$V_{A\,IN}$	−2.5	1.5	V
Digital input voltage	$V_{Str\,1}$, $V_{Str\,2}$	−3.5	0	V
Output current	$I_{D0}\ldots I_{D7}$		20	mA
Junction temperature	T_j		125	°C
Ambient temperature (with heat sink)	T_A	−25	50	°C
Storage temperature	T_{stg}	−25	125	°C
Thermal resistance Junction – ambient (without heat sink)	$R_{th\,JA}$		50	K/W

Characteristics

V_{CC}, $V_{CC,\,D} = 5\ V \pm 5\%$, V_{EE}, V_{EE}, $V_{EE,\,D} = -4.5\ V \pm 5\%$, $T_j = 25\,°C$ to $125\,°C$

Description	Symbol	min	typ	max	Unit
Current Consumption					
Pos. supply current, analog	I_{CC}		95		mA
Pos. supply current, digital	$I_{CC,\,D}$		85		mA
Total pos. supply current	$I_{CC} + I_{CC,\,D}$		180	200	mA
Neg. supply current, analog	I_{EE}		70		mA
Neg. supply current, digital	$I_{EE,\,D}$		20		mA
Total neg. supply current	$I_{EE} + I_{EE,\,D}$		90	100	mA
Power dissipation	P_D		1.3	1.5	W
Permissible supply voltage difference	ΔV_{CC}, ΔV_{EE}			100	mV
Reference Inputs					
Reference voltages[1])	$+V_{REF}$, $-V_{REF}$	−2		1	V
Total reference resistance	R_{REF}	105	150	190	Ω
Temperature coefficient of reference resistor	TC		3×10^{-3}		1/K
Analog Input					
Voltage range	V	−2		1	V
Input current[2]) $V_{AIN} \geq +V_{REF}$	I_I	150		700	µA
$V_{AIN} \leq -V_{REF}$	I_I			1	µA
Input capacitance $V_{AIN} \geq +V_{REF}$	C_{AIN}		45		pF
$V_{AIN} \leq -V_{REF}$	C_{AIN}		55		pF

For comments see page 395

Characteristics

V_{CC}, $V_{CC,\,D} = 5\ V \pm 5\%$, V_{EE}, $V_{EE,\,D} = -4.5\ V \pm 5\%$; $T_j = 25\,°C$ to $125\,°C$

Description	Symbol	min	typ	max	Unit
Strobe Inputs					
H input voltage	V_{IH}	−1.165			V
L input voltage	V_{IL}			−1.475	V
Max. strobe frequency	f_{Str}	100	125		MHz
H input current $V_{Str} = V_{IH}$	I_{IH}	2		30	µA
L input current $V_{Str} = V_{IL}$	I_{IL}			40	nA
Aperture delay	$t_{d,\,ap}$		1		ns
Aperture jitter	t_{jit}		15		ps
Data Outputs					
H output voltage (100-Ω resistor to −2 V)	V_{QH}	−1.025		−0.880	V
L output voltage (100-Ω resistor to −2 V)	V_{QL}	−1.810		−1.620	V
Signal transition time[3])	$t_{d,\,Q1}$			10.5	ns
	$t_{d,\,Q2}$			14	ns
Time of valid output data[4]) $f_{Str} = 100$ MHz	$t_{V,\,Q}$	4	6		ns
Conversion Characteristics					
Static Nonlinearity[5])					
Integral nonlinearity $\Delta V_{REF} = 1.8$ V	*I NL*			0.5	LSB
Differential nonlinearity $\Delta V_{REF} = 1.8$ V	*D NL*		0.5	0.6	LSB
Dynamic Performance[6])					
Large signal bandwidth	$f_{3\,dB}$	80			MHz
Signal-to-noise ratio					
$f_{an} = 30$ MHz	*SNR*	40	43		dB
$f_{an} = 45$ MHz	*SNR*		35		dB
Total harmonic distortion					
$f_{an} = 30$ MHz	*THD*		−43		dB
$f_{an} = 45$ MHz	*THD*		−30		dB
Effective bits					
$f_{an} = 1$ MHz	N_{eff}		7.4		bit
$f_{an} = 30$ MHz	N_{eff}	6.0	6.3		bit
$f_{an} = 45$ MHz	N_{eff}		4.5		bit

For comments see page 395

Comments

1) $+V_{REF}$ has always to be more positive than $-V_{REF}$.
2) The input current is linearly dependent on the input voltage.
3) Delay from the rising edge ($t_{d,\,Q1}$) or falling edge ($t_{d,\,Q2}$) of Str 2 to the begin of validity of the associated output data.
4) Time interval, during which the conversion of a 30 MHz/2 V_{pp} signal at 100 MHz sampling rate yields an *SNR* of more than 40 dB.
5) The actual transfer characteristic is measured by means of the servo loop principle at both low sampling rates (100 kHz) and slow strobe edges (> 500 ns).
6) Dynamic measurements are performed at 100 MHz sampling rate using the typical strobe timing. All specified parameters are derived from the FET of the converter's response to a full scale (2 V_{pp}) sine wave input. The analog source impedance is 25 Ω (50-Ω line with 50-Ω termination). The test circuit is shown in **figure 5.**

Figure 4
Transfer Characteristic and Truth Table

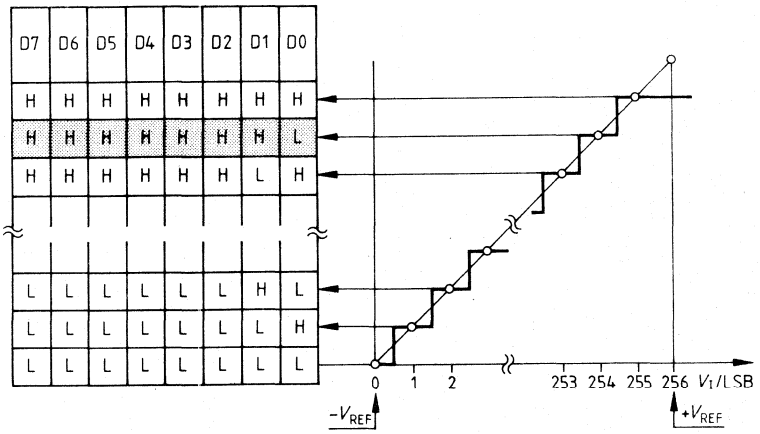


Figure 5
Test Circuit

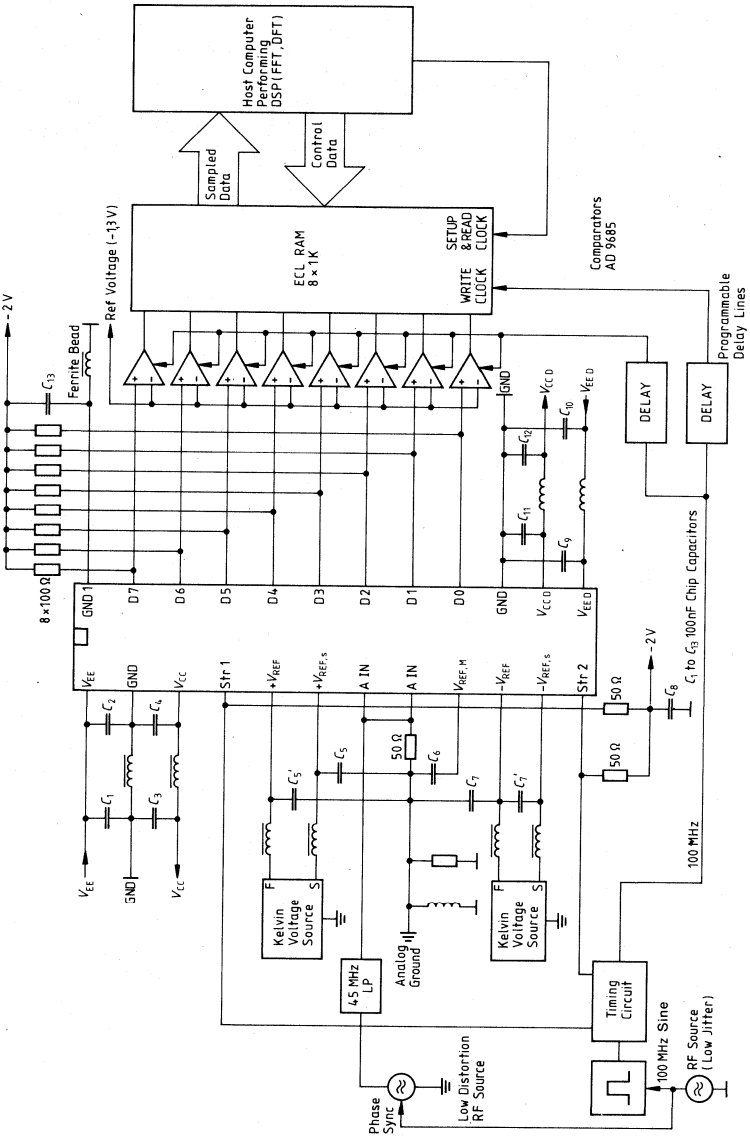


Figure 6
Analog Input Capacitance versus Input Bias Voltage
($+V_{REF} = 1$ V; $-V_{REF} = -1$ V)

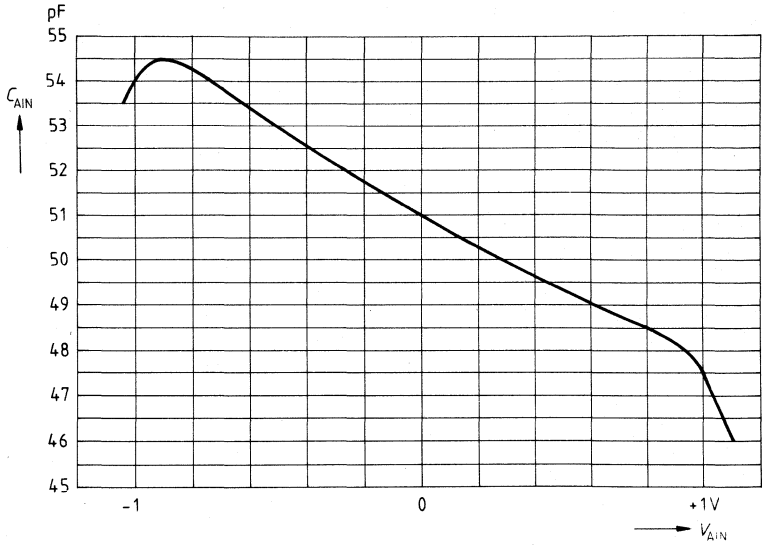


Figure 7
Signal Transition Time $t_{d,Q1}$ and Valid Data Range $t_{V,Q}$ versus Junction Temperature

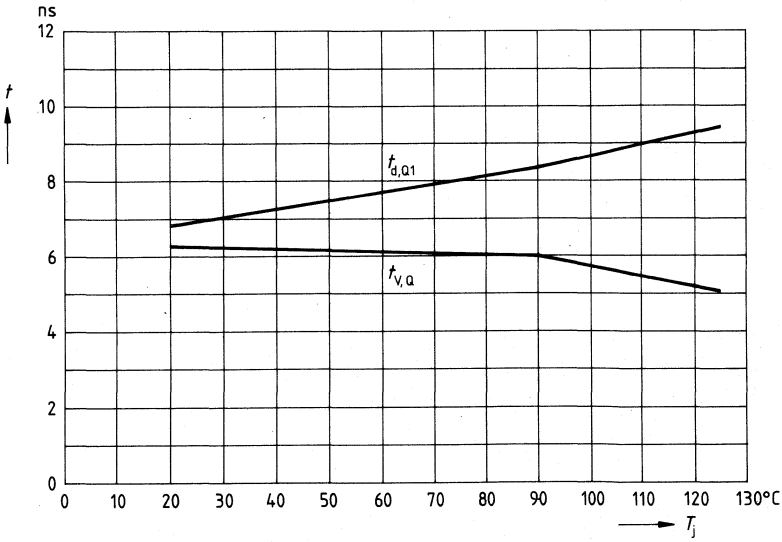


Figure 8
Amplitude Response versus Analog Frequency
a) including voltage drop across source impedance (25 Ω)
b) without voltage drop across source impedance (25 Ω)

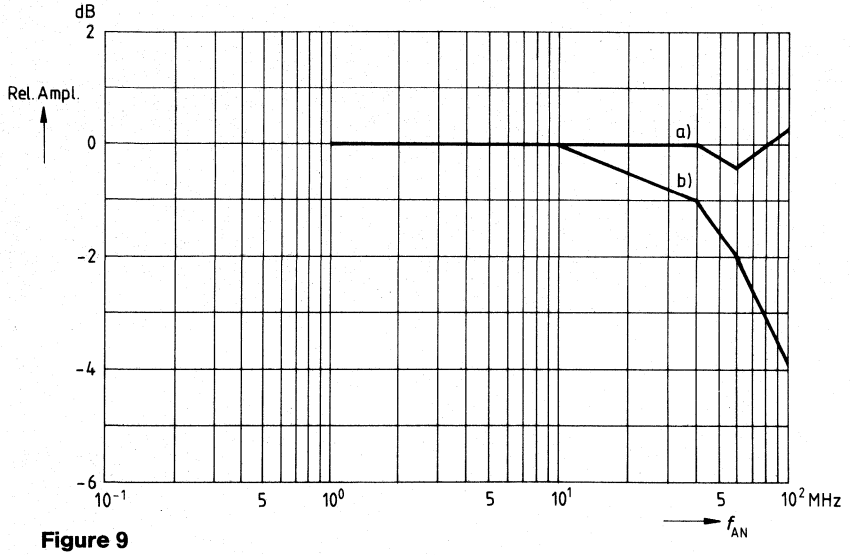


Figure 9
Signal-to-Noise-Ratio *SNR* and Harmonic Distortion *THD* versus Analog Frequency

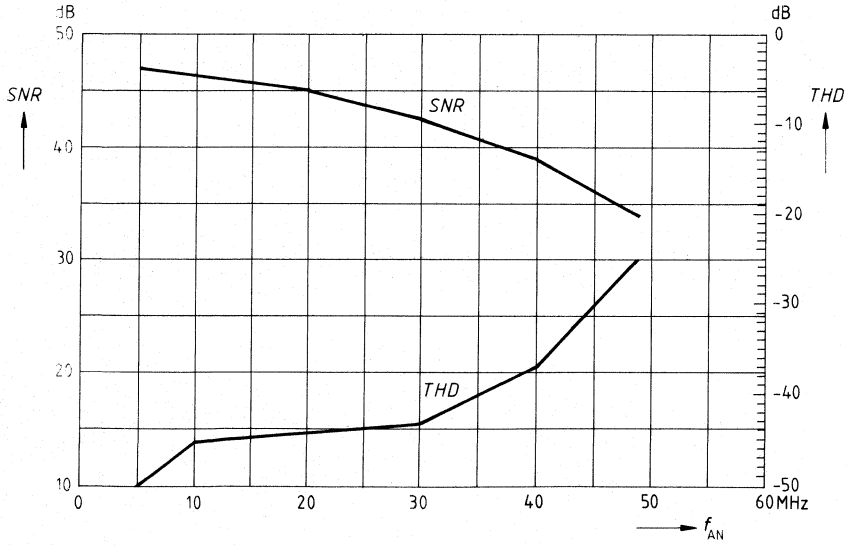
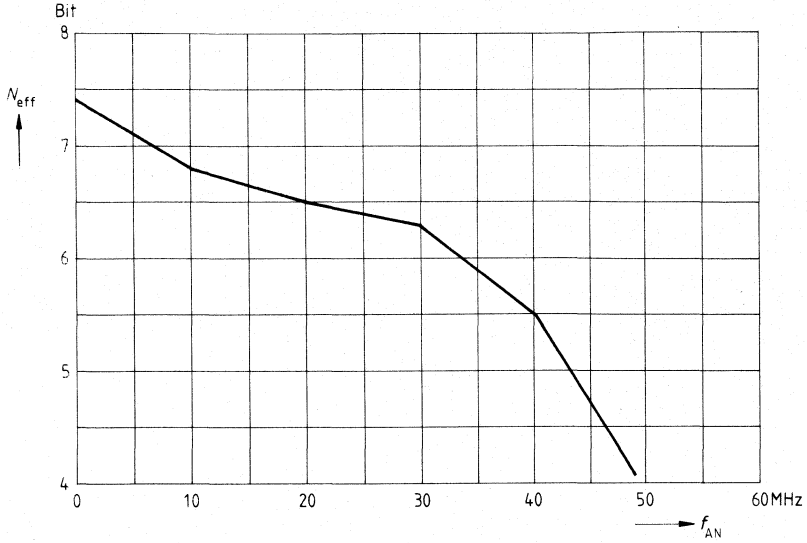


Figure 10
Effective Resolution N_{eff} versus Analog Frequency



Microprocessor-Compatible 8-Bit Analog/Digital Converters with 8-Channel Multiplexer

SDA 0808
SDA 1808

Preliminary Data

CMOS IC

Type	Ordering Code	Package
SDA 0808 A	Q67100-A8128	P-DIP-28
SDA 0808 B	Q67100-A8129	P-DIP-28
SDA 0808 N	Q67100-A8206	PL-CC-28 (SMD)
SDA 1808 N	Q67100-A8254	PL-CC-28 (SMD)

SDA 0808 and SDA 1808 are monolithic 8-bit CMOS A/D converters with an 8-channel analog multiplexer and a single 5 V dc supply. The ICs contain a microprocessor-compatible control logic and an 8-bit data bus. They are pin-compatible with the data-acquisition component ADC 0808/0809.

SDA 0808 and SDA 1808 use the method of successive approximation by means of a capacitor network. The converters feature a temperature-stabilized comparator, an 8-channel multiplexer for 8 analog inputs and a sample and hold circuit. The converters need no external offset or gain adjustment. Easy interfacing to microprocessors is provided by 3-bit address latches, 8-bit data output latches and an 8-bit tristate data bus.

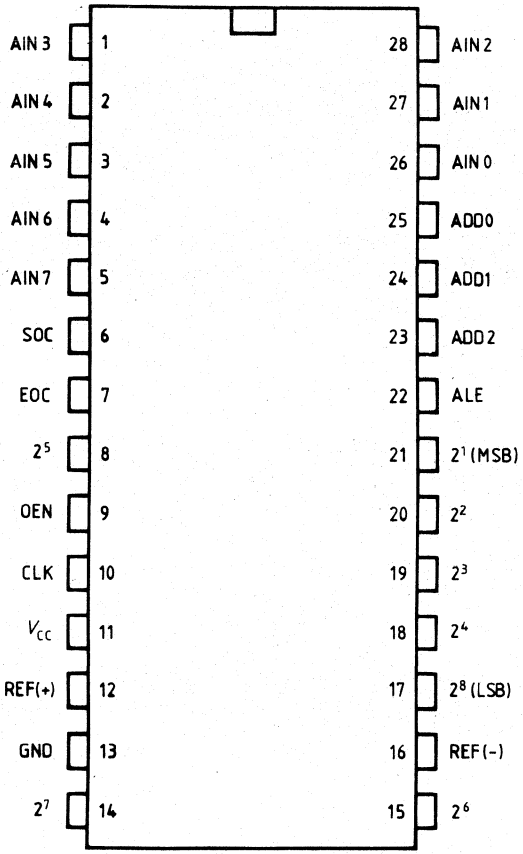
The temperature range of the SDA 0808 A/N, SDA 1808 N is between −40 °C and +85 °C and that of the SDA 0808 B between −40 °C and +125 °C.

Features

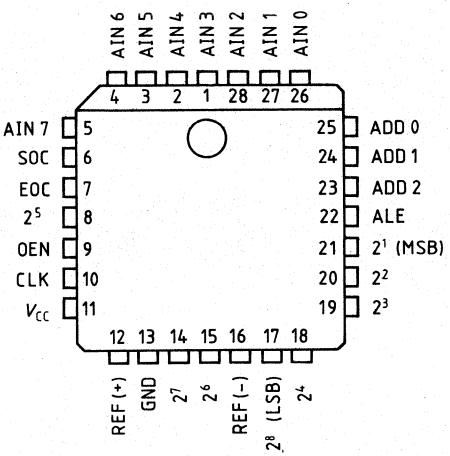
- **A**dvanced **CMOS** (ACMOS) technology
- 8 bit resolution
- Absolute unadjusted error ± 1/2 LSB
- No missing codes
- Fast conversion time (15 µs)
- Single 5 V dc supply voltage
- 8-channel multiplexer with latched control logic
- Easy interfacing to all microprocessors, or stand-alone operation
  0 V to 5 V analog input voltage range
- No offset or gain adjustment required
- Latched tristate outputs
- TTL-compatible output voltage
- CMOS IC with low power consumption (15 mW)
- 28 pin P-DIP and PL-CC standard packages
- Extended temperature range between −40 °C and +125 °C (SDA 0808 B)

Pin Configurations
(top view)

SDA 0808 A; B



SDA 0808 N,
SDA 1808 N



Pin Description

Pin	Symbol	Function
1 to 16	AIN 3 to AIN 7	Analog inputs
6 7	SOC EOC	Start of conversion End of conversion
8	2^5	Digital output signal
9	OEN	Output enable signal
10	CLK	External clock input
11 12	V_{CC} REF (+)	Positive supply voltage Positive reference voltage
13	GND	Ground
14, 15	2^7, 2^6	Digital output signals
16	REF (–)	Negative reference voltage
17 to 21	2^8 (LSB) to 2^1 (MSB)	} Digital output signals
22	ALE	Address latch enable
23 to 25 26 to 28	ADD 2 to ADD 0 AIN 0 to AIN 2	Address inputs Analog inputs

Functional Description

Converter

The converter consists of three major parts: A capacitor network (approx. 50 pF) as a sample and hold circuit, the successive approximation register and the comparator. The capacitor network includes a circuit configuration which provides the first output for a transition when the analog signal has reached +1/2 LSB.

The A/D converter's successive approximation register (SAR) is reset with the positive edge of the start of conversion (SOC) pulse. The conversion starts with the next rising edge of the external clock signal after the falling edge of the SOC pulse. A conversion in process will be interrupted by an SOC pulse.

Following the rising edge of the SOC pulse, the EOC output (end of conversion) passes to the low level. It is set to logic one with the first rising edge of the external clock after the internal latch pulse.

The comparator is automatically set to zero, has a high resolution and a low drift. Thus the A/D converter is extremely insensitive to temperature errors.

A/D Converter Timing

The values stated apply to the SDA 0808, those is parentheses to the SDA 1808.

After a conversion has been started, the analog voltage at the selected input channel is sampled for 10 (20) external clock cycles which will be kept at the sampled level for the remaining conversion time. The external analog source must be capable of supplying the current that is necessary to charge the sample and hold capacitance of approx. 50 pF within those 10 (20) clock cycles.

Conversion of the sampled analog voltage takes place between the 11th (22nd) and 19th (38th) clock cycle after sampling has been completed. In the 19th (38th) clock cycle the result of the conversion is written into the output data latch. The EOC signal is set during the rising edge of the 20th (40th) clock cycle.

Multiplexer

The converters provide eight multiplexed analog input channels. The input channels are selected by programming of three address lines (AD2, AD1, AD0).

Table 1 shows the input states for the address lines that select a channel. The address is latched on the rising slope of the ALE signal.

Address Lines			Selected Analog Channel
AD2	AD1	AD0	AIN
L	L	L	AIN 0
L	L	H	AIN 1
L	H	L	AIN 2
L	H	H	AIN 3
H	L	L	AIN 4
H	L	H	AIN 5
H	H	L	AIN 6
H	H	H	AIN 7

Table 1

Maximum Ratings

Description	Symbol	min	max	Unit
Supply voltage[1])	V_{CC}		6.5	V
Input voltage range, any input	V_I	−0.3	V_{CC} +0.3	V
Power dissipation (at or below T_A = 25 °C)	P_D		875	mW
Storage temperature range	T_{stg}	−65	150	°C

Recommended Operating Conditions

Description	Symbol	min	typ	max	Unit
Supply voltage	V_{CC}	4.5	5	6	V
Positive reference voltage[2])	V_{REF}		V_{CC}	V_{CC}+0.1	V
Negative reference voltage			0	−0.1	V
Differential reference voltage	$\Delta V_{REF} = +V_{REF} - V_{REF}$		5		V
Start pulse duration	$t_{w\,(S)}$	200			ns
Address load control pulse width	$t_{w\,(ALE)}$	200			ns
Address setup time	t_{Setup}	50			ns
Address hold time	t_{Hold}	50			ns
Clock frequency SDA 0808	f_{CLK}	10	640	1500	kHz
SDA 1808	f_{CLK}	20	1280	2500	kHz
Ambient temperature					
SDA 0808 A/N; SDA 1808 N	T_A	−40		85	°C
SDA 0808 B	T_A	−40		125	°C

For notes refer to page 408

Electrical Characteristics in the Recommended Operating Temperature Range

V_{CC} = 4.75 V to 5.25 V (unless otherwise specified)

Total Component

Description	Symbol	Test conditions	min	typ	max	Unit
High-level input voltage, control inputs	V_{IH}	V_{CC} = 5 V	V_{CC}−1.5			V
Low-level input voltage, control inputs	V_{IL}	V_{CC} = 5 V			1.5	V
High-level output voltage	V_{QH}	I_Q = −360 µA	V_{CC}−0.4			V
Low-level output voltage, data outputs	V_{QL}	I_Q = 1.6 mA			0.45	V
End of conversion	V_{QL}	I_Q = 1.2 mA			0.45	V
OFF-state output current (high impedance-state)	I_{QZ}	V_Q = 5 V			3	µA
Output current	I_{QZ}	V_Q = 0			−3	µA
Control input current at max. input voltage	I_I	V_I = 5 V			1	µA
Low-level control input current	I_{IL}	V_I = 0			−1	µA
Supply current	I_{CC}	f_{CLK} = 640 kHz		0.3	3	mA
Input capacitance, control input	C_I	T_A = 25 °C		10	15	pF
Output capacitance, data outputs	C_Q	T_A = 25 °C		10	15	pF
Resistance between pins 12 und 16	R	T_A = 25 °C	1		1000	kΩ

Analog Multiplexer

V_{CC} = 5 V, T_A = 25 °C

Description	Symbol	Test conditions	min	typ	max	Unit
Channel on-state current[3)]	I_{ON}	V_I = 5 V, f_{CLK} = 640 kHz			2	µA
		V_I = 0 V, f_{CLK} = 640 kHz			−2	µA
Channel off-state current	I_{OFF}	V_{CC} = 5 V, T_A = 25 °C, V_I = 5 V		10	−200	nA
		V_{CC} = 5 V, T_A = 25 °C, V_I = 0 V		−10	−200	nA
		V_{CC} = 5 V, V_I = 5 V			1	µA
		V_{CC} = 5 V, V_I = 0 V			−1	µA

For notes refer to page 408

Operating Characteristics

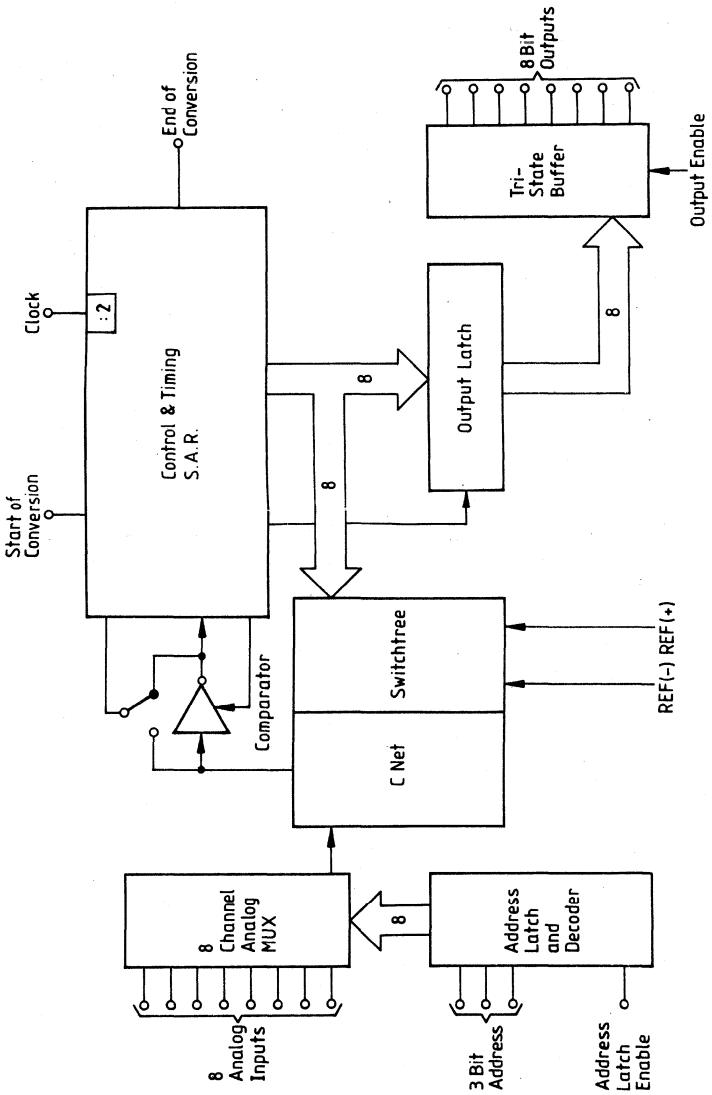
$T_A = 25\,°C$, $V_{CC} = +V_{REF} = 5\,V$, $-V_{REF} = 0\,V$, $f_{CLK} = 640\,kHz$, unless otherwise specified

Description	Symbol	Test conditions	min	typ	max	Unit
Supply voltage sensitivity	k_{SVS}	$V_{CC} = V_{REF+} = 4.75\,V$ to $5.25\,V$, $T_A = -40\,°C$ to $85\,°C$ [4]		±0.05		%/V
Linearity error[5]					±0.5	LSB
Zero error[6]					±0.5	LSB
Absolute unadjusted error[7] SDA 0808 B		$T_A = 25\,°C$ $T_A = -40\,°C$ to $85\,°C$ $T_A = -40\,°C$ to $125\,°C$		±0.25	±0.5 ±0.5 ±0.5	LSB LSB LSB
SDA 0808 N $f_{CLK} = 2.5\,MHz$		$T_A = -40\,°C$ to $85\,°C$		±0.5	±1	LSB
Output enable time **(Figure 1)**	t_{en}	$C_L = 50\,pF$, $R_L = 10\,k\Omega$		80	250	ns
Output disable time **(Figure 1)**	t_{dis}	$C_L = 10\,pF$, $R_L = 10\,k\Omega$		40	95	ns
Output turn-off-time **(Figure 1)**	t_{OFF}	$C_L = 10\,pF$, $R_L = 10\,k\Omega$		20	60	ns
Conversion time	t_{Conv}	$f_{CLK} = 1.5\,MHz/640\,kHz/10\,kHz$ [8]	13	31	2000	µs
SDA 1808 N	t_{Conv}	$f_{CLK} = 2.5\,MHz/1280\,kHz/20\,kHz$ [8]	15	31	2000	µs
Delay time, EOC output	$t_{D\,(EOC)}$	[9]	0		200	ns

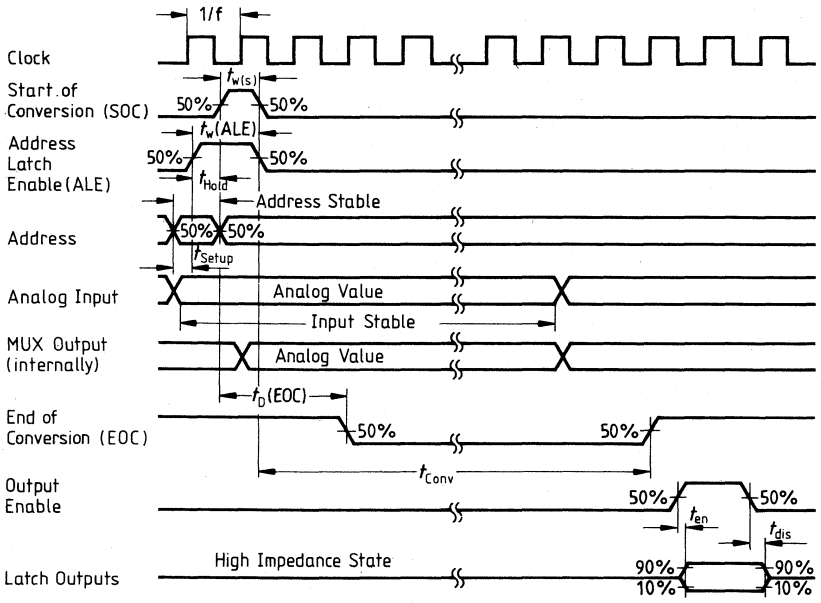
Notes

1) All voltage values refer to the network's ground terminal.
2) Care must be taken that this rating is observed, even during power-up.
3) The channel on-state current is primarily generated by the current of the Schmitt Trigger and varies directly with the clock frequency.
4) The supply voltage sensitivity relates to the ability of an A/D converter to maintain accuracy as the supply voltage varies. Supply voltage and $+V_{REF}$ are both changed at the same time and the change in accuracy is measured with respect to full-scale deflection.
5) The linearity error is the maximum deviation from a straight line to the end points of the A/D transfer characteristic.
6) The zero error is the difference between the output of an ideal converter and that of the present A/D converter at zero input voltage.
7) The absolute unadjusted error is the total of linearity error, zero error and full-scale deflection error.
8) SDA 0808: $t_{Conv\ max} = 20.1/f_{CLK}$ $t_{Conv\ min} = 19.1/f_{CLK}$;
   SDA 1808: $t_{Conv\ max} = 40.1/f_{CLK}$ $t_{Conv\ min} = 38.1/f_{CLK}$
9) Refer to the operating pulse diagram

Block Diagram



Operating Pulse Diagram



Typical Error Curve

(Absolute unadjusted error including offset errors, full-scale deflection errors, linearity errors and multiplexer errors).

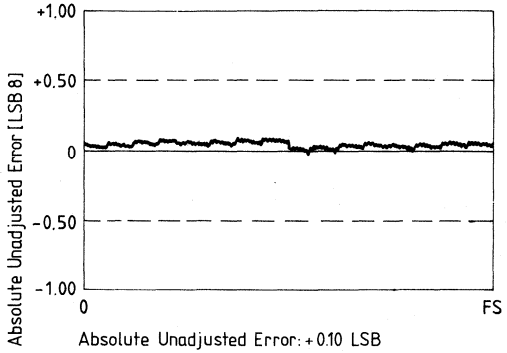
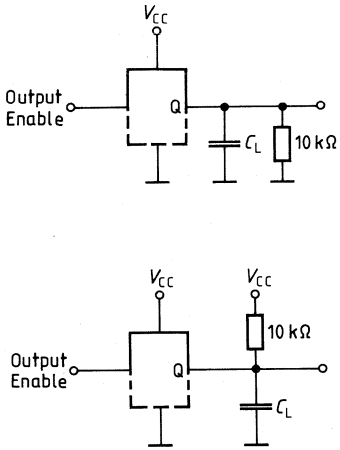
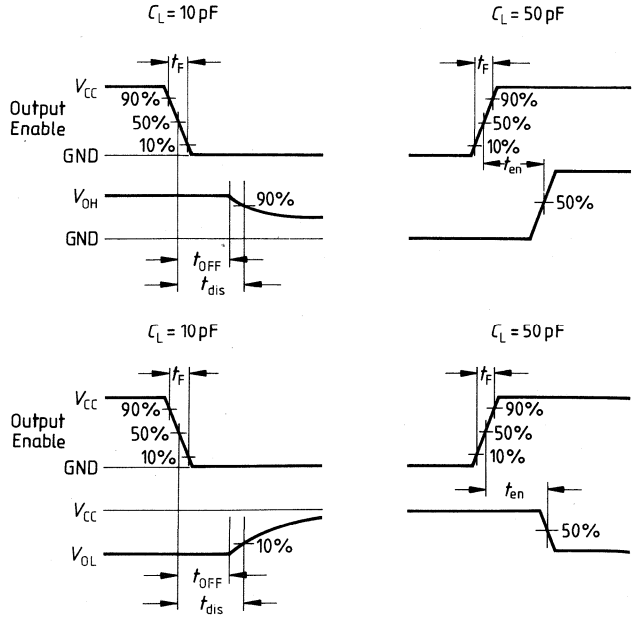


Figure 1
Tristate Measurement Circuits and Pulse Diagrams





Microprocessor Interface

Microprocessor interfacing is straightforward and requires only a few external gates (only one 75LS02).

INTEL Microprocessors

A typical interface is shown in **figure 2.**

Start of conversion

A write instruction selects one of the analog input channels and starts the conversion.

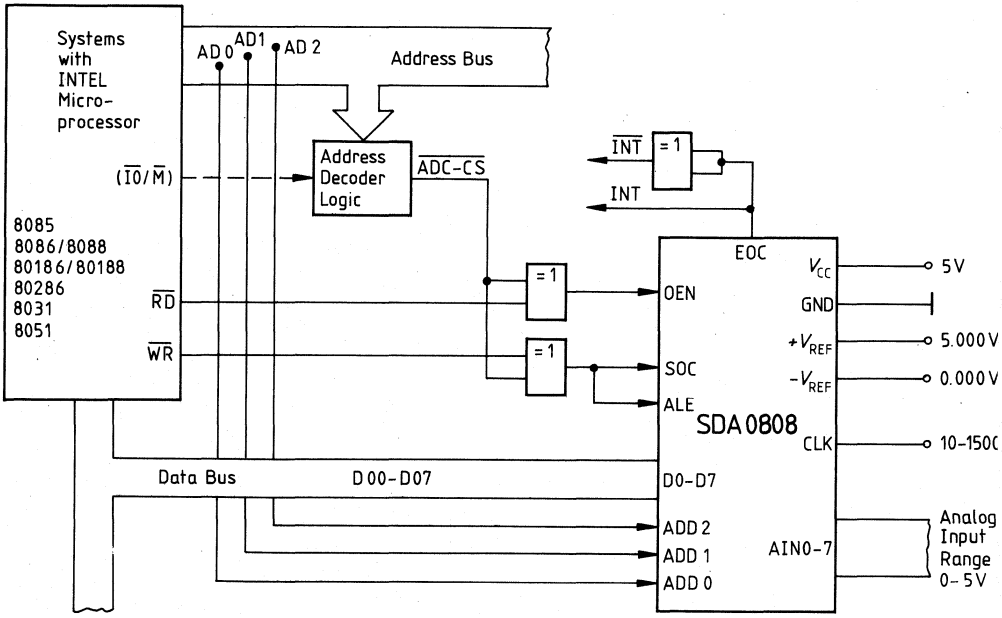
Write address: $\overline{\text{ADC\_CS}}$

The end of conversion signal (EOC) can be used for producing an interrupt in the microprocessor (INT or $\overline{\text{INT}}$).

Reading the conversion result

With a read instruction the conversion result is read from the $\overline{\text{ADC\_CS}}$ address.

Figure 2



[1]) SDA 1808: 20-2500 kHz

Motorola Microprocessors

A typical interface is shown in **figure 3.**

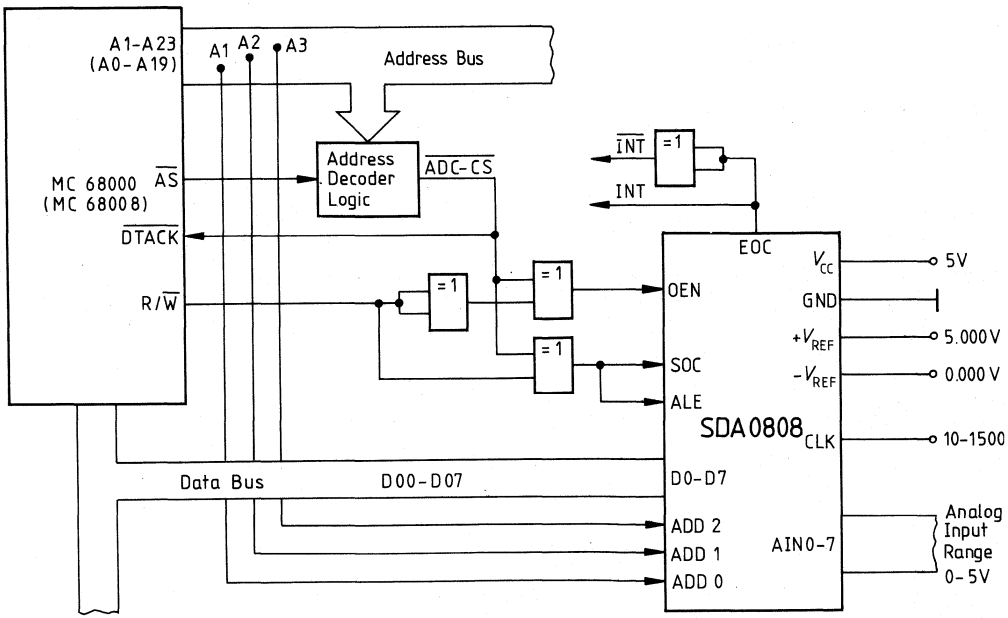
Start of conversion

A write instruction to an address that has been decoded by the address decoder logic will start a conversion. The lower 3 bits of the address bus select the input channel.

Reading of the conversion result

A read instruction from the ADC-ADDRESS puts the conversion result to the data bus: MOVE.B ADC-ADDRESS, D0 places the conversion data in the D0 register of the microprocessor.

Figure 3



[1]) SDA 1808: 20-2500 kHz

Application Hints

Power Supply Decoupling

The power supply of the SDA 0808 should be connected with a 10 µF tantalum or an electrolytic capacitor. To ensure good HF performance this capacitor should be connected in parallel with an 0.01 µF ceramic capacitor. These capacitors should be placed as close as possible to the converter.

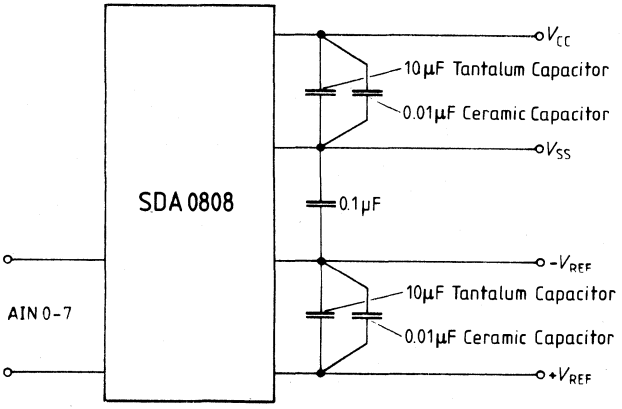
Reference Voltage

To avoid dynamic errors a 10 µF tantalum or electrolytic capacitor connected in parallel with an 0.01 µF ceramic capacitor should be placed as close as possible to the component between pins $+V_{REF}$ and $-V_{REF}$. Also an 0.1 µF ceramic capacitor should be placed between pins $-V_{REF}$ and GND.

Analog input

The high input impedance of the analog channels AIN0 to AIN7 allows simple analog interfacing. Signal sources ($-V_{REF} \leq AIN \leq +V_{REF}$) can directly be connected to the analog input channels, that is without additional buffering, if they are able to supply the current that is necessary to load the sample and hold capacitance being approx. 50 pF, within 10 clock cycles.

Figure 4
Capacitors



Microprocessor-Compatible 10-Bit Analog/Digital Converters with 8-Channel Multiplexer

SDA 0810
SDA 1810

Preliminary Data

CMOS IC

Type	Ordering Code	Package
SDA 0810 A	Q67100-A8130	P-DIP-28
SDA 0810 B	Q67100-A8144	P-DIP-28
SDA 0810 N	Q67100-A8207	PL-CC-28 (SMD)
SDA 1810 N	Q67100-A8230	PL-CC-28 (SMD)

SDA 0810 and SDA 1810 are monolithic 10-bit CMOS A/D converters with an 8-channel analog multiplexer and a single 5 V dc supply. They contain a microprocessor-compatible control logic and an 8-bit data bus. They are pin-compatible with the industrial standards ADC 808 and 809. The 10-bit data stream is supplied in a 2-byte format for interfacing with 8-bit microprocessors. While the SDA 0810 can be operated at a clock frequency of 1 MHz, the SDA 1810 operates at a clock frequency of 2 MHz.

The converters use the method of successive approximation by means of a capacitor network. The converters feature a temperature-stabilized comparator, an 8-channel multiplexer for 8 analog inputs and a sample and hold circuit. The converters need no external offset or gain adjustment. Easy interfacing to microprocessors is provided by 3-bit address latches, 10-bit data output latches and an 8-bit tristate data bus.

The temperature range of the SDA 0810 A/N and SDA 1810 N is between −40 °C and +85 °C, and that of the SDA 0810 B between −40 °C and +125 °C.

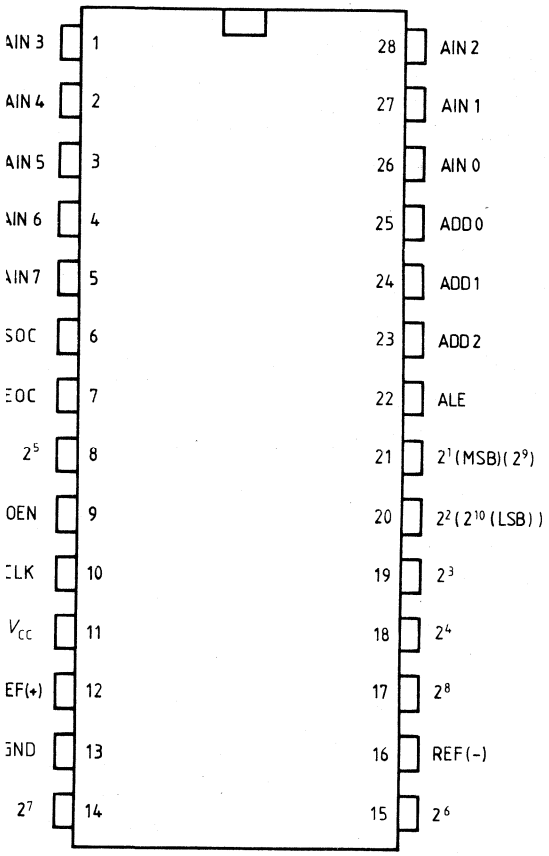
Features

- **A**dvanced **CMOS** (ACMOS) technology
- 10 bit resolution
- Absolute unadjusted error ± 1/2 LSB
- No missing codes
- Fast conversion time (15 µs)
- Single 5 V dc supply voltage
- 8-channel multiplexer with latched control logic
- Easy interfacing to all microprocessors, or stand-alone operation
- 0 V to 5 V analog input voltage range
- No offset or gain adjustments required
- Latched tristate outputs
- TTL-compatible output voltages
- CMOS IC with low power consumption (15 mW)
- 28-pin P-DIP and PL-CC standard packages
- Extended temperature range between −40 °C and +125 °C (SDA 0810 B)

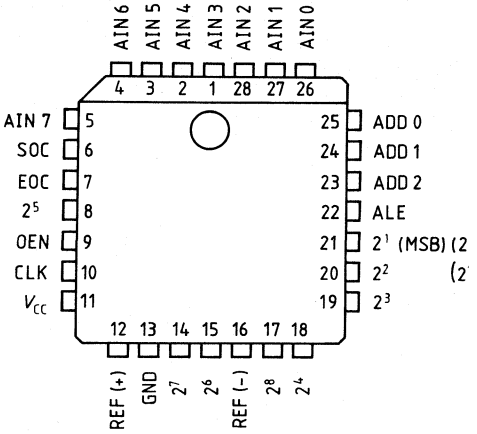
Pin Configurations

(top view)

SDA 0810 A;
SDA 0810 B



SDA 0810 N;
SDA 1810 N



Pin Description

Pin	Symbol	Function
1 to 5	AIN 3 to AIN 7	Analog inputs
6 7	SOC EOC	Start of conversion End of conversion
8	2^5	Digital output signal
9	OEN	Output enable signal
10	CLK	External clock input
11	V_{CC}	Positive supply voltage
12	REF (+)	Positive reference voltage
13	GND	Ground
14, 15	2^7, 2^6	Digital output signals
16	REF (–)	Negative reference voltage
17 to 21	2^8 to 2^1	Digital output signals
22	ALE	Address latch enable
23 to 25 26 to 28	ADD 2 to ADD 0 AIN 0 to AIN 2	Address inputs Analog inputs

Functional Description

Converter

The converter consists of three major parts: A capacitor network (approx. 50 pF) as a sample and hold circuit, the successive approximation register and the comparator. The capacitor network includes a circuit which provides the first output for a transition when the analog signal has reached +1/2 LSB.

The A/D converter's successive approximation register (SAR) is reset with the positive edge of the start of conversion (SOC) pulse. The conversion starts with the next rising edge of the external clock signal after the falling edge of the SOC pulse. A conversion in process will be interrupted by an SOC pulse.

Following the rising edge of the SOC pulse, the EOC output passes to the low level. It is set to logic one with the first rising edge of the external clock after the internal latch pulse.

The comparator is a differential comparator which is automatically set to zero; it has a high supply current rejection factor.

A/D Converter Timing

The values stated apply to the SDA 0810, those in parentheses to the SDA 1810.

After a conversion has been started, the analog voltage at the selected input channel is sampled for 4 (8) external clock cycles which will then be kept at the sampled level for the remaining conversion time. The external analog source must be capable of supplying the current that is necessary to charge the sample and hold capacitance of approx. 50 pF within those 4 (8) clock cycles.

Conversion of the sampled analog voltage takes place between the 5th and 15th (10th and 30th) clock cycle after sampling has been completed. In the 15th (30th) clock cycle the result of the conversion is written into the output data latch. The EOC signal is set during the rising edge of the 16th (32nd) clock cycle.

Multiplexer

The converters provide eight multiplexed analog input channels. The input channels are selected by programming three address lines (AD2, AD1, AD0).

Table 1 shows the input states of the address lines that select a channel. The address is latched on the rising edge of the ALE signal.

Address Lines			Selected Analog Channel
AD2	AD1	AD0	AIN
L	L	L	AIN 0
L	L	H	AIN 1
L	H	L	AIN 2
L	H	H	AIN 3
H	L	L	AIN 4
H	L	H	AIN 5
H	H	L	AIN 6
H	H	H	AIN 7

Table 1

Reading the Conversion Results

The data is read as two 8-bit bytes. The digital outputs of the converters are positive true. Data is presented left-justified and high byte first. The first OEN high after completion of a conversion enables high byte (2^{-1} to 2^{-8}) to the output buffers, the second OEN pulse enables the low byte (2^{-9} to 2^{-10}), the unused bits of this byte are grounded. The byte control logic determines which byte is to be read. With each reading operation a flipflop is toggled so that in successive reading operations the bytes are output alternately. This flipflop is always reset to the high byte at the end of a conversion.

Data Bit Location

High Byte	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
Low Byte	2^{-9}	2^{-10}	0	0	0	0	0	0

Maximum Ratings

Description	Symbol	min	max	Unit
Supply voltage[1])	V_{CC}		6.5	V
Input voltage range, any input	V_I	−0.3	V_{CC} +0.3	V
Power dissipation (at or below $T_A = 25\,°C$)	P_D	875		mW
Operating ambient temperature SDA 0810 A, SDA 0810 N, SDA 1810 N SDA 0810 B	 T_A T_A	 −40 −40	 85 125	 °C °C
Storage temperature range	T_{stg}	−65	125	°C

Recommended Operating Conditions

Description	Symbol	min	typ	max	Unit
Supply voltage Positive reference voltage [2]) Negative reference voltage Differential reference voltage	V_{CC} $+V_{REF}$ $-V_{REF}$ $V_{REF} = +V_{REF} - V_{REF}$	4.5	5 V_{CC} 0 5	6 V_{CC} +0.1 −0.1	V V V V
Start pulse duration Address load control pulse width Address setup time Address hold time	$t_{W\,(S)}$ $t_{W\,(ALE)}$ t_{Setup} t_{Hold}	200 200 50 50			ns ns ns ns
Clock frequency SDA 0810 SDA 1810	f_{CLK} f_{CLK}	50 100	640 1280	1000 2000	kHz kHz

For notes refer to page 423

Electrical Characteristics in the Recommended Operating Temperature Range

V_{CC} = 4.75 V to 5.25 V, unless otherwise specified

Total Component

Description	Symbol	Test conditions	min	typ	max	Unit
High-level input voltage, control inputs	V_{IH}	V_{CC} = 5 V	V_{CC}–1.5			V
Low-level input voltage, control inputs	V_{IL}	V_{CC} = 5 V			1.5	V
High-level output voltage	V_{QH}	I_Q = –360 µA	V_{CC}–0.4			V
Low-level output voltage, data outputs	V_{QL}	I_Q = 1.6 mA			0.45	V
End of conversion	V_{QL}	I_Q = 1.2 mA			0.45	V
OFF-state output current (high impedance-state)	I_{QZ}	V_Q = 5 V			3	µA
Output current	I_{QZ}	V_Q = 0			–3	µA
Control input current at max. input voltage	I_I	V_I = 5 V			1	µA
Low-level control input current	I_{IL}	V_I = 0			–1	µA
Supply current	I_{CC}	$f_{CLK} = f_{CLK}$ (typ)		0.3	3	mA
Input capacitance, control inputs	C_I	T_A = 25 °C		10	15	pF
Output capacitance, data outputs	C_Q	T_A = 25 °C		10	15	pF
Resistance between pins 12 and 16	R		1	1000		kΩ

Characteristics

Analog Multiplexer

V_{CC} = 5 V; T_A = 25 °C

Description	Symbol	Test conditions	min	typ	max	Unit
Channel on-state current[3])	I_{ON}	V_I = 5 V $f_{CLK} = f_{CLK}$ (typ)			2	µA
		V_I = 0 V $f_{CLK} = f_{CLK}$ (typ)			–2	µA
Channel off-state current	I_{OFF}	V_{CC} = 5 V T_A = 25 °C, V_I = 5 V		10	200	nA
		V_{CC} = 5 V T_A = 25 °C, V_I = 0		–10	–200	nA
		V_{CC} = 5 V, V_I = 5 V			1	µA
		V_{CC} = 5 V, V_I = 0			–1	µA

For notes refer to page 423.

Operating Characteristics

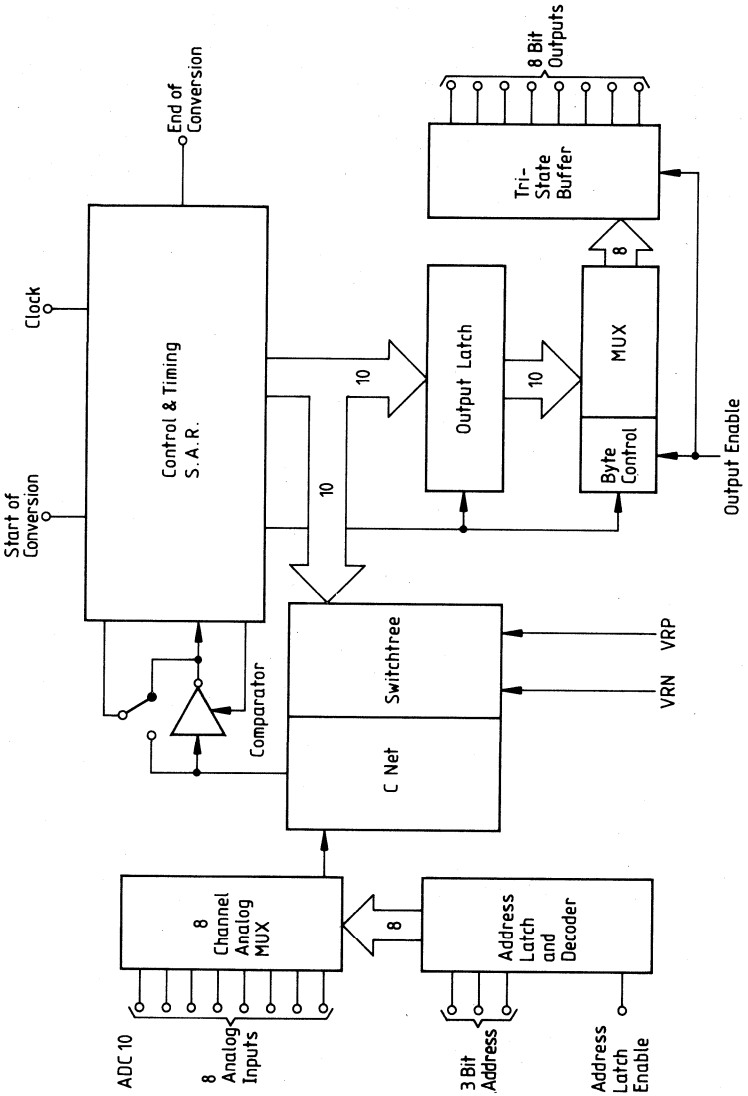
$T_A = 25\,°C$, $V_{CC} = +V_{REF} = 5\,V$, $-V_{REF} = 0\,V$, $f_{CLK} = 640\,kHz$, unless otherwise specified

Description	Symbol	Test conditions	min	typ	max	Unit
Supply voltage sensitivity[4]	k_{SVS}	$V_{CC} = +V_{REF} = 4.75\,V$ to $5.25\,V$ $T_A = -40\,°C$ to $85\,°C$		± 0.05		%/V
Linearity error[5]					± 0.5	LSB
Zero error[6]					± 0.5	LSB
Absolute unadjusted error[7]		$T_A = 25\,°C$ $T_A = -40\,°C$ to $85\,°C$ $T_A = -40\,°C$ to $125\,°C$			± 0.5 ± 0.5 ± 0.5	LSB LSB LSB
Output enable time **(Figure 1)**	t_{en}	$C_L = 50\,pF$, $R_L = 10\,k\Omega$		80	250	ns
Output disable time **(Figure 1)**	t_{dis}	$C_L = 10\,pF$, $R_L = 10\,k\Omega$		40	95	ns
Output turn-off time **(Figure 1)**	t_{OFF}	$C_L = 10\,pF$, $R_L = 10\,k\Omega$		20	60	ns
Conversion time[8] SDA 0810	t_{Conv}	$f_{CLK} = 1\,MHz/640\,kHz/50\,kHz$	15	25	320	µs
Conversion time[8] SDA 1810	t_{Conv}	$f_{CLK} = 2\,MHz/1280\,kHz/100\,kHz$	15	25	320	µs
Delay time, output EOC[9]	$t_{D\,(EOC)}$		0		200	µs

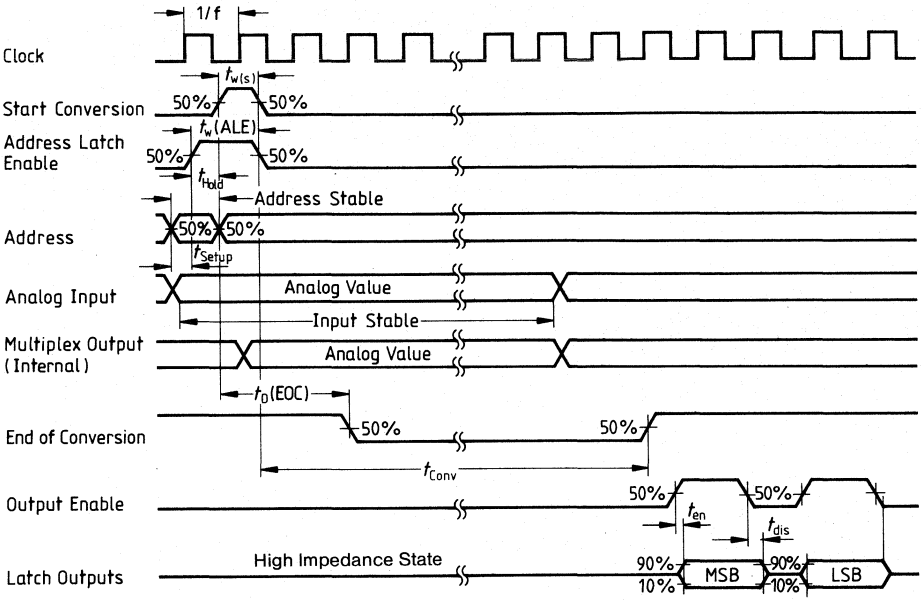
Notes

1) All voltage values refer to the network's ground terminal.
2) Care must be taken that this rating is observed, even during power-up
3) The channel on-state current is primarily generated by the current of the Schmitt Trigger and varies directly with the clock frequency.
4) The supply voltage sensitivity relates to the ability of an A/D converter to maintain accuracy as the supply voltage varies. Supply voltage and $+V_{REF}$ are both changed at the same time and the change of accuracy is measured with respect to full-scale deflection.
5) The linearity error is the maximum deviation from a straight line to the end points of the A/D transfer characteristic.
6) The zero error is the difference between the output of an ideal converter and that of the present A/D converter at zero input voltage.
7) The absolute unadjusted error is the total of linearity error, zero error, and full-scale deflection error.
8) SDA 0810: $t_{Conv\ max} = 16 \cdot 1/f_{CLK}$, $t_{Conv\ min} = 15 \cdot 1/f_{CLK}$
   SDA 1810: $t_{Conv\ max} = 32 \cdot 1/f_{CLK}$, $t_{Conv\ min} = 30 \cdot 1/f_{CLK}$
9) Refer to the operating pulse diagram

Block Diagram



Operating Pulse Diagram



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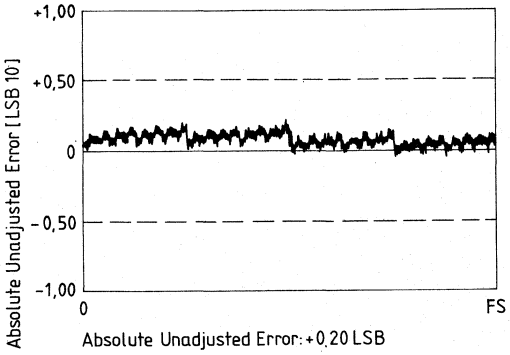
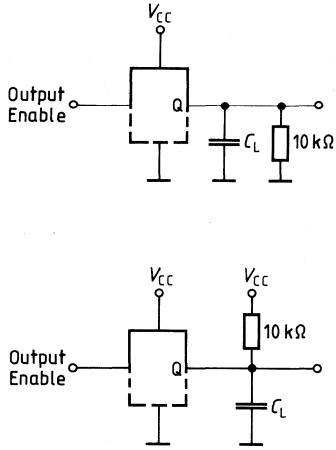
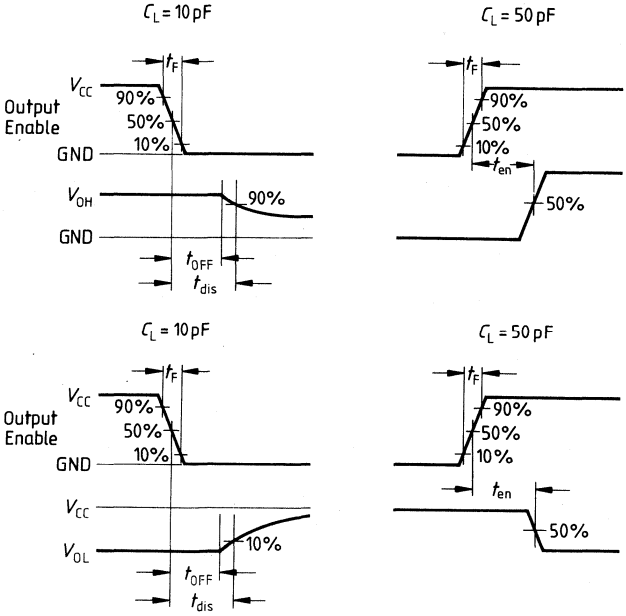


Figure 1
Tristate Measurement Circuits and Pulse Diagrams





Microprocessor Interface

Microprocessor interfacing is straightforward and requires only a few external gates (only one 75LS02).

INTEL Microprocessors

A typical interface is shown in **figure 2.**

Start of conversion

A write instruction selects one of the analog input channels and starts the conversion.

Write address: $\overline{\text{ADC\_CS}}$

The end of conversion-signal (EOC) can be used for producing an interrupt in the microprocessor (INT or $\overline{\text{INT}}$).

Reading the conversion result

With the first read instruction the high byte is read from the $\overline{\text{ADC\_CS}}$ address, with the second read instruction the low byte.

Figure 2

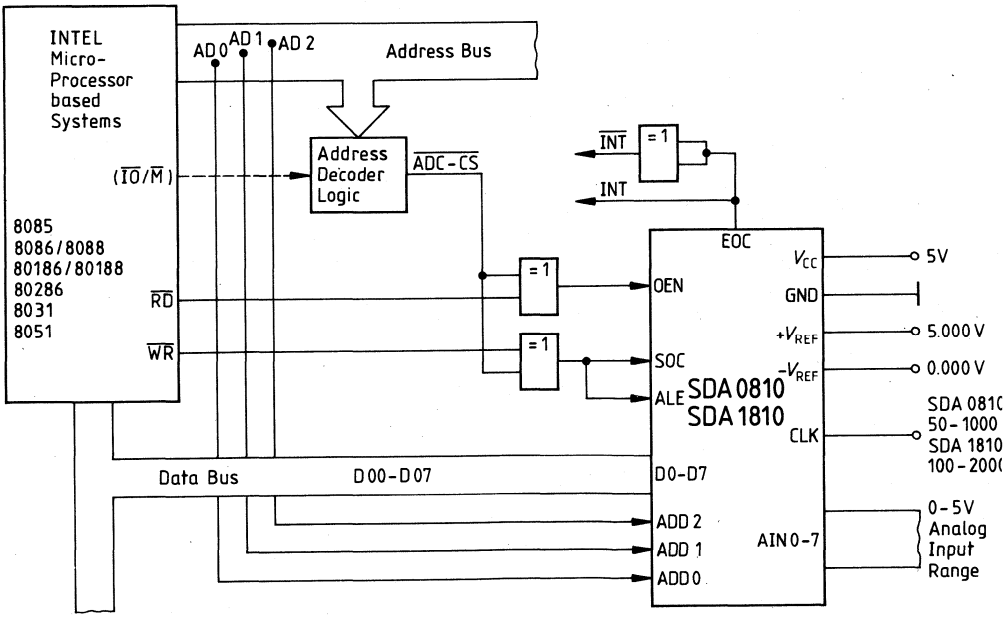
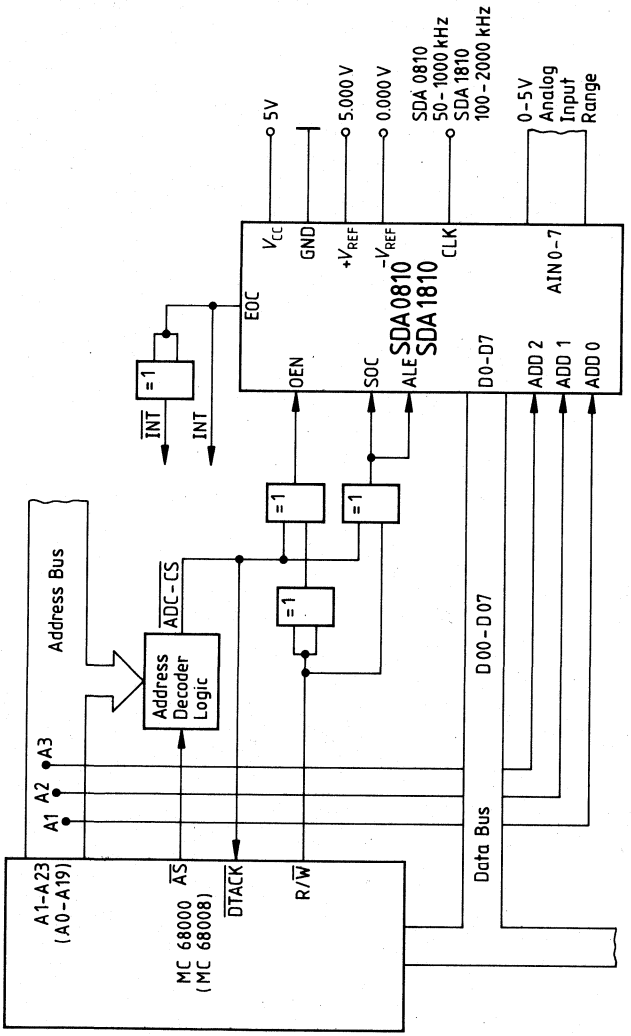


Figure 3
Motorola Microprocessors

A typical interface is shown in **Figure 3.**



Application Hints

Power Supply Decoupling

The power supply of the SDA 0810 or SDA 1810 should be connected with a 10 µF tantalum or an electrolytic capacitor. To ensure good HF performance this capacitor should be connected in parallel with an 0.01 µF ceramic capacitor. These capacitors should be placed as close as possible to the converter.

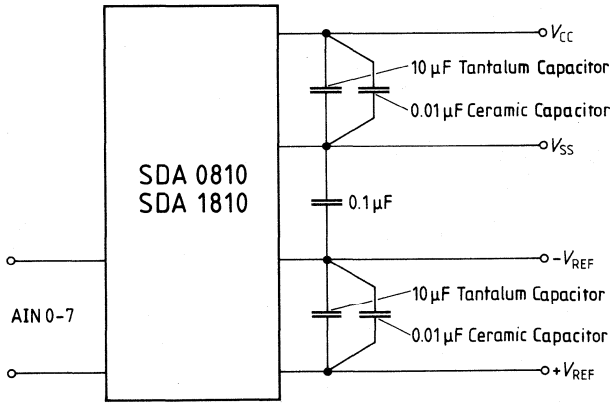
Reference Voltage

To avoid dynamic errors a 10 µF tantalum or electrolytic capacitor connected in parallel with an 0.01 µF ceramic capacitor should be placed as close as possible to the component between pins $+V_{REF}$ and $-V_{REF}$. Also an 0.1 µF ceramic capacitor should be placed between pins $-V_{REF}$ and GND.

Analog Input

The high input impedance of the analog channels AIN 0 to AIN 7 allows simple analog interfacing. Signal sources ($-V_{REF} \leq AIN \leq +V_{REF}$) can directly be connected to the analog input channels, that is without additional buffering, if they are able to supply the current that is necessary to load the sample and hold capacitance being approx. 50 pF, within 4 clock cycles for the SDA 0810 and 8 clock cycles for the SDA 1810.

Figure 4
Capacitors



Bipolar IC

Type	Ordering Code	Package
SDA 8005	Q67000-A2262	C-DIP-16

The SDA 8005 is a high-speed 8-bit D/A converter with ECL-compatible data and strobe inputs.

Features

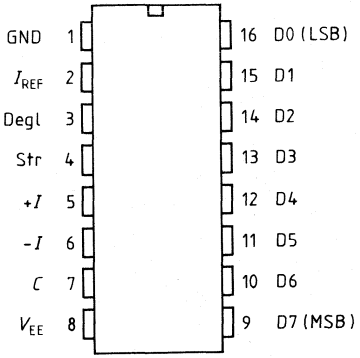
- Settling time typ. 7 ns
- Extremely small glitch area
- Digital input register
- Data inputs 10 K and 100 K-ECL-compatible
- Single power supply −5.2 V
- Deglitch control input

Functional Description

The data word is received in the input buffer with the Low active strobe. An external reference voltage source with a reference resistor is needed. At a reference current of 2.5 mA the full-scale output current amounts to 40 mA.

The output glitches can be minimized by adjusting the deglitch input voltage between −2.3 V and −2.9 V. The deglitch input can also be left unwired.

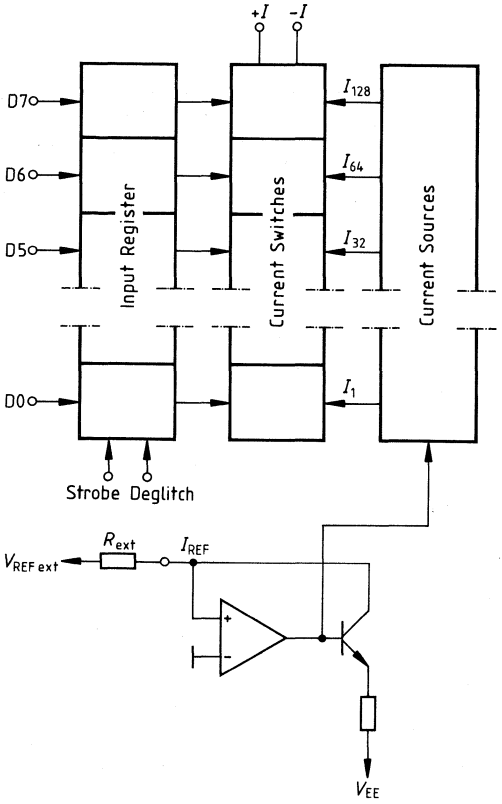
Figure 1
Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	GND	Ground
2 3	I_{REF} Degl	Reference current input Deglitch input
4	Str	Strobe
5, 6	$+I, -I$	Complementary currents outputs $+I$: zero current if D0 to D7 are High
7	C	Stabilization
8	V_{EE}	Supply voltage −5.2 V
16 to 9	D0 to D7	Data input 0 (LSB) to 7 (MSB)

Figure 2
Block Diagram



Maximum Ratings

Description	Symbol	min.	max	Unit
Supply voltage	V_{EE}	−6.0	0.3	V
Input voltage	$V_{D0...D7}$	−3.0	0	V
Strobe input voltage	V_{Str}	−4.0	0	V
Deglitch input voltage	V_{Degl}	−5.2	0	V
Output voltages, $+I$, $-I$	V_{QI+}, V_{QI-}	−1.9	5	V
Junction temperature	T_j		125	°C
Ambient temperature	T_A	−25	85	°C
Storage temperature	T_{stg}	−65	125	°C
Thermal resistance	$R_{th\ JA}$		85	K/W

Characteristics

Description	Symbol	min	typ	max	Unit
Analog Outputs					
Static Performance					
Ratio of full-scale output current to reference current	I_{QFS}/I_{REF}		16		
Absolute unadjusted error	ERR	−1		+1[2])	%
Integral nonlinearity	*I NL*		0.40[1])	0.55[2])	LSB
Differential nonlinearity	*D NL*		0.6[1])	1[2])	LSB
Full-scale temperature coefficient					
−25 °C to +25 °C	*TC*	80		120	ppm/°C
+25 °C to +85 °C	*TC*	50		80	ppm/°C
Zero-code output current	I_{Q0}		6[1])	30[3])	µA
Full-scale output current	$I_{Q\,FS}$			40[2])	mA
Output voltage range	V_Q	−1.4		+5	V
Supply voltage sensitivity	S_{VS}		0.03[1])	0.04[2])	%/%
Dynamic Performance[1])					
Output rise time	$t_{r\,Q}$		1.3		ns
Output setting time	$t_{s\,Q}$		7		ns
Adjusted worst case glitch area			80		pVs
Digital crosstalk attenuation					
Data	α_{Data}		15[4])		pVs
Strobe	α_{Strobe}		30[4])		pVs

For comments see page 435

Characteristics

Description	Symbol	min	typ	max	Unit
Digital Inputs					
DC Characteristics					
H input voltage	V_{IH}	−1.105		−0.810	V
L input voltage	V_{IL}	−1.850		−1.505	V
Input capacitance D7	$C_{I\ D7}$		1.2		pF
D6	$C_{I\ D6}$		0.8		pF
D0 to D5	$C_{I\ D0...D5}$		0.5		pF
Strobe	$C_{I\ Str}$		1.5		pF
H input current D7	$I_{IH\ D7}$		25		µA
D6	$I_{IH\ D6}$		12		µA
D0 to D5	$I_{IH\ D0...D5}$		6		µA
Strobe	$I_{IH\ Str}$		75		µA
Input coding			binary		
Switching Characteristics					
Setup time	t_{setup}	0.5			ns
Hold time	t_{Hold}	2.5			ns
Strobe time (see **figure 3**)	t_{Str}	2			ns
Deglitch Input					
Deglitch input current at $V_{Degl} = 2.3$ V	$I_{I\ Degl}$			200	µA
at $V_{Degl} = 2.9$ V	$I_{I\ Degl}$	−150			µA
Deglitch voltage range	$-V_{Degl}$	+2.9		+2.3	V
Deglitch voltage (not connected)	V_{Dgl}		0.5 x V_{EE}		V
Power Supply[1])					
Supply voltage	V_{EE}	−5.46		−4.94	V
Supply current	I_{EE}		98	105	mA
Power consumption	P_D		495		mW

For comments see page 435

Comments

[1]) Measured at: 25 °C
$V_{EE} = -5.2$ V
Full-scale output current $I_Q = 20$ mA
Output load = 50 Ω

[2]) Guaranteed at: −25 °C to +85 °C
−5.46 V to −4.94 V
Full-scale output current $I_Q = 1$ mA to 40 mA

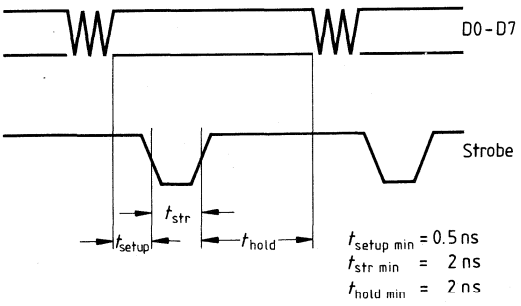
[3]) Measured at 100 °C
Full-scale output current $I_Q = 20$ mA
$V_{Degl} = -2.3$ V
$V_{EE} = -5.2$ V

[4]) $V_{IH} = -0.95$ V
$V_{IL} = -1.6$ V
Input signal rise time $t_r = 3$ ns

Switching all inputs at the same time in the same direction (worst case).

The crosstalk attenuation can be reduced by using other input signals.

Figure 3
Pulse Diagram of the Inputs



Application Hints

- Board containing at least one ground area.
- Ground pin should be connected very close to the large ground area by using contact studs or by direct soldering.
- Voltage supply must be blocked directly at the V_{EE} pin by using a 100-nF ceramic capacitor (preferably small chip capacitors).
- The analog outputs should be loaded with 50 Ω as near as possible to the package.
- Each of the DC voltages (V_{EE}, *DEGL*, V_{REF}) has to be checked for its suitability as regards ripple and noise.
- If a D/A output is connected to the 50-Ω input of an oscilloscope, an attenuator should be arranged on the D/A converter side of the connecting line to prevent the reflection from the oscilloscope from entering the practically open line termination (output impedance of D/A converter approx. 20 kΩ); the ground connection between the board and the instrument should have a very low impedance.
- To minimize crosstalk between the used strobe and the output a voltage divider can be placed at the strobe input to form an RC filter in combination with the input capacitance (see **figure**).

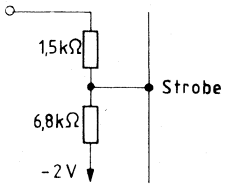
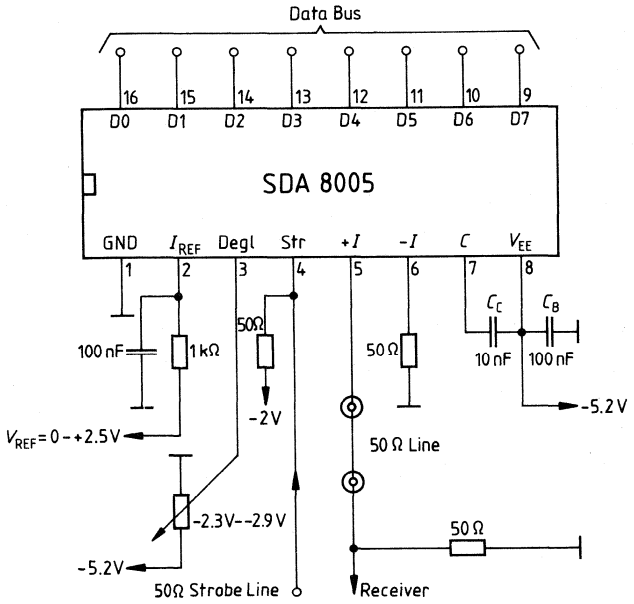


Figure 4 shows an application where the output signal is transmitted over a 50-Ω line to a receiver with a 50-Ω input, possibly a high-speed oscilloscope.

I_{REF} may be adjusted by varying V_{REF} between 0 V and 2.5 V, reference resistor R_{REF} being 1 kΩ.

Alternatively R_{REF} can be changed with V_{REF} constant.

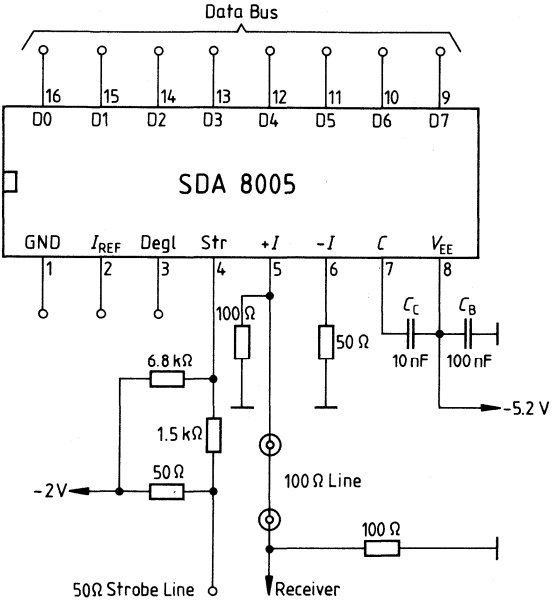
Figure 4



Here the strobe input is connected to a voltage divider, which forms an RC filter together with the input capacitance, and in this way reduces the digital crosstalk from strobe to output. The 100-Ω output line from $+I$ is terminated at both ends.

The high maximum, full-scale output current in this case also allows an acceptable voltage range.

Figure 5



DASR – Data Acquisition Shift Register for HSDA Systems

SDA 8020 N

Preliminary Data

Bipolar IC

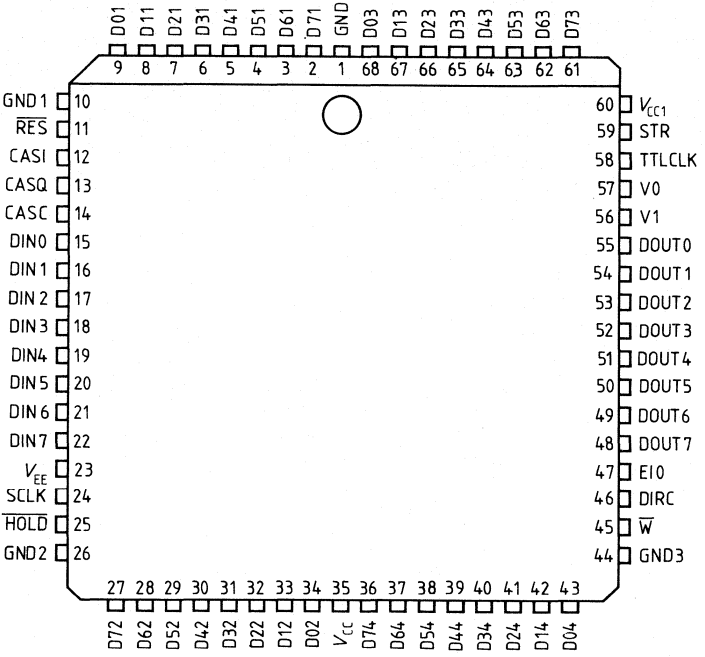
Type	Ordering Code	Package
SDA 8020 N	Q67000-A8127	PL-CC-68 (SMD)

The DASR SDA 8020 N with ECL signal compatible inputs is capable of **DEMULTIPLEXING** an 8-bit wide data stream with a clock rate of up to 100 MHz into four parallel 8-bit TTL data channels with a clock rate one quarter of the serial clock. In a second operating mode a **MULTIPLEX** function combining four 8-bit wide TTL data channels into one 8-bit ECL compatible channel with up to 100 MHz clock rate is provided.

Features

- 4 x 8-bit shift register
- ECL-serial or TTL-parallel loading
- 125 MHz shift clock frequency typically
- Latches for parallel TTL input/output data
- TTL-compatible control pins
- Cascadable, thereby automatically decreasing the TTL clock frequency
- Two clock outputs, TTL CLK and $\overline{W}$, for easy handling
- Interface between high speed ECL and costumary TTL circuits
- Power consumption typically 1.5 W

Figure 1
Pin Configuration
(top view)



Pin Description

Pin	Type	Symbol	I/O	Function
1		GND		TTL data ground
9-2 34-27 43-36 68-61	TTL TTL TTL TTL	D01..D71 D02..D72 D04..D74 D03..D73	I/O I/O I/O I/O	These are the 32 parallel TTL inputs or outputs (dependent on the DIRC input) of the single shift register cells. The fanout of these outputs is 2 TTL loads.
10		GND1		ECL ground
11	TTL	$\overline{\text{RES}}$	I	By activating this input (Low active) all 32 shift register cells are cleared and the clock generator is reset (DOUT 0..7 = Low, TTLCLK = Low, $\overline{\text{W}}$ = High)
12, 13	–	CASI, CASO	I/O	Cascading in, Cascading out **(see figure 4)** These two pins control in connection with the cascading control input the TTL Clock rate and internal strobe timing. Used only to establish the clock loop. They don't provide ECL compatibility.
14	TTL	CASC	I	Cascading control The required logic level at this input depends on the cascading configuration **(see chapter "cascading" and figure 4).** A single chip configuration requires a High level.
15-22	ECL	DIN 0...7	I	ECL data input byte
23		V_{EE}		Negative supply voltage; ECL section
24	ECL	SCLK	I	The single shift register cells are clocked by this signal. Data pending at DIN 0...7 are transferred with the falling clock edge.
25	TTL	$\overline{\text{HOLD}}$	I	A logic Low at the $\overline{\text{Hold}}$ input inhibits the shift clock and sets the 32 parallel I/Os into the High impedance state. The register is inactive.
26		GND2		TTL ground; clock and control section
35		V_{CC}		Positive supply voltage; TTL data section
44		GND 3		Ground for ECL output emitter followers
58	TTL	TTLCLK	O	The frequency of the TTL clock in single chip operation is 1/4 of the shift clock frequency. In a cascaded configuration the TTL clock frequency is automatically decreased.

Pin Description (continued)

Pin	Type	Symbol	I/O	Function
46	TTL	DIRC	I	A logic High on the DIRC configurates the DASR for parallel in/serial out (multiplexing, parallel loading), and a logic Low for serial in/parallel out (demultiplexing, serial loading) operation
47	ECL	EIO	I/O	Enables the internal data transfer from the latches to the shift registers in multiplexing mode. In this mode the EIOs provide internal timing information to all cascaded DASRs. This pin must be connected to −2 V via 1 kΩ resistor **(see figure 4).** In demultiplexing mode the EIO pin has no influence on internal timing and may be left open.
55-48	ECL	DOUT 0...7	O	ECL data output byte. Data are transferred to the output on the falling SCLK edge.
56, 57	TTL	V1, V0	I	With V0, V1 one of four possible delay times of the $\overline{W}$ signal is selected.
45	TTL	$\overline{W}$	O	The $\overline{W}$ output has the same frequency as the TTLCLK but a different duty cycle (1/4 in single chip operation). It may be used as the write or chip select signal for high speed MOS SRAMs which are placed at the parallel inputs/outputs. It can be delayed in multiples of shift clock periods programmable by V0, V1 (see programming table for V0, V1 below).
59	TTL	STR	I	The four 8-bit data words are latched in the first input/second output latch by the Strobe. A high strobe level makes these latches transparent.
60		V_{CC1}		Positive supply voltage; TTL clocks and control signal section.

Programming table for V0, V1

V0	V1	Delay of $\overline{W}$
0	0	0 SCLK period
0	1	1 SCLK period
1	0	2 SCLK periods
1	1	3 SCLK periods

Circuit Description

The DASR contains eight parallel 4-bit deep shift registers, each of them with two internally cascaded level-operated input/output latches. The device has 8 ECL compatible serial inputs and outputs and 32 parallel TTL compatible common inputs/outputs. Beside the data inputs and outputs the device is equipped with 7 mode control inputs and it provides 2 clock signals which especially support the use of the DASR together with fast static MOS RAMs in a data acquisition system. All these inputs and outputs are TTL compatible.

The clock section comprises a 1-bit x 4 shift register whose output (CASO) is fed back to its input (CASI) via the external clock loop. If the cascade control input (CASC) is set to H a single pulse is written into the first shift register cell. When $\overline{\text{HOLD}}$ is released this single clock pulse is moved around the clock loop and all timing signals are derived from this pulse.

The DASR is intended primarily as an interface between a high speed A/D or D/A converter and the memories in a data acquisition or waveform generating system. Further applications are high speed logic analyzers and digital word generators.

Mode of Operation

The DASR has two distinct modes of operation, selected by the DIRC. To avoid excessive power dissipation those circuit parts, which are unused in one mode, are switched off.

1 **Serial IN/Parallel OUT**

After activating the DASR by asynchronous $\overline{RES}$ and $\overline{HOLD}$ **(see figure 5** for recommended $\overline{HOLD}$, $\overline{RES}$ timing), the 8-bit wide ECL data words (present at DIN0...DIN7) are loaded synchronously into the register by the falling SCLK edge. Shortly after every fourth trailing SCLK edge the contents of the single shift register cells are strobed into the first output latch by an internally created clock. These four data bytes appear at the outputs (D01...D71, ...D04...D74) after they are passed to the second output latch by the external STR signal. This latch can also be made transparent by setting STR to H or leaving it unconnected. The first acquired data byte appears at D04...D74, the second at D03...D73, the third at D02...D72 and the fourth at D01...D71. Due to the inherent skew of the latches a falling edge of the external STR must not appear during a short interval ($t_{H,\ STR,\ D}$) after every fourth SCLK period (because output latch 1 has only just been made transparent; **see figure 8**).

An acquisition cycle is finished by a negative $\overline{HOLD}$ level, which is internally synchronized first with the leading TTLCLK edge and secondly with the leading W edge. This double synchronization simplifies stopping the acquisition on a well-defined sample **(see application note, figure 12)**.

There are a few TTLCLK waveforms possible at the end of an operation cycle depending on the delay of $\overline{W}$ **(see figure 5).** $\overline{W}$ remains High after stopping the DASR. When inhibitting SCLK by $\overline{HOLD}$ the TTL data outputs change to the high impedance state.

2 **Parallel IN/Serial OUT**

Synchronous parallel loading is accomplished by applying four 8-bit TTL data words at D01...D74 and taking the STR high.

Every fourth SCLK period, beginning with the 6th falling edge of SCLK after starting operation with a high $\overline{HOLD}$, the second input latch is transparent for one SCLK cycle. With the next falling edge of SCLK the data are written into the shift register cells. The first valid data at DOUT do not appear before the 8th falling edge of SCLK from the beginning onwards. Those data pending at D04...D74 are shifted out first and those at D01...D71 last within a TTLCLK cycle. To obtain defined starting conditions at DOUT, DIN should be set to logic Low. The setup and hold times $t_{S,\ D,\ SCLK}$, $t_{H,\ D,\ SCLK}$ apply only if the first input latch is made transparent by setting STR to H.

In either operating mode the first rising edge of the TTLCLK appears two falling edges of shift clock after activating the DASR. The first $\overline{W}$ pulse with a duration of one SCLK cycle and a delay programmed by V0 and V1 is provided after the third falling edge of SCLK.

Cascading

The ability to cascade the DASR enables lower TTL data rates combined with the advantage of a 100 MHz shift clock. By cascading the DASR the CASO of one device must be connected with the CASI of the next. This clock loop is closed by connecting the CASO of the last DASR with the CASI of the first one. Furthermore the cascading control input (CASC) of one DASR only is set High **(see figure 4)**. The position of the DASR with a high CASC input determines the moment for the internal strobes to transfer data to the second input latch and to the single shift register cells in parallel in/serial out mode **(see figure 7).** The first internal strobes appear at the same time as in single chip operation and their period depends on the length of the shift register cascade. In a system with cascaded DASRs the first edge of $\overline{W}$ or TTLCLK is to transfer at that DASR with CASC = H. The $\overline{W}$ and TTLCLK signals of the other SDA 8020s are provided in the same succession as if they were interconnected via CASI, CASO.

The time delay between the rising edges of the TTLCLK signals is four SCLK periods. In parallel in/serial out mode all EIOs must be tied together and connected to −2 V via a 1 kΩ-resistor. In serial in/parallel out mode the position of the DASR with a High CASC is unimportant for internal timing. In this mode the period of the internal strobe (for output latch 1) is not increased. So the data of the shift registers are strobed to the output latch 1 every fourth SCLK period. To obtain valid TTL output data over the whole TTLCLK period an STR pulse with a duration of a maximum of 4 SCLK periods must be used, e.g.: $\overline{W}$ **(see figure 6).** The signals at the EIOs are for internal use only **(see figure 4).**

The TTL clock High phase of the DASRs with a Low CASC is doubled. When cascading the DASR the $\overline{W}$ signal can be delayed not only in four steps as in the single chip configuration but over the whole TTL clock period by using the $\overline{W}$ output of the appropriate chip.

Figure 2
Functional Block Diagram

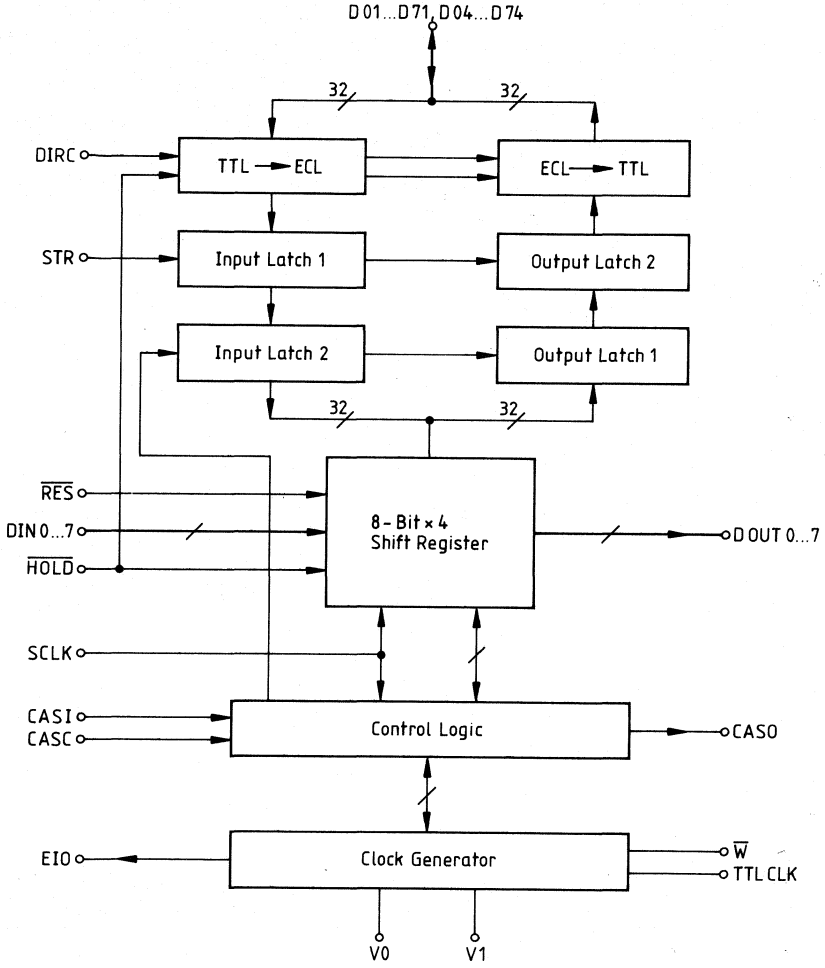
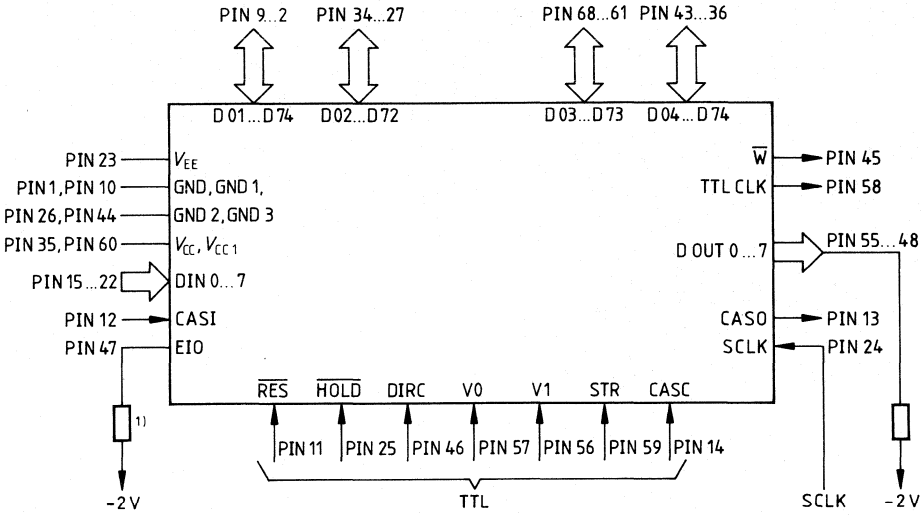


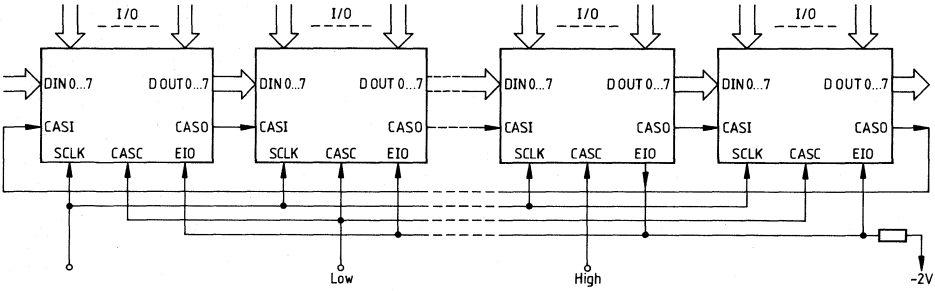
Figure 3
Basic Configuration



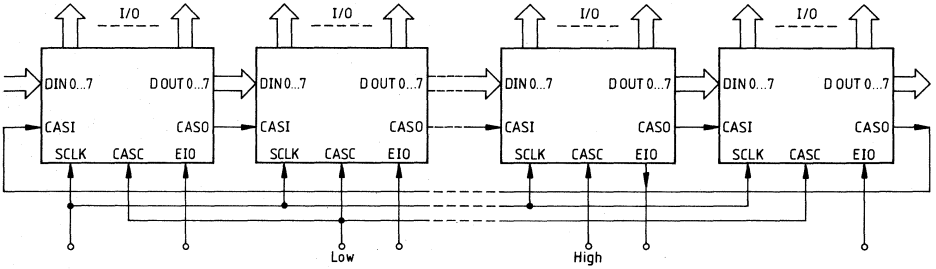
1) Only in multiplexing mode

Figure 4
Cascading Block Diagram

a) Parallel in / serial out



b) Serial in / parallel out



Maximum Ratings

Description	Symbol	min	max	Unit
Positive supply voltage	V_{CC}	−0.3	6.0	V
Negative supply voltage	V_{EE}	−6.0	0.3	V
ECL input voltage		−3.5	0	V
ECL output voltage			1	V
TTL input and output voltage		−0.6	5.5	V
Tristate current into D01...D74			1	mA
Output current at W		−40[1])	40[2])	mA
Output current at D01...D74		−10[1])	10[2])	mA
Output current at TTLCLK		−20[1])	20[2])	mA
Output current at DOUT 0...7		−20	0	mA
Output current at EIO		−10	0	mA
Junction temperature	T_j		125	°C
Ambient temperature	T_A	−25	70	°C
Storage temperature	T_{stg}	−65	125	°C
Thermal resistance				
system – ambient	$R_{th\ SA}$		30	K/W
system – package	$R_{th\ SP}$		15	K/W

[1]) High-State
[2]) Low-State

Electrical Characteristics

$T_A = -25\,°C$ to $+70\,°C$, $V_{CC} = 5\,V \pm 5\%$, $V_{EE} = -4.5\,V \pm 5\%$, $|V_{CC} - V_{CC\,1}| < 0.5\,V$

Description	Symbol	Test conditions	Test circuit	min	typ	max	Unit
Power Supply							
Positive supply current	I_{CC}				65	80	mA
Negative supply current	I_{EE}				240	265	mA
TTL Pins							
H input voltage	V_{IHT}			2			V
L input voltage	V_{ILT}					0.8	V
H input current	I_{IHT}	$V_{CC} = \max$; $V_I = 2.4\,V$				30	µA
L input current	I_{ILT}	$V_{CC} = \max$; $V_I = 0.5\,V$				−1.6	mA
H output voltage	V_{QHT}	$V_{CC} = \min$; $I_{IQH} = -800\,\mu A$	a	2.4			V
L output voltage	V_{QLT}	$V_{CC} = \min$; $I_{QL} = 3.2\,mA$	a			0.5	V
Off-state output current	I_{QZLT}	$V_{CC} = \max$; $V_Q = 0.5\,V$				−50	µA
	I_{QZHT}	$V_{CC} = \max$; $V_Q = 2.4\,V$				50	µA
ECL Pins							
H input voltage	V_{IHE}			−1.165		−0.88	V
L input voltage	V_{ILE}			−1.81		−1.475	V
H output voltage	V_{QHE}		c	−1.025		−0.88	V
L output voltage	V_{QLE}		c	−1.81		−1.62	V
CASI, CASO							
H input voltage	V_{IHC}			−1.0		−0.65	V
L input voltage	V_{ILC}			−1.6		−1.35	V
H output voltage	V_{QHC}				−0.9		V
L output voltage	V_{QLC}				−1.55		V
Maximum load capacity at CASO	C_{CASO}			5			pF

Timing Characteristics

$T_A = -25\,°C$ to $+70\,°C$, $V_{CC} = 5\,V \pm 5\%$, $V_{EE} = -4.5\,V \pm 5\%$, $|V_{CC} - V_{CC\,1}| < 0.5\,V$

Description	Symbol	min	typ	max	Unit
Setup time DIN 0...7 to SLCK	$t_{S,DIN}$	0.5			ns
Hold time DIN 0...7 to SCLK	$t_{H,DIN}$	2.0			ns
Setup time D01...D74 to STR	$t_{S,D}$ [1]	8.0			ns
Hold time D01...D74 to STR	$t_{H,D}$ [1]	0			ns
Setup time Control to $\overline{HOLD}$	$t_{S,CONT}$ [2]	30	7		ns
Hold time Control to $\overline{HOLD}$	$t_{H,CONT}$ [2] [6]	20	0		ns
min. Setup time STR to SCLK	$t_{S,STR,D}$ [1] [3]		−4.5		ns
min. Hold time STR to SCLK	$t_{H,STR,D}$ [1] [3]		6.5		ns
min. Setup time $\overline{HOLD}$ to SCLK	$t_{S,\overline{HOLD},S}$		14	20	ns
Setup time $\overline{HOLD}$ to TTL CLK	$t_{S,\overline{HOLD},T}$	20			ns
Setup time $\overline{RES}$ to $\overline{HOLD}$	$t_{S,\overline{RES}}$	20			ns
min. Setup time STR to SCLK	$t_{S,STR,SLCK}$ [4] [7]		3		ns
min. Hold time STR to SCLK	$t_{H,STR,SCLK}$ [4] [7]		0		ns
min. Setup time D01...D74 to SCLK	$t_{S,D,SCLK}$ [5]		5		ns
min. Hold time D01...D74 to SCLK	$t_{H,D,SCLK}$ [5]		1		ns

For notes see page 452

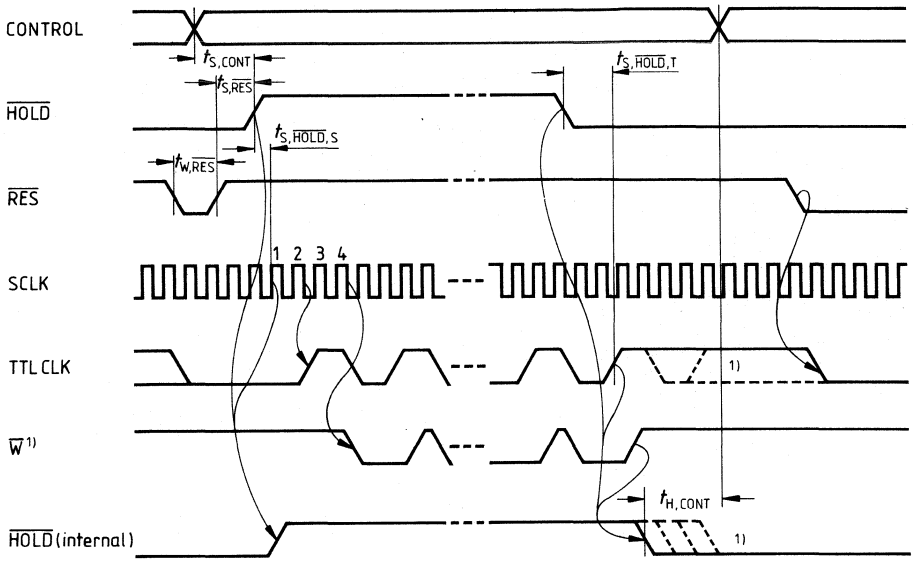
Timing Characteristics (cont'd)

Description	Symbol	Test conditions	Test circuit	min	typ	max	Unit
Delay SCLK – D01...D74	$t_{d,\ SCLK,\ D}$	$R_L = 1200\ \Omega$, $C_L = 15$ pF	a		24		ns
Delay STR – D01...D74	$t_{d,D}$	$R_L = 1200\ \Omega$, $C_L = 15$ pF	a	16.5	21	23	ns
Delay DIRC, $\overline{\text{HOLD}}$-D01...D74	t_{ZL} t_{ZH}	$R_{L1} = 1200\ \Omega$, $C_L = 15$ pF	b		40		ns
Delay DIRC, $\overline{\text{HOLD}}$-D01...D74	t_{HZ}[6], t_{LZ}[6]	$R_{L1} = 1200\ \Omega$, $C_L = 15$ pF	b		25		ns
Delay SCLK – $\overline{W}$	$t_{d\ HL\overline{W}}$	$R_L = 1200\ \Omega$, $C_L = 40$ pF	a		9.5	13	ns
Delay SCLK – $\overline{W}$	$t_{d\ LH\overline{W}}$	$R_L = 1200\ \Omega$, $C_L = 40$ pF	a		9	11	ns
Delay SCLK – TTLCLK	$t_{d\ LH,\ TTLCLK}$	$R_L = 1200\ \Omega$, $C_L = 15$ pF	a		11	13	ns
Delay SCLK – TTLCLK	$t_{d\ HL\ TTLCLK}$	$R_L = 1200\ \Omega$, $C_L = 15$ pF	a		12.5	15	ns
Delay SCLK – DOUT 0...7	$t_{d,\ DOUT}$		c		5	7.5	ns
Delay $\overline{\text{RES}}$ – DOUT 0...7	t_d		c		15		ns
Pulse width of SCLK	t_W			4			ns
Pulse width of $\overline{\text{RES}}$	$t_{W,\overline{\text{RES}}}$			30			ns
Min. pulse width of STR	t_{STR}				6		ns
Max. SCLK frequency	f_{SCLK}			100	125		MHz

Notes

1) Only every 4th SCLK period from the 4th trailing edge onwards
2) Control: Signals DIRC, V0, V1, CASC
3) Doesn't apply if output latch 2 is transparent
4) Doesn't apply if input latch 1 is transparent
5) Only every 4th SCLK period and if input latch 1 is transparent
6) Refers to $\overline{\text{HOLD}}$ after internal synchronization
7) Only every 4th SCLK period from the 7th trailing edge onwards

Figure 5
$\overline{\text{HOLD}}/\overline{\text{RES}}$ Timing



1) Dependent on the programmed delay of $\overline{W}$; solid line shows conditions for V0 = 0, V1 = 0

Figure 6a
Cascading of Two DASRs – Serial IN/Parallel OUT

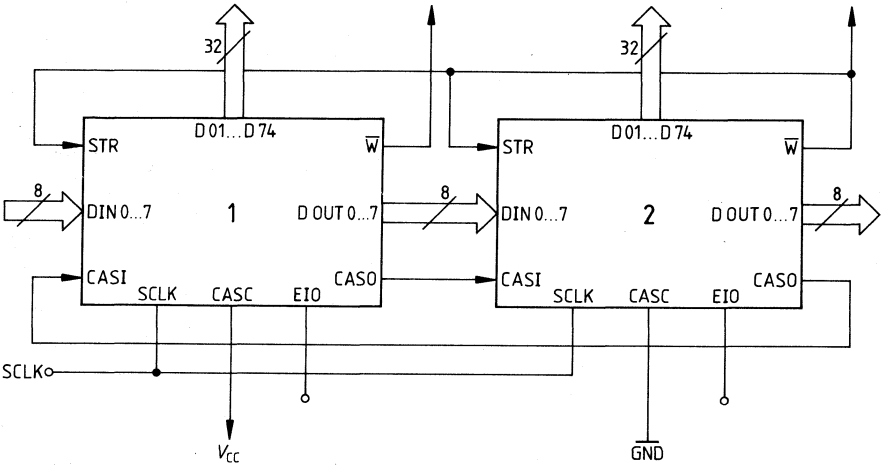
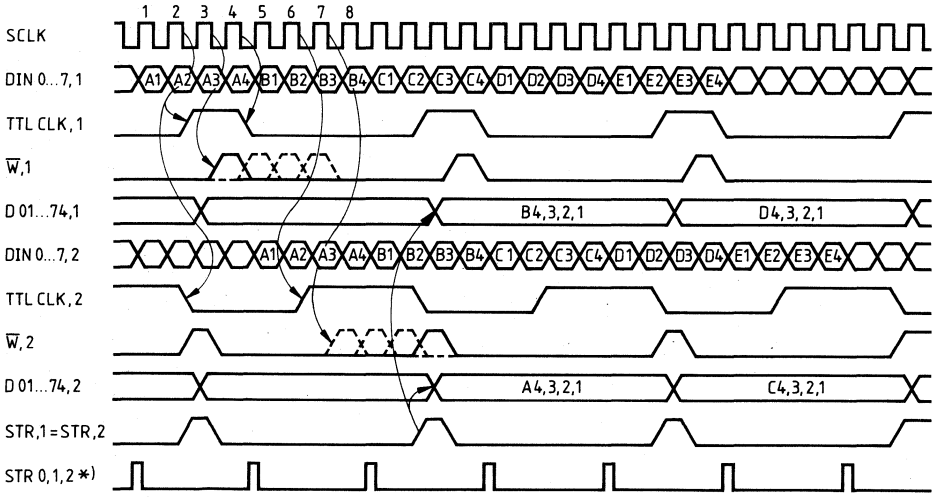


Figure 6b
Cascading of Two DASRs – Serial IN/Parallel OUT



*) Controls output latch 1 of either DASR

Figure 7a
Cascading of Two DASRs – Parallel IN/Serial OUT

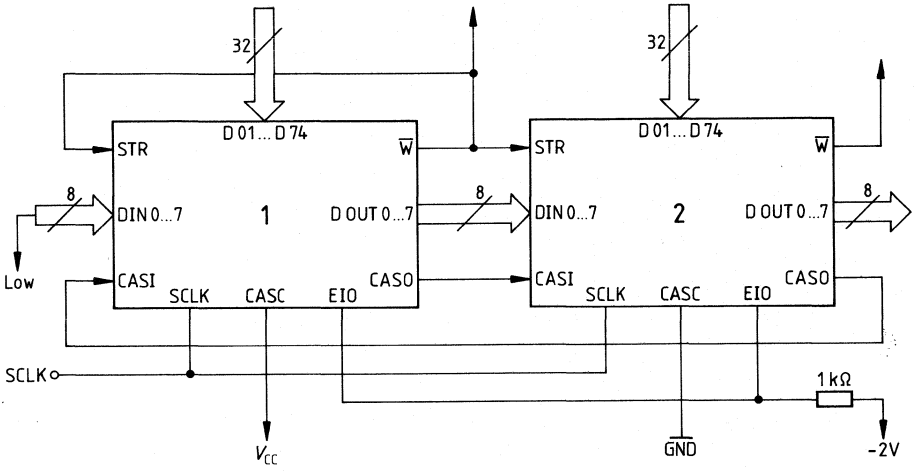
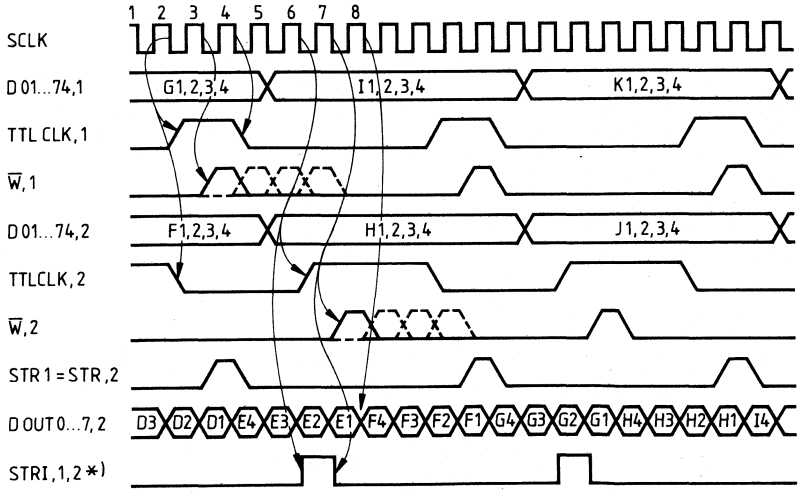


Figure 7b
Cascading of Two DASRs – Parallel IN/Serial OUT



*) Controls input latch 2 of either DASR

Figure 8
Timing Relations for Serial IN/Parallel OUT Operation

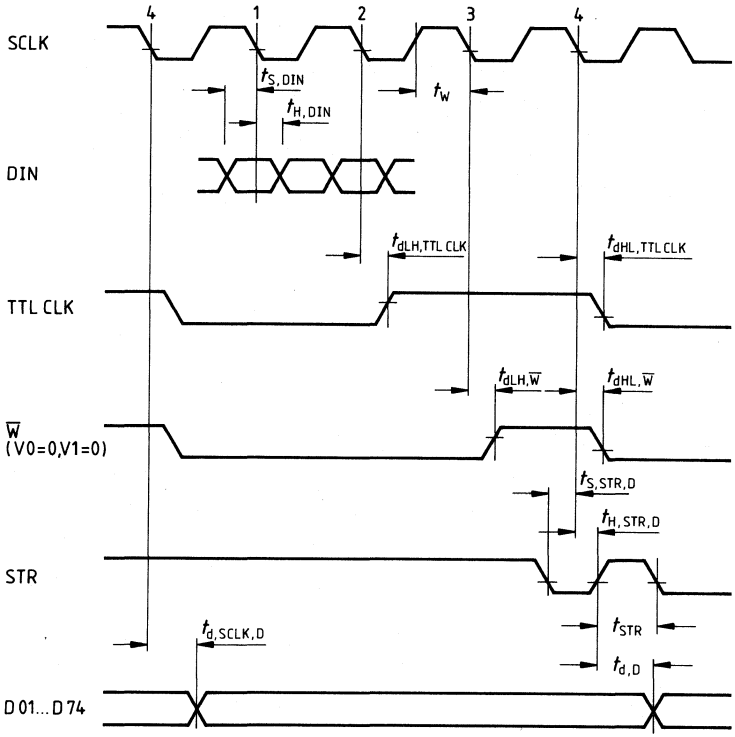


Figure 9
Timing Relations for Parallel IN/Serial OUT Operation

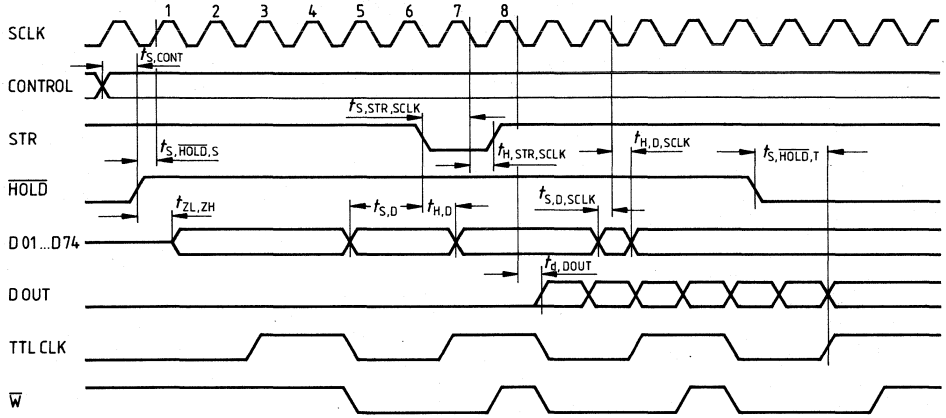
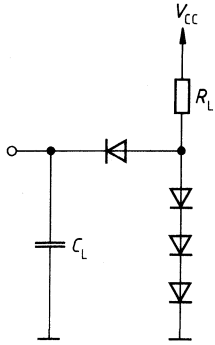
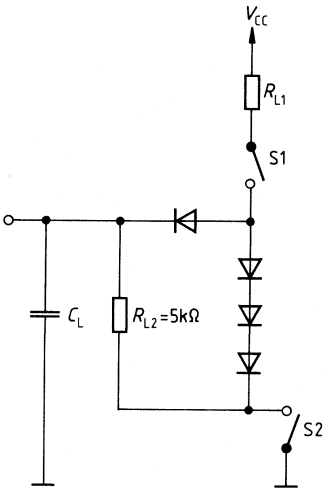


Figure 10
Test Circuits

a)



b)



c)

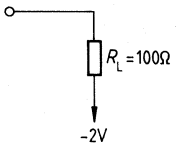
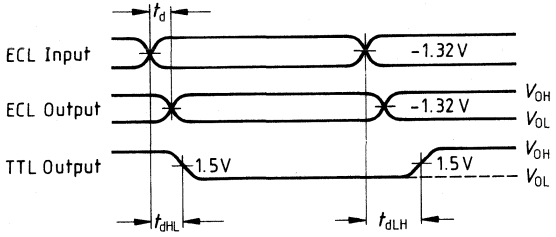
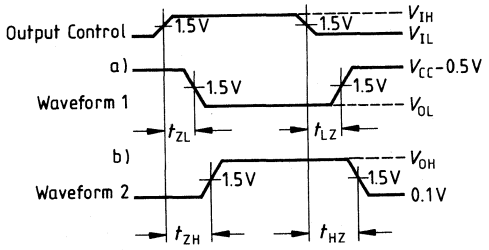


Figure 11
Testing Points

Delay times, setup and hold times



Enable and disable times (Tristate outputs)



a) for an output with internal conditions such that the output is Low except when disabled by the output control

b) for an output with internal conditions such that the output is High except when disabled by the output control

Figure 12
Application Circuit
Data Acquisition System

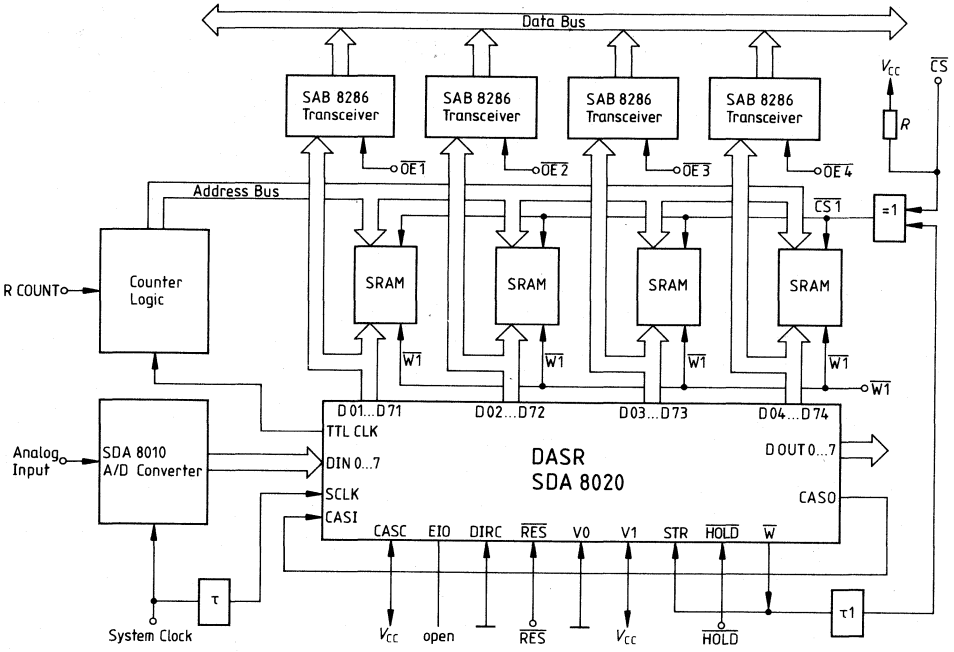
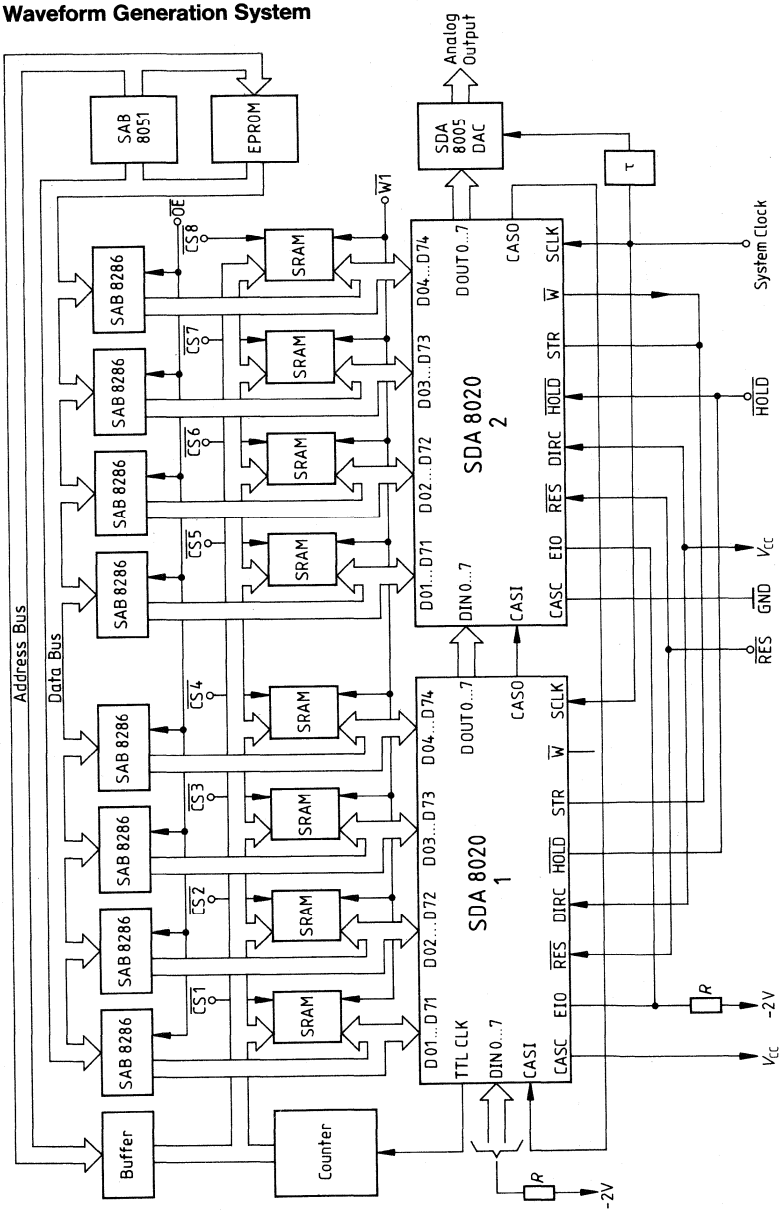


Figure 13
Application Circuit
Waveform Generation System



Timer ICs

Selector Guide

Type	Package	Function
SAB 0529	P-DIP-18	Programmable digital timer
SAB 0529 G	P-DSO-20 (SMD)	Programmable digital timer
SAE 0530	P-DIP-18	Programmable timer for 50 Hz line frequency
SAE 0531	P-DIP-18	Programmable timer for 60 Hz line frequency
SAE 0532	P-DIP-18	Timer for 50/60 Hz line frequency
SAE 0532 G	P-DSO-20 (SMD)	Timer for 50/60 Hz line frequency

Characteristics of Line-Commutated Clock Generators

Feature		SAB 0529	SAE 0530	SAE 0531	SAE 0532
Package		P-DIP-18, P-DSO-20	P-DIP-18, P-DSO-20	P-DIP-18, P-DSO-20	P-DIP-20, P-DSO-20
		same pin configuration			
Line frequency		50 Hz	50 Hz	60 Hz	50/60 Hz switchable
Clock line separated from N pin		no	no	no	yes
Temperature range		0 to 70 °C	−25 to 85 °C		
Response delay at S		for rising edge	for rising and falling edge		
Response delay at R		no	yes		
Timer start behavior when	S = L	no timer start	no timer start		
V_S is applied	S = H	undefined	timer start		
Integrated pull-up resistor to S		no	yes		
Clamping diodes at S		no	yes		
Switching thresholds at A, B, C, S, FC, R		0.6 V	1.8 V		
Switching thresholds at N or FT (SAE 0532)		1,2 V	1.3/1.8 V hysteresis of 0.5 V		
Condition of the pins D to I after reset		L	H		
Output voltage at T at 100 mA		1.8 V	1 V		
Operation as pulse generator		with additional circuit	without additional circuit		

(For further slight deviations refer to characteristics/maximum ratings)

Bipolar IC

Type	Ordering Code	Package
■SAB 0529	Q67000-H2176	P-DIP-18
■SAB 0529 G	Q67000-H2952	P-DSO-20 (SMD)

With the digital timer SAB 0529, delay times between 1 second and 31 1/2 hours can be set. Time base is the 50 Hz line frequency. A triac may be triggered by the SAB 0529 IC.

The SAB 0529 can be programmed to two operating modes: "momentary switching" and "switch-off delay" (according to DIN 46120). In the first mode, a rising edge at the start input activates the triac and starts the timing period. In the switch-off delay mode, the rising edge at the start input activates the triac; but the falling edge starts the timing period.

The versatile IC SAB 0529 covers a great variety of applications, e.g. electronic timers, cooking equipment control, espresso machines, hand-driers, coin changing machines and slot machines, stairwell-light time switches, industrial controls, developing systems for photographic labs, automatic starters (to preheat car engines), and operating-hours counters.

Features

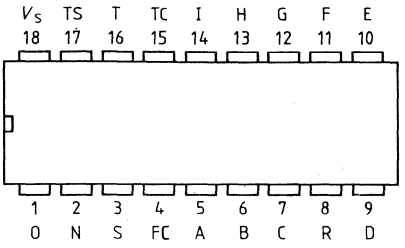
- Direct operation from ac line or dc supply possible
- Time base is 50 Hz line frequency
- Triac triggering with voltage synchronization for resistive loads, or with current synchronization for resistive, inductive and capacitive loads
- Triac gate trigger current up to 100 mA
- Continuous output current to relay actuation max. 100 mA
- 8 overlapping timing periods between 1 second and 31 1/2 hours (at 50 Hz)
- 2 operating modes: momentary switching or switch off delay, both are retriggerable
- Upon request, delay times can be tailored to costumer's specification, requiring only minimum external components. This is possible through mask programming, but is based on minimum order quantities.

■ Not for new design.

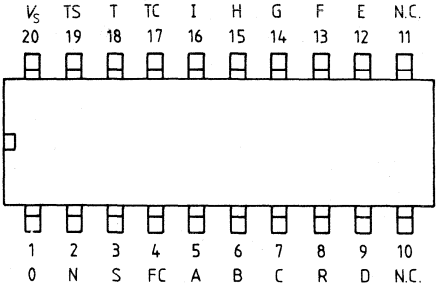
Pin Configurations

(top view)

SAB 0529



SAB 0529 G



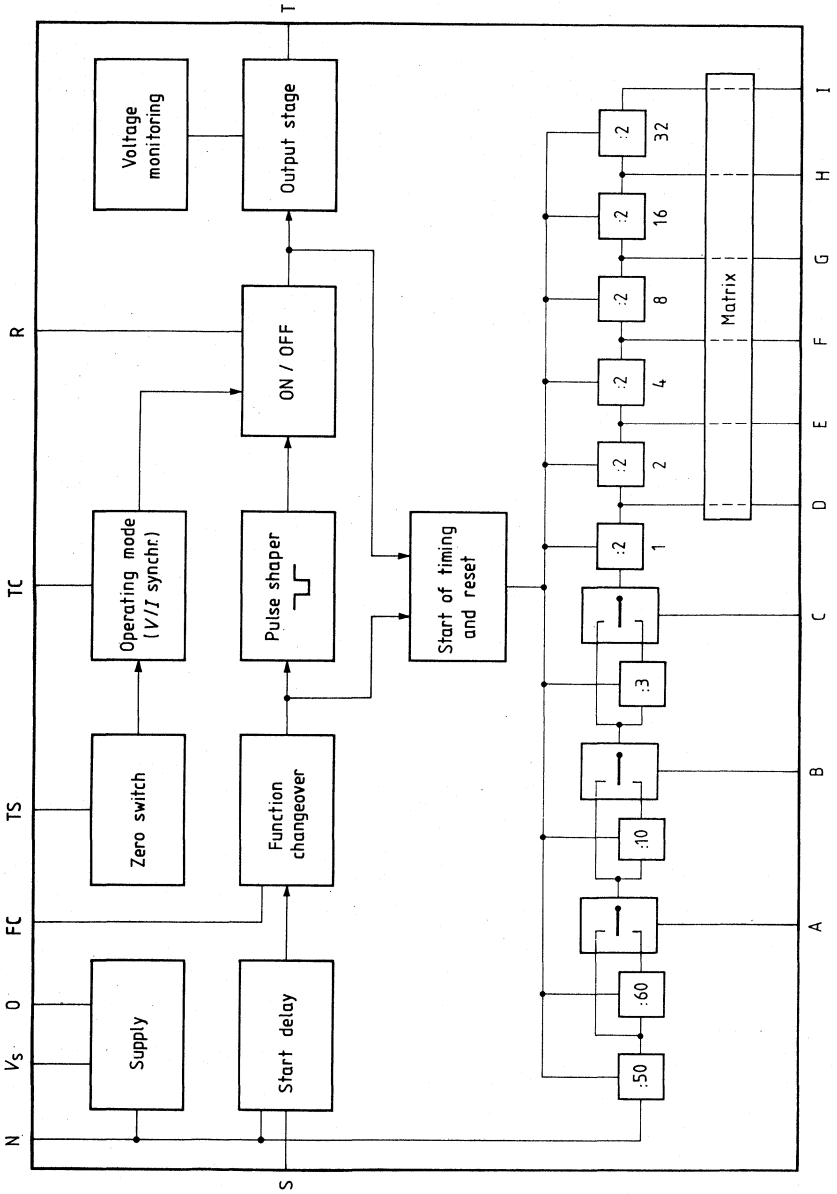
Pin Description

SAB 0529 Pin	SAB 0529 G Pin	Symbol	Function
1	1	0	Circuit ground
2	2	N	Line voltage via series resistor
3	3	S	Start
4	4	FC	Function changeover
5	5	A	Programming of basic timing unit
6	6	B	Programming of basic timing unit
7	7	C	Programming of basic timing unit
8	8	R	Reset
9	9	D	Basic timing unit x 1
10	12	E	Basic timing unit x 2
11	13	F	Basic timing unit x 4
12	14	G	Basic timing unit x 8
13	15	H	Basic timing unit x 16
14	16	I	Basic timing unit x 32
15	17	TC	Triac operation mode setting
16	18	T	Triac triggering
17	19	TS	Triac synchronization
18	20	V_S	Positive supply voltage

These values apply to the standard SAB 0529 version. By mask programming, each of those pins may be assigned a value between 1 and 63.

With the P-DSO-20-L package (SAB 0529 G), pins 10 and 11 are not connected.

Block Diagram



Functional Description

Through division of the line frequency into the portions 1:50, 1:60, 1:10, and 1:3, the basis for 8 timing periods is created. The timing period is selected via inputs A, B, and C, according to the following truth table.

Timing range	A	B	C	Basic timing unit	Max. time at 50 Hz line	
1	L	L	L	1 s	63 s	(approx. 1 min)
2	L	L	H	3 s	189 s	(approx. 3 min)
3	L	H	L	10 s	630 s	(10.5 min)
4	L	H	H	30 s	1890 s	(31.5 min)
5	H	L	L	1 min	63 min	(approx. 1 hr)
6	H	L	H	3 min	189 min	(approx. 3 hrs)
7	H	H	L	10 min	630 min	(10.5 hrs)
8	H	H	H	30 min	1890 min	(31.5 hrs)

L and H potentials are referred to terminal 0, e.g. L = 0, H = V_S

The time basis of the set period is multiplied by the corresponding value in the flipflops 1, 2, 4, 8, 16, 32.

The delay time at output T results from connecting a terminal between D and I with terminal R. Should several of the pins D to I be connected to R, the corresponding delay times are added.

Example

Line frequency = 50 Hz; set range 1 (basic timing unit = 1 s); D, F, and I are connected to R (value 37): resulting delay time is 37 seconds.

Mask Programming of Matrix

Upon request – however, based on a minimum order quantity (of 50,000 items) – assigning any value between 1 and 63 to each pin from D to I in the matrix is possible by mask programming. Thus, individual delay times tailored to the applications are available at those pins, and can be selected by means of a simple multiposition switch.

In such a case, however, it is no longer possible to add delay times when several pins between D and I are connected to R.

Example

Delay times of 3 s, 6 s, 9 s, 12 s, 15 s, and 18 s, at 50 Hz line frequency are required.

With the standard SAB 0529 version the following connections would have to be established (e.g. by a coding switch).

Timing period 2, basic timing unit 3 s: A, B on L potential, C on H potential

3 s: D – R
6 s: E – R
9 s: D – E – R
12 s: F – R
15 s: D – F – R
18 s: E – F – R

Mask programming would establish the necessary connections between pin D to I internally in the matrix, so a simple multiposition switch can select by delay times and connect them to R.

Timing period 2, basic timing unit 3 s: A, B on L potential, C on H potential
e.g. 3 s: D – R
6 s: E – R
9 s: F – R
12 s: G – R
15 s: H – R
18 s: I – R

Reset during a timing period is accomplished by interrupting the connection to *R*, or by applying an H potential to R (in the latter case a protective resistor between R and D through I is necessary as those pins are not protected against short circuit to V_S), or by turning on and off V_S.

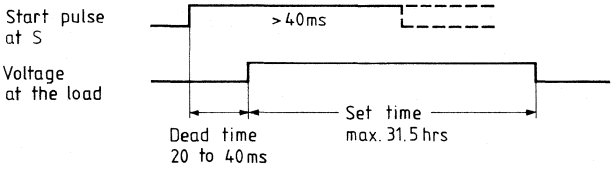
Application note

If R is connected to one of the pins D through I via a multiposition switch, and if during the changeover a reset of the timing period is to be avoided, a suitable capacitor is required between R and 0.

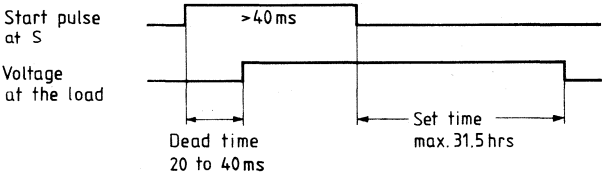
With the **connection of the supply voltage,** the circuit is automatically reset. A timing period does not commence if 0 potential is applied to S.

The SAB 0529 allows two operation modes which are set through pin FC (function changeover):

1. the **"momentary switching function"** in accordance with DIN 46120
   The triac at pin T turns on with the rising edge at the start input S and turns off when the set time has passed, independent of the start pulse length.



2. the **"switch-off delay"** in accordance with DIN 46120
   The triac turns on with the rising edge at S. The falling edge at S starts the timing period. The triac remains in on-state until the set period has passed.



To protect the start input S against external interference and contact bounce, it has a **dead time** of between 20 and 40 ms for its positive switching edge, depending on the phase of the 50-Hz line.

Both operation modes are **retriggerable** during the timing period.

Function Changeover

FC	Function
L	momentary switching
H	switch-off delay

Triac stage

Pin TS (triac synchronization) is the input of a zero voltage switch and serves to synchronize the output T (open collector) with the load voltage or the load current.

With $V_S < 3$ V, the output current is disconnected.

The input TC has a double function:

- to change TS over to voltage synchronization
- to adjust the triac trigger pulse width (by connecting a capacitor C_e to TC) in case of current synchronization.

Three operation modes are possible by varying the connection of the pins TC and/or TS:

Operation mode 1

TC to V_S: Output T is connected to the zero voltage switch. T operates when $V_S - 1.3\ V \leq V_{TS} \leq V_S + 1.3\ V$.

Is utilized in case of voltage synchronization; **see application circuit 1** (operation with resistive load) and **pulse diagram.**

Operation mode 2

TC via C_e to Q: Output T is connected to the zero voltage switch via a monoflop. If $V_S - 1.3$ V is fallen below or $V_S + 1.3$ V exceeded at TS, the output T releases a triac gate trigger pulse determined by C_e.

Is utilized in case of current synchronization; **see application circuit 2** and **pulse diagram.**

Operation mode 3

TC and TS to V_S: Output T conducts after release of start pulse.

Is utilized for any load in case of continuous triac triggering (e.g. low performance), or if any other load is to be operated instead of the triac **(see application circuits 3, 4, 5).**

Operation with line voltage

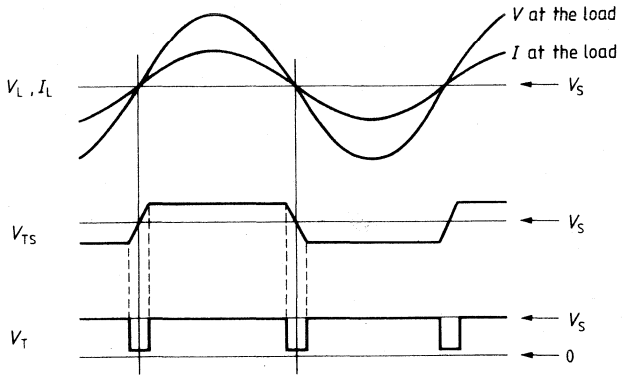
A series resistor R_s and a charging capacitor C_{ch} serve for line voltage supply. If a diode is connected in series with R_s (anode to N), the rms current consumption is halved. The series resistor may also be an *RC* network **(see application circuit 6).**

Operation with dc voltage

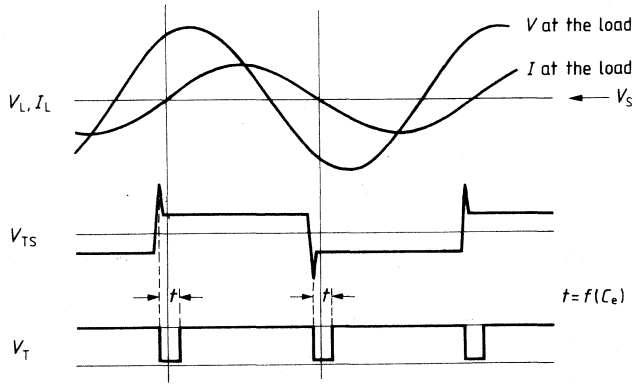
This IC can also be operated with dc voltage or current **(see application circuits 4 and 5).**

Pulse diagrams for triac operation modes 1 and 2

Operation mode 1
Voltage synchronization with resistive loads (TC to V_S)

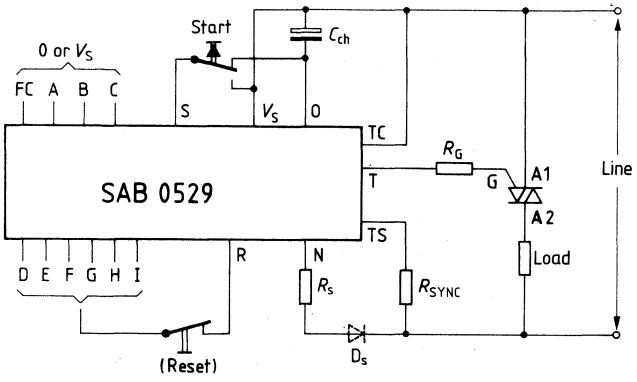


Operation mode 2
Current synchronization with nonresistive loads (capacitance C_e to TC)

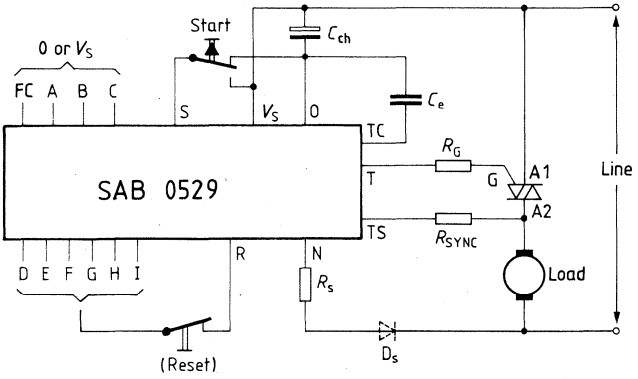


Application Circuits

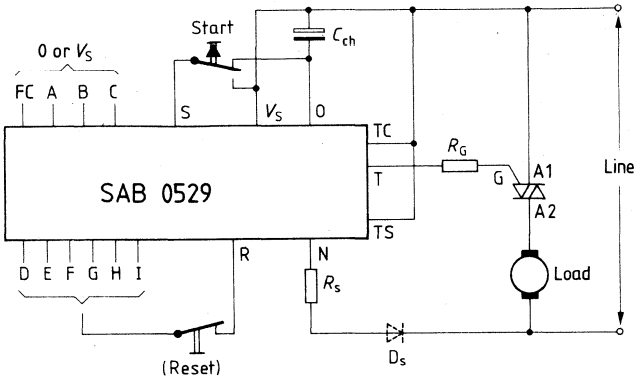
1. Operation with resistive loads



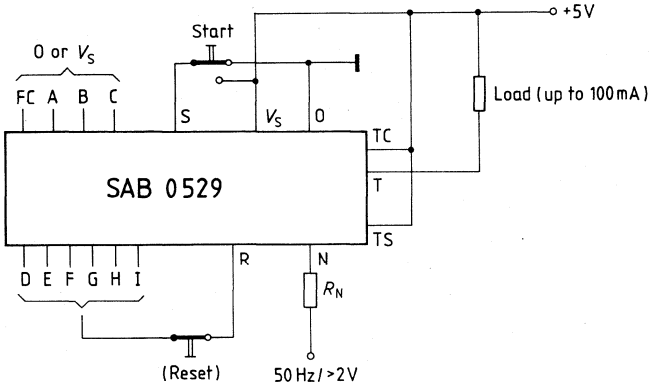
2. Operation with resistive, capacitive, or inductive loads



3. Operation with any load and continuous triac triggering

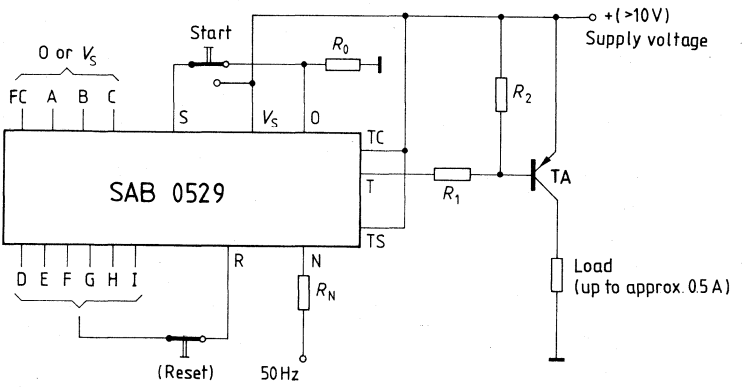


4. Operation with 5 V dc voltage



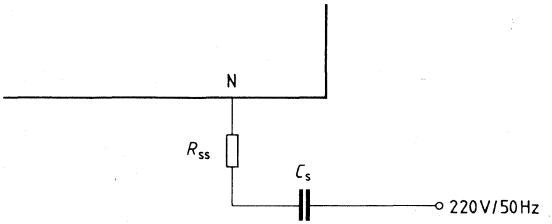
Note: The diode D in **application circuits 1 to 3** must not necessarily be used. This diode, however, may halve the power dissipation at R_S.

5. Operation with dc voltage > 10 V (limited only by transistor TA)



6. Operation with capacitive series resistor

In the **application circuits 1 to 3,** a series connection of R and C may be utilized instead of R_s or R_S and D.



Note: If not required, the reset key may be omitted in **application circuits 1 to 5.**

Dimensioning the application circuits

The following formulae give reference values for operation with sine-shaped ac voltages of 50 Hz. The triac is always triggered in the 2nd and 4th quadrant (negative gate trigger current).

Trigger pulse length Z: $Z = \frac{5 \text{ x holding current}}{\text{rms load current}}$ (ms); applies to $Z \leq 1$ ms

$$R_G = \frac{V_S - V_{ATL} - \text{gate trigger voltage}}{\text{gate trigger current}}$$

$$R_s = \frac{0.5 \text{ x rms line voltage} - V_S}{I_S + \text{average gate trigger current}}$$ (with or without diode D)

average gate trigger current = gate trigger current x $\frac{Z}{10}$ (Z in ms)

Power dissipation at R_s:

$$\text{(without diode D)} = \frac{(\text{rms line voltage})^2}{R_s}$$

$$\text{(with diode D)} = 0.5 \text{ x } \frac{(\text{rms line voltage})^2}{R_s}$$

$$C_{ch} = 20 \text{ x } \frac{\text{rms line voltage}}{R_s}$$ (µF, V, kΩ)

(residual ac voltage at $V_{Spp} \leq 0.5$ V)

Note for C_{ch}

If short-term line failures are to be compensated, C_{ch} has to be accordingly larger (approx. 1000 µF for ≤ 5 s line failure).

Application circuit 1 (voltage sychronization for resistive load)

$$R_{SYNC} = \frac{0.22\ Z \text{ x rms line voltage} - 1.3}{0.04} \geq \frac{\text{peak line voltage}}{4}$$ (kΩ, V, mA, ms)

Notes for application circuit 1

An average I_{TS} of 0.04 mA was inserted into the formula approximating R_{SYNC}.

As $I_{TS}+$ and $I_{TS}-$ contain production deviations, utilizing the determined R_{SYNC} requires certain tolerances to be taken into account for pulse length Z.

To minimize the effect of these tolerances, a resistor may be connected between V_S and TS, which generates a constant current of $\frac{V_{TS}}{R}$ to be added to I_{TS}.

However, a TC of −4 mV/K should be noted for V_{TS}.

Application circuit 2 (current synchronization)

$C_e = 22 \times Z$ (nF, ms)

$$R_{SYNC} \geq \frac{\text{max. on-state voltage} - 1.3}{I_{TSmin}}$$

$$R_{SYNC} \geq \frac{\text{peak line voltage}}{4}$$

} The largest value applies (kΩ, V, mA)

$$R_{SYNC} \leq \frac{\text{gate trigger voltage} - 1.3}{I_{TSmax}} \quad \text{(kΩ, V, mA)}$$

Notes for application circuit 2

In this circuit, an even shorter pulse length than determined for Z is sufficient to trigger the triac. This is possible by the trigger pulse being automatically repeated until the holding current is reached. Overdimensioning of Z for safety reasons is, therefore, not necessary. The disadvantage of multiple trigger pulses, however, is a somewhat larger interference band during the triggering.

The interference band and/or the interference amplitude generated also depend on the amount of the gate trigger voltage necessary to trigger the triac after each current zero passage. That voltage is determined by the size of R_{SYNC} and should not exceed 20 V.

Application circuit 3

Dimensioning of R_s, R_G, and C_{ch} as described at the beginning of this section.

Application circuit 4

$R_N \approx 15 \times$ ac voltage (50 Hz) (kΩ, Vrms)

Application circuit 5

R_N see above. The ac voltage for the timing base must be greater than (supply voltage −4.8 V).

$$R_0 = \frac{\text{supply voltage} - 6.8\ \text{V}}{I_S + I_{R1}} \qquad I_{R1} = I_{B(TA)} + I_{R2}$$

$$R_1 = \frac{6.8\ \text{V} - V_{QTL} - V_{B(TA)}}{I_{R1}} \qquad I_{R2} \approx 0.05\ I_{B(TA)}$$

$$R_2 = \frac{V_{B(TA)}}{I_{R2}}$$

Application circuit 6

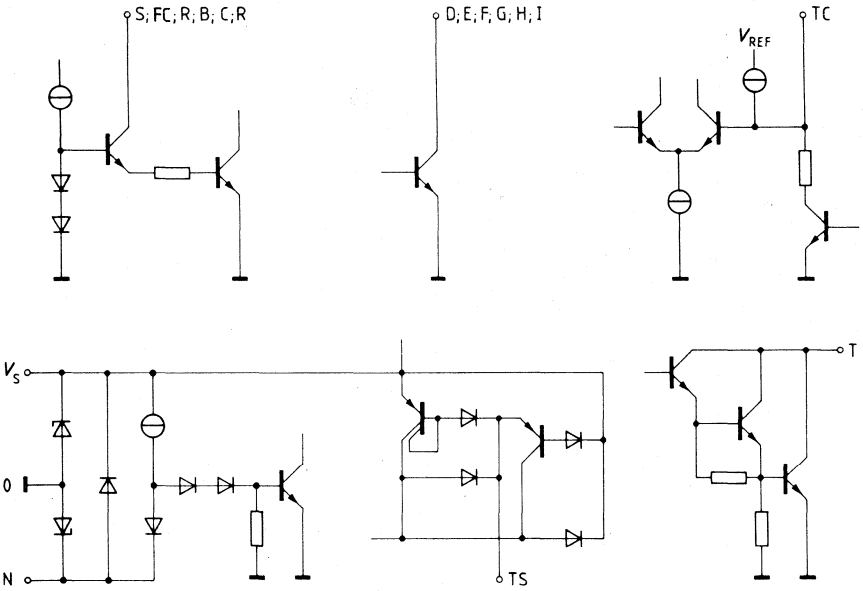
$$C_s = \frac{3.5}{R_s}\ (\mu\text{F, k}\Omega)$$

$$R_{ss} = 0.2\ R_s$$

} applies to 50 Hz

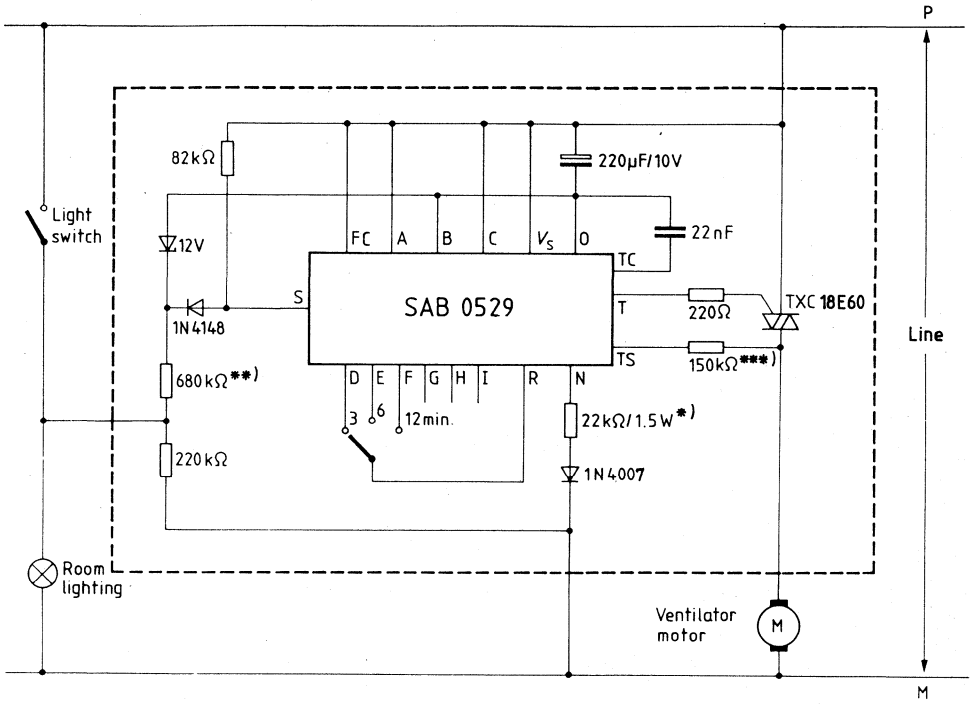
To limit the inrush current, R_{ss} has to be $\geq 0.2\ R_s$. Otherwise, the circuit may be damaged.

Internal connection of inputs, outputs, and supply pins



Typical Application

Time control for ventilator motor, adjustable to 3, 6, or 12 minutes' ventilation



*) for 220 Vac, 10 kΩ for 110 Vac;
**) for 220 Vac, 330 kΩ for 110 Vac;
***) for 220 Vac, 82 kΩ for 110 Vac;
} (high-voltage proof)

Maximum Ratings

Description	Symbol	min	max	Unit	Notes
Supply voltage at impressed dc voltage	V_S	−0.3	5.5	V	
Peak current at N	I_{Np}	−35	35	mA	50 Hz operation
DC from N (rms)	$-I_{Nrms}$		12.5	mA	with $V_S \leq 7.5$ V
AC at N with impressed current	I_{Nrms}		25	mA	50 Hz operation with $V_S \leq 7.5$ V
Voltage at S, FC, A, B, C, R	V	−0.3	7.5	V	
Voltage at N, with N utilized as clock input	V_{NT}	−0.3	V_S	V	
Voltage at TC	V_{TC}	−0.3	V_S	V	
Current at TS	I_{TS}	−4	4	mA	
Voltage at T	V_T	−0.3	7.5	V	
Peak current in T	I_{Tp}		150	mA	1 ms (10 ms interval)
Continuous current in T	I_T		100	mA	
Current in D, E, F, G, H, I	I		0.5	mA	D, E, F, G, H, I on-state
Voltage at D, E, F, G, H, I	V	−0.3	7.5	V	D, E, F, G, H, I off-state
Short-term peak current at N	I_{Np}	−350	350	mA	0.3 ms (100 ms interval) with $C_{ch} > 40$ µF
Junction temperature	T_j		125	°C	
Storage temperature	T_{stg}	−55	125	°C	
Thermal resistance system – air SAB 0529	$R_{th\ SA}$		70	K/W	
SAB 0529 G	$R_{th\ SA}$		105	K/W	

All voltages are referred to pin 0, unless otherwise specified.

Operating Range

Supply voltage at impressed dc voltage Impressed dc or impressed ac at N[2])	V_S	4.5	5.5	V	Voltage between pin 0 and V_S
DC supply from N (rms)	$-I_N$	2,5[1])	12.5	mA	see application circuit
AC supply at N (rms)	I_{Nrms}	5[1])	25	mA	see application circuit
Ambient temperature	T_A	0	70	°C	

1) Only the supply current for the IC, i.e. without triac gate current. The rms gate current additionally flows through N. (The IC may be operated with dc or ac; see also application circuits).
2) The voltage between 0 and V_S is between 5.5 V and 7.0 V for impressed ac and between 6.0 V and 7.5 V for impressed dc. Operation, however, is also assured if V_S falls to 4.5 V (e.g. due to ripple at V_S with dc supply).

Characteristics

$V_S = 4.5$ V to ≤ 5.5 V (7.5 V)[1]), $T_A = 0$ °C to +70 °C

Description	Symbol	Test conditions	min	typ	max	Unit
Supply current at V_S and/or N	I_S	$I_S = -I_N$		1.4	2.5	mA
V_S with impressed current at N:						
Impressed ac	V_S	$I_{N\,rms} = 5$ mA	5.5	6.2	7.0	V
Impressed dc	V_S	$-I_N = 2.5$ mA	6.0	6.8	7.5	V
Switching threshold at:						
A, B, C, S, FC, R	$V_{A...}$		0.3	0.6	1	V
N (if N is clock input)	V_N		0.6	1.2	2	V
TC	V_{TC}			3.5	4.5	V
TS (for voltages $> V_S$)	$V_{TS}+$			$V_S+1.3$		V
TS (for voltages $< V_S$)	$V_{TS}-$			$V_S-1.3$		V
L input current at:						
A, B, C, S, FC, R	$-I_{I\,L}$	$V_{A...} = 0$ V			20	µA
N (if N is clock input)	$-I_{I\,NL}$	$V_N = 0$ V			40	µA
H input current at:						
A, B, C, S, FC, R	$I_{I\,H}$	$V_{A...} = V_S \leq 5.5$ V			20	µA
N (if N is clock input)	$I_{I\,NH}$	$V_N = V_S$			10	µA
TC	$I_{I\,TCH}$	$4.5\text{ V} \leq V_{TC} \leq V_S$			50	µA
Pos. switching current at TS	$I_{TS}+$	$V_{TS} = V_{TS}+$	27	45	81	µA
Neg. switching current at TS	$I_{TS}-$	$V_{TS} = V_{TS}-$	18	30	54	µA
L voltage at D, E, F, G, H, I	V_L	$I_L = 0.5$ mA			0.3	V
Reverse current at D, E, F, G, H, I	I_H				1	µA
L output voltage at T	$V_{Q\,TL}$	$I_T = 1$ mA		1.5	1.8	V
		$I_T = 10$ mA		1.6	2	V
		$I_T = 100$ mA		1.8	2.3	V

[1]) with impressed current at N.

Preliminary Data

Bipolar IC

Type	Ordering Code	Package
SAE 0530	Q67000-H8403	P-DIP-18
SAE 0531	Q67000-H8431	P-DIP-18

SAE 0530 for 50 Hz line frequency
SAE 0531 for 60 Hz line frequency

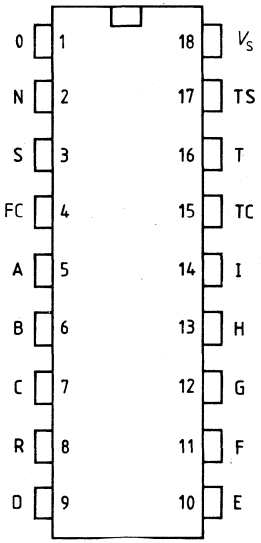
With these programmable timers (at 50-Hz or 60-Hz line frequency, respectively) delay times between 1 second and 31.5 hours can be set. Among other purposes they serve for triggering triacs in an ac line. The power may be supplied either by the ac line or by a dc source. The time base is the line frequency.

The versatile programmable timer covers a great variety of applications, such as electronic timers, cooking equipment control, espresso machines, hand-driers, coin changing machines and slot machines, stairwell-light time switches, industrial controls, developing systems for photographic labs, automatic starters (to preheat car engines), and operating-hours counters.

Features

- Direct operation from ac line or dc supply possible
- Time base is 50/60-Hz line frequency
- Triac triggering with voltage synchronization for resistive loads, or with current synchronization for inductive and capacitive loads
- Triac gate trigger current up to 150 mA
- Continuous output current for relay actuation max. 100 mA
- Input and output delay can be retriggered
- 8 overlapping timing periods between 1 second and 31.5 hours
- Extended temperature range from −25 °C to +85 °C

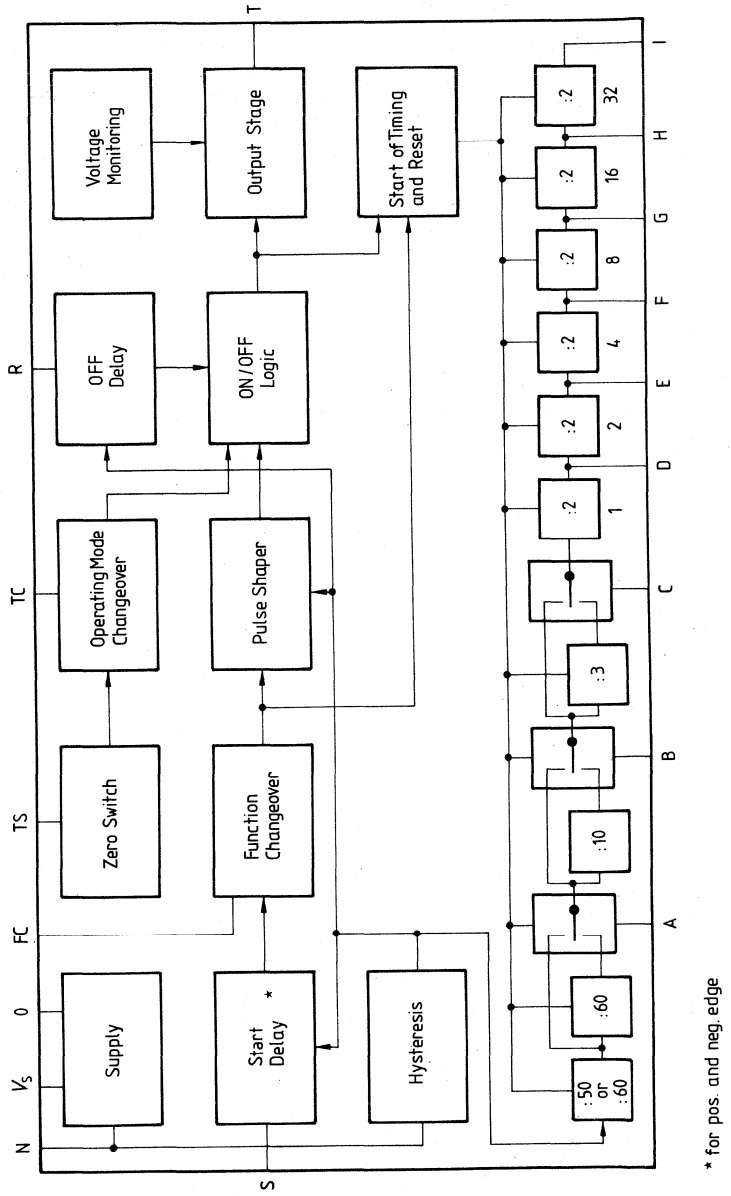
Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	0	Circuit ground
2	N	Line voltage via series resistor
3	S	Start
4	FC	Function changeover
5	A	Programming of basic timing unit
6	B	Programming of basic timing unit
7	C	Programming of basic timing unit
8	R	Reset
9	D	Basic timing unit x 1
10	E	Basic timing unit x 2
11	F	Basic timing unit x 4
12	G	Basic timing unit x 8
13	H	Basic timing unit x 16
14	I	Basic timing unit x 32
15	TC	Triac operation mode setting
16	T	Triac triggering
17	TS	Triac synchronization
18	V_S	Positive supply voltage

Block Diagram



* for pos. and neg. edge

Circuit Description

The clock frequency is applied to N (line voltage via series resistor). Clock input N has a hysteresis of about 0.5 V. Through division of the line frequency into the portions 1:50 (1:60)[1]), 1:60, 1:10, and 1:3 the time basis for 8 timing periods is generated. The timing period is selected via inputs A, B and C, according to the following truth table:

Timing period	A	B	C	Basic timing unit	Max. time
1	L	L	L	1"	1'3"
2	L	L	H	3"	3'9"
3	L	H	L	10"	10'30"
4	L	H	H	30"	31'30"
5	H	L	L	1'	1 h3'
6	H	L	H	3'	3 h9'
7	H	H	L	10'	10 h30'
8	H	H	H	30'	31 h30'

L and H potentials are referred to terminal 0; e.g. L = 0, H = V_S

The time basis of the set period is multiplied in the flipflops 1, 2, 4, 8, 16, 32. The flipflops are connected to the pins D, E, F, G, H, I in such a way that these get a certain value, i.e. the values 1, 2, 4, 8, 16, 32. The desired delay time at output T derives from the following formula: delay time = basic timing unit x value D...I. This time results from connecting the corresponding pins D...I to pin R. Should several of this pins D to I be connected to R, the corresponding delay times are added.

Example

Line frequency = 50 (60)[1]) Hz; set range 1 (basic timing unit = 1 s); D, F and I are connected to R (value 37); the resulting delay time is 37 s.

Function changeover

The circuit allows two operation modes which are set through pin FC (function changeover):

1. **"momentary switching function"** in acc. with DIN 46120.
   The triac at pin T turns on with the **rising edge** at the start input S and turns off when the set time has passed, independently of the start pulse length.
2. **"switch-off delay"** in acc. with DIN 46120.
   The triac turns on with the rising edge at S. The **falling edge** at S starts the timing period. The triac remains in on-state until the set period has passed. Both operation modes are **retriggerable** during the timing period.

FC	Function
L	Momentary switching function
H	Switch-off delay

[1]) Value in parentheses applies to 60-Hz version

To protect the start input S against external interference and contact bounce, it has a **dead time** of between 20 and 40 ms (1/60 to 1/30 s)[1], depending on the phase of the 50 (60)[1] Hz line. To avoid positive and negative voltages the IC is equipped with an internal pull-up resistor and with clamping diodes.

Reset during a timing period is accomplished by interrupting the connection to R, by applying an H potential to R or by turning V_S on and off. The reset input R is equipped with a dead time of 40 ms (1/30 s)[1].

Application note

If R is connected to one of the pins D through I via a multiposition switch, and if a reset of the timing period is to be avoided during the changeover, a suitable capacitor is required between R and 0. This applies only in cases where the interruption is greater than 40 ms (1/30 s)[1].

When the supply voltage is applied the circuit is automatically reset. Whereas no timing period is started when 0 potential is applied to S, a timing period is initiated upon applying S to V_S.

Triac stage

Pin TS (triac synchronization) is the input of a zero voltage switch and is used to synchronize the output T (open collector) with the load voltage or the load current. With $V_S < 3$ V, the output current is disconnected.

The input TC has a double function. It serves for changing TS over to voltage synchronization and for adjusting the triac trigger pulse widrh (by connecting an external capacitor) in case of current synchronization.

Three operation modes are possible by varying the connection of the pins TC and/or TS:

Operation mode 1 (TC to V_S):

Output T is connected to the zero voltage switch. T operates when $V_S - 1.3\ V \leqq V_{TS} \leqq V_S + 1.3\ V$. Is utilized in case of voltage synchronization; **see application circuit 1** (operation with resistive load).

Operation mode 2 (TC via C_e to 0):

Output T is connected to the zero voltage switch via a monoflop. The output T releases a triac gate trigger pulse, determined by C_e, as soon as the voltage at TC decreases below $V_S - 1.3$ V or increases above $V_S + 1.3$ V. Is utilized in case of current synchronization; **see application circuit 2.**

Operation mode 3 (TC and TS to V_S):

Output T conducts after release of start pulse. Is utilized for any load in case of continuous triac triggering (e.g. low performance), or if any other load is to be operated instead of the triac **(see application circuits 3, 4, 5).**

Operation with line voltage

A series resistor R_S and a charging capacitor C_{ch} serve for line voltage supply. If a diode is connected in series with R_S (anode to N), the rms current consumption is halved. The series resistor may also be an RC network **(see application circuit 6).**

Operation with dc voltage

This IC can also be operated with dc voltage or current **(see application circuits 4 and 5).**

[1] Value in parentheses applies to 60-Hz version.

Comments

in general

To obtain better noise immunity the pins D through I, which are not connected, are to be applied to 0.

on C_L

If short-term line failures are to be compensated, C_L has to be accordingly higher.

on application circuit 1 (voltage synchronization for resistive load)

An average I_{TS} of 0.025 mA was inserted into the formula approximating R_{SYN}. As I_{TS+} and I_{TS-} contain production deviations, utilizing the determined R_{SYN} requires certain tolerances to be taken into account for pulse length Z.

on application circuit 2 (current synchronization)

In this circuit, an even shorter pulse length than determined for Z is sufficient to trigger the triac. This is possible by the trigger pulse being automatically repeated until the holding current is reached. Overdimensioning of Z for safety reasons is, therefore, not necessary. A disadvantage of multiple trigger pulses, however, is a somewhat larger interference band during the triggering. The interference band and/or the interference amplitude generated also depend on the amount of the gate trigger voltage necessary to trigger the triac after each current zero passage. That voltage is determined by the size of R_{SYN} and should not exceed 20 V.

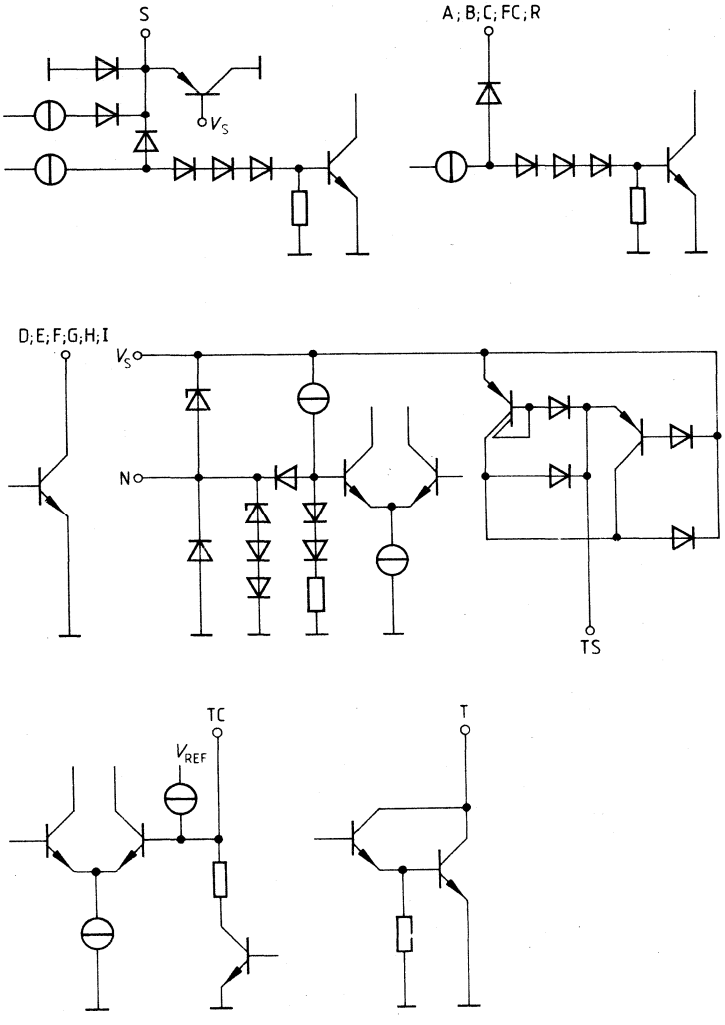
on application circuit 6

To limit the inrush current, R_{SS} has to be $\geq 0.2\ R_S$. Otherwise, the circuit might be damaged.

Dimensioning the application circuits

The following formulae give reference values for operation with sine-shaped ac voltages of 50 Hz or 60 Hz, respectively. The triac is always triggered in the 2nd and 3rd quadrant (negative gate trigger current).

Internal Connection of Inputs, Outputs, and Supply Pins



Maximum Ratings

$T_A = -25\,°C$ to $+85\,°C$

Description	Symbol	min	max	Unit	Notes
Supply voltage[1])	V_S	−0.3	5.5	V	
AC at N[2]) DC from N[2]) Peak current at N[2])	$I_{N\,rms}$ $-I_N$ I_{Np}	 −200	35 18 200	mA mA mA	RMS value Average value 2 ms, 100 ms interval
Voltage at A, B, C, FC, N, R, S, TC Voltage at D, E, F, G, H, I, T Voltage at TS	$V_{A...}$ $V_{D...}$ V_{TS}	−0.3 −0.3 $V_S-0.7$	$V_S+0.3$ 20 $V_S+0.7$	V V V	 D...T off-state
Current in D, E, F, G, H, I Current at S[3]) Continuous current in T Peak current in T Current at TS	$I_{D...}$ I_{InS} I_T I_{Tp} I_{TS}	 −2 −4	0.5 2 100 150 4	mA mA mA mA mA	D...I on-state T on-state 1 ms / 10 ms interval
Junction temperature Storage temperature range Thermal resistance system – air	T_j T_{stg} $R_{th\,SA}$	 −55 	125 125 70	°C °C K/W	

Operating Range

Supply voltage[4])	V_S	4.5	5.5	V	
Supply current (dc)[4]) Supply current (ac)[4])	$-I_N$ $I_{N\,rms}$	2.5 5	18 35	mA mA	[5]) [5])
Ambient temperature	T_A	−25	85	°C	

Notes

1) with impressed voltage at V_S
2) with impressed current at N
3) with impressed current at S
4) The ICs can be operated with impressed voltage or with impressed current. With impressed voltage at V_S, the voltage that is applied can be between 0 and $V_{S\,max}$ 5.5 V (see maximum ratings).
With impressed dc or ac at N, V_S is internally limited and thus ranges between 6 and 8.2 V (typ. 7.5 V). Operation, however, is also ensured if V_S falls to 4.5 V.
5) Only supply current for I_S, i.e. without triac gate current. The rms gate current additionally flows through N.

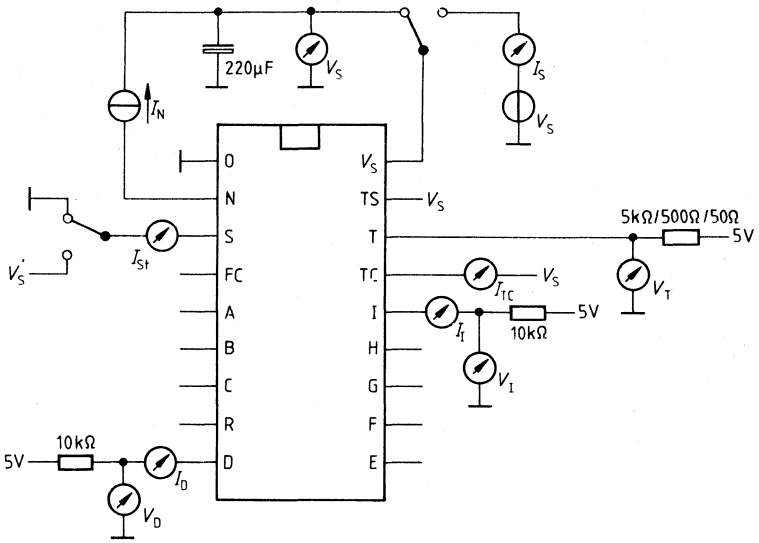
Characteristics

$V_S = 5.5$ V; $T_A = 25$ °C

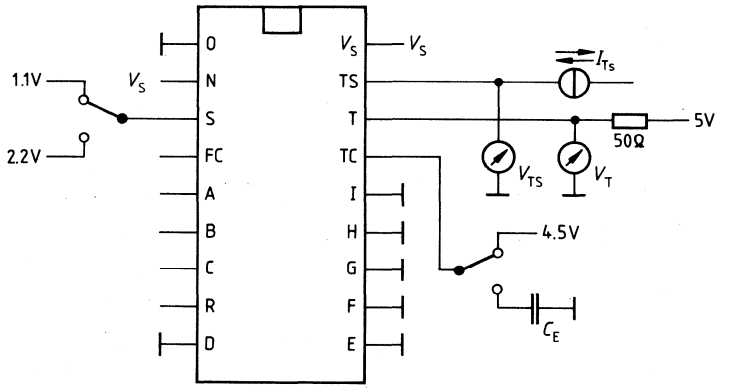
Description	Symbol	Test conditions	Test circuit	min	typ	max	Unit
Supply current[1])	I_S	$V_{IS} = 0$ V	1		1.5	2.5	mA
V_S (impressed dc)[2])	V_S	$-I_N = 2.5$ mA	1		7.5	8.2	V
V_S (impressed ac)[2])	V_S	$I_{N\,rms} = 5$ mA	1		7.5	8.2	V
Voltage at S[3])	V_{IS}	$I_{IS} = 2$ mA				V_S+0.9	V
		$-I_{IS} = 2$ mA		−0.9			V
Switching threshold							
at A, B, C, S, FC, R	$V_{A...}$		2	1.1	1.8	2.2	V
H switching threshold at N[4])	V_N		2		1.8	2.4	V
L switching threshold at N[4])	V_N		2	0.8	1.3		V
Switching hysteresis at N	V_{HY}		2	0.4	0.5	0.9	V
Switching threshold at TC	V_{TC}		2		3.4	4.5	V
Switching threshold at TS	V_{TS+}	$V_{TS} > V_S$	2		V_S+1.3		V
	V_{TS-}	$V_{TS} < V_S$	2		V_S−1.3		V
L input current at A,B,C,FC,R	$I_{A...}$	$V_{A...} = 0$ V	1		20	30	µA
L input current at S	$-I_{IS}$	$V_{IS} = 0$ V	1		60	90	µA
L input current at N[4])	$-I_N$	$V_N = 0$ V	1		40	60	µA
H input current at A,B,C,S,FC,R	$I_{A...}$	$V_{A...} = V_S$	1			1	µA
H input current at N[4])	I_N	$V_N = V_S$	1			1	µA
H input current at TC	I_{TC}	$4.5 \le V_{TC} \le V_S$	1		20	40	µA
Pos. switch-over current at TS	I_{TS+}	$R_{Syn} = 0$	2	20	25	35	µA
Pos. switching hysteresis at TS	I_{Hy+}	$R_{Syn} = 0$	2	1	2	4	µA
Neg. switch-over current at TS	I_{TS-}	$R_{Syn} = 0$	2	20	25	35	µA
Neg. switching hysteresis at TS	I_{Hy-}	$R_{Syn} = 0$	2	1	2	4	µA
L voltage at D, E, F, G, H, I	$V_{D...}$	$I_{D...} = 0.5$ mA	1		0.2	0.4	V
H reverse current at D,E,F,G,H,I	$I_{D...}$		1			1	µA
L output voltage at T	V_Q	$I_T = 1$ mA	1		0.7	1.1	V
	V_Q	$I_T = 10$ mA	1		0.8	1.2	V
	V_Q	$I_T = 100$ mA	1		1	1.5	V

[1]) with impressed voltage at V_S
[2]) with impressed current at N
[3]) with impressed current at S
[4]) if N is clock input

Measuring Circuit 1

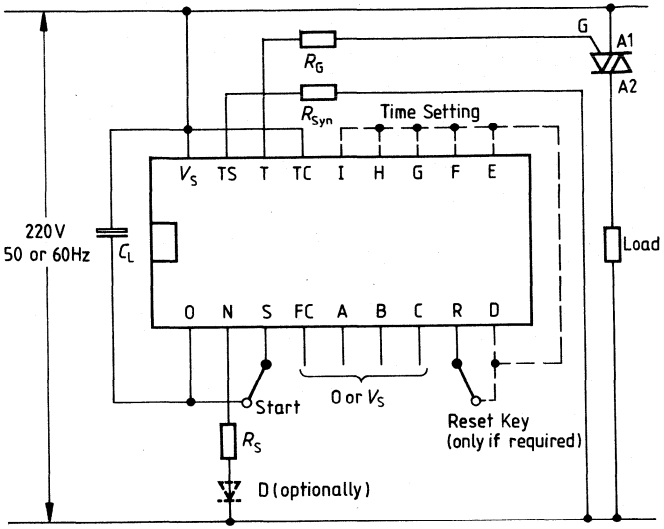


Measuring Circuit 2



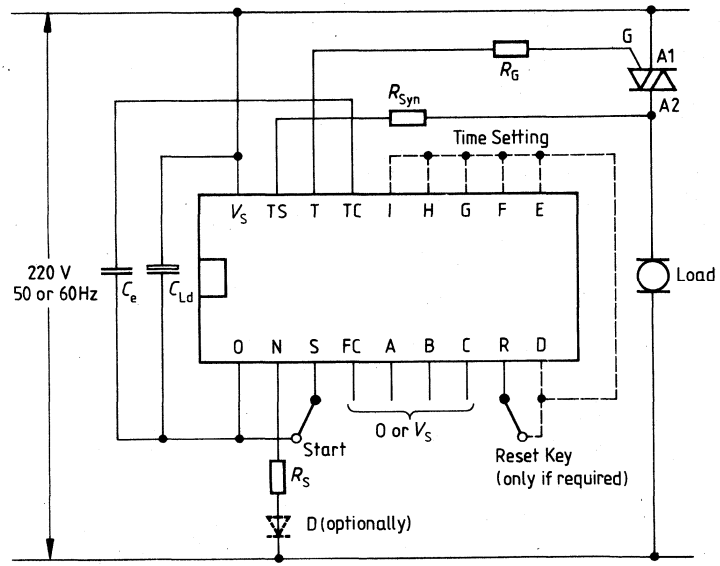
Application Circuit 1

Operation with resistive load



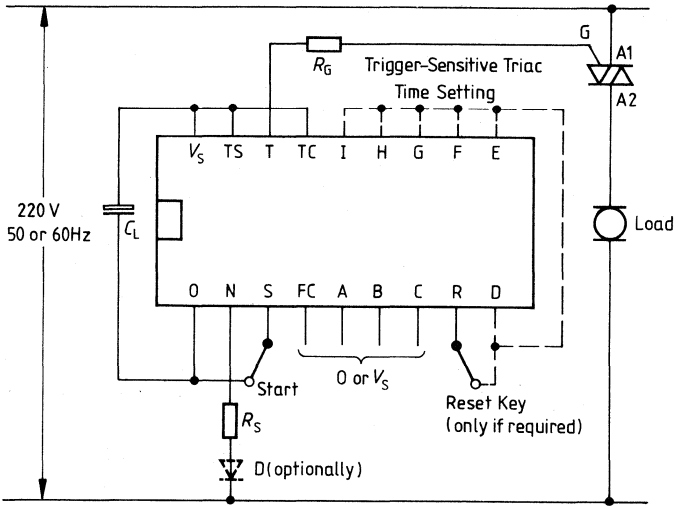
Application Circuit 2

Operation with resistive, capacitive and inductive load



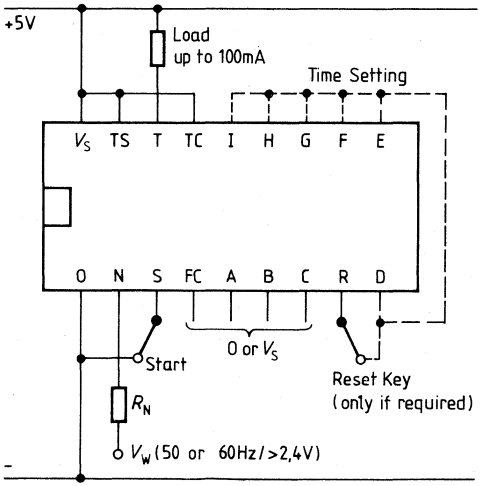
Application Circuit 3

Operation with any load and continuous triac triggering



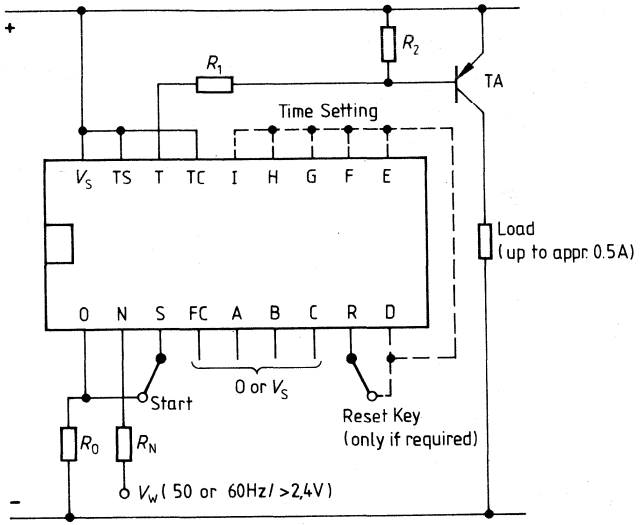
Application Circuit 4

Operation with 5 V dc voltage



Application Circuit 5

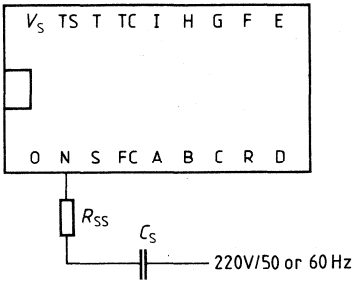
Operation with dc voltage > 5.5 V



Application Circuit 6

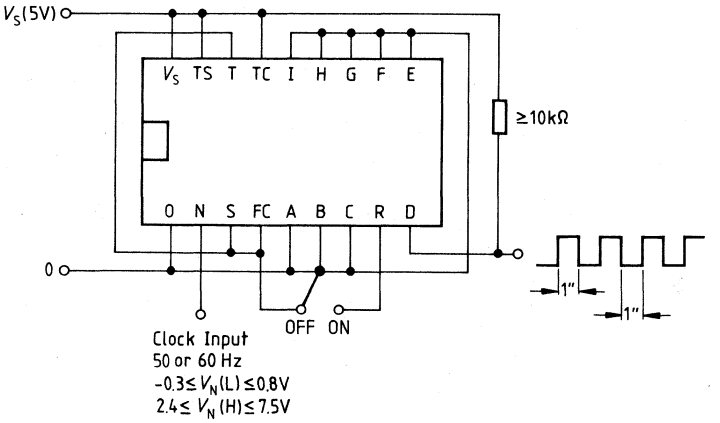
Operation with capacitive series resistor

In the **application circuits 1 to 3** a series connection of R and C may be utilized instead of R_S or R_S and D.



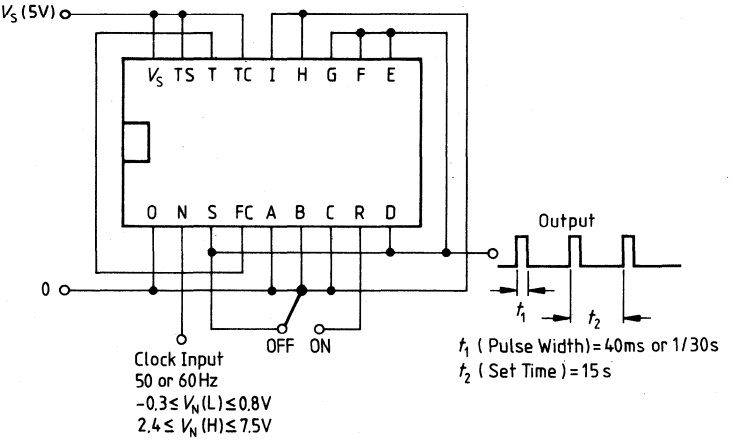
Application Circuit 7

Square wave generator



Application Circuit 8

Pulse generator



Note

The pulse width t_1 is exclusively determined by the clock frequency f at the input FT:

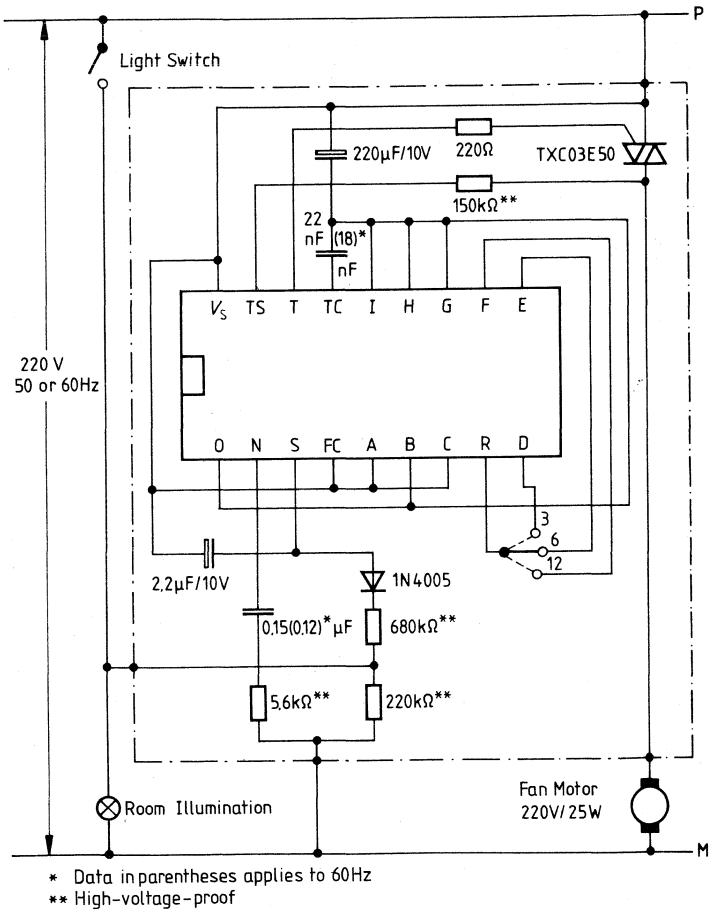
$$t_1 = 2/f = 2/50 \text{ (or } 2/60) = 40 \text{ ms (or } 1/30 \text{ s)}$$

Thus, immediately after turning on the first pulse t_1 and consequently the first time period t_2 could be up to 20 ms (1/60 s) shorter (depending on the phase of the 50/60 Hz line).

As soon as the IC has been turned on, the output T becomes conductive and remains on L-potential during operation.

Application Circuit 9

Time control for a ventilation, can be set to 3, 6 or 12 minutes follow-up time



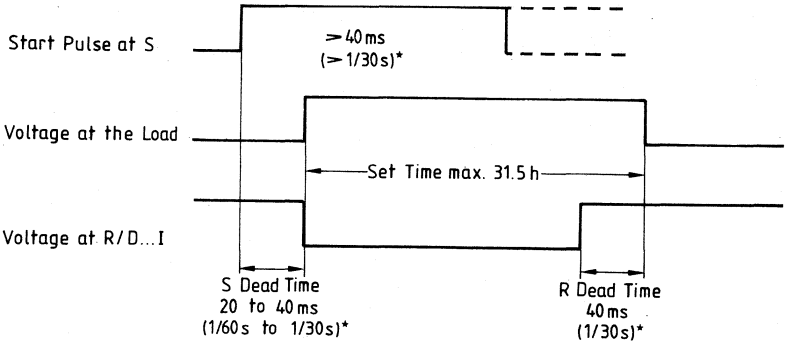
* Data in parentheses applies to 60Hz
** High-voltage-proof

Function of the circuit

The fan motor is started by turning on the room illumination and is automatically turned off 3 (6, 12) minutes after the lighting is turned off. (Dimensioning of the external wiring is not binding and subject to change without notice).

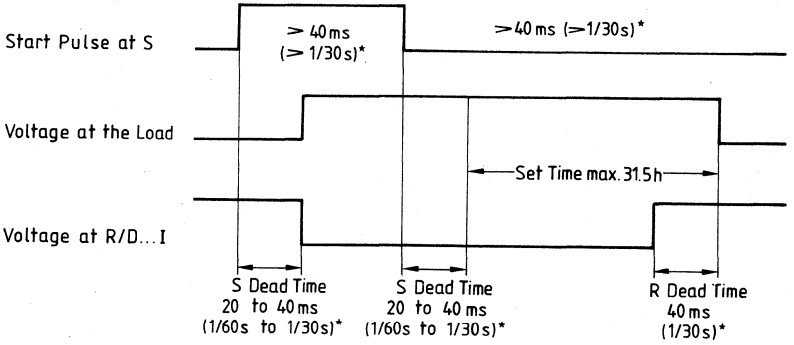
Pulse Diagrams of the Time Operation Modes

Momentary switching function



* Data in Parentheses Applies to 60-Hz Version

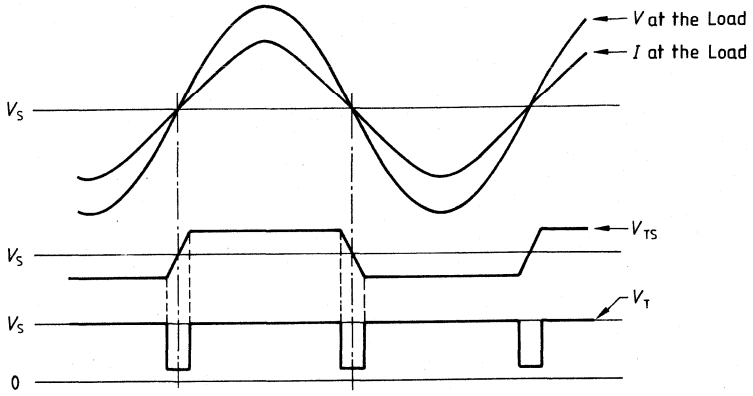
Switch-off delay



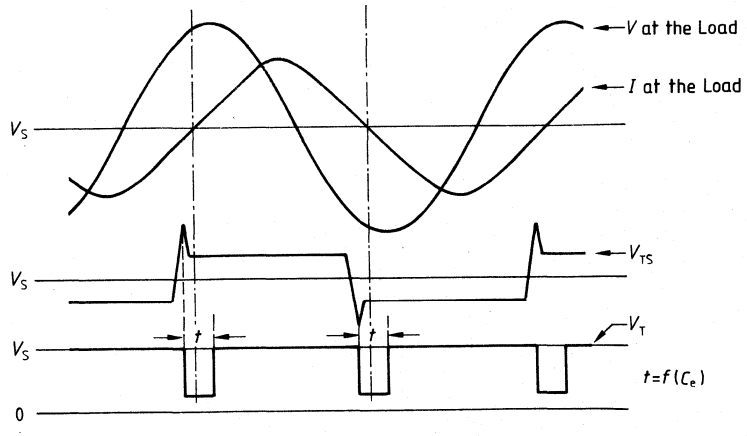
* Data in Parentheses Applies to 60-Hz Version

Pulse Diagrams for Triac Operation Modes 1 and 2

Operation mode 1: Voltage synchronization with resistive loads (TC at V_S)



Operation mode 2: Current synchronization with non-resistive loads
(Capacitance C_e at TC)



Preliminary Data **Bipolar IC**

Type	Ordering Code	Package
SAE 0532	Q67000-H8404	P-DIP-20
SAE 0532 G	Q67000-H8432	P-DSO-20 (SMD)

With this 50/60-Hz programmable timer (at 50-Hz or 60-Hz line frequency, respectively) delay times between 1 second and 31.5 hours can be set. Among other purposes it serves for triggering triacs in an ac line. The power may be supplied either by the ac line or by a dc source. The time base is either the 50 Hz/60 Hz line frequency (FT connected to N) or an oscillator connected to FT.

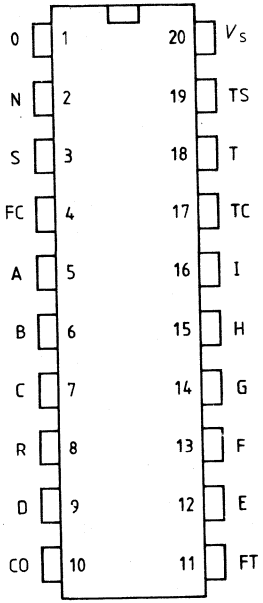
The versatile programmable timer covers a great variety of applications, such as electronic timers, cooking equipment control, espresso machines, hand-driers, coin changing machines and slot machines, stairwell-light time switches, industrial controls, developing systems for photographic labs, automatic starters (to preheat car engines), and operating-hours counters.

Features

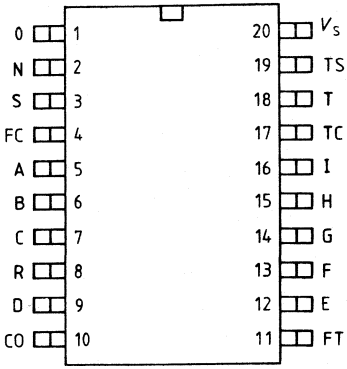
- Direct operation from ac line or dc supply voltage
- Can be changed over to 50 Hz or 60 Hz line frequency as time base
- Triac triggering with voltage synchronization for resistive loads, or with current synchronization for resistive, inductive and capacitive loads
- Triac gate trigger current up to 100 mA
- Continuous output current for relay actuation max. 100 mA
- Two operation modes, can be retriggered
- 8 overlapping timing periods between 1 second and 31.5 hours
- Extended temperature range from −25 °C to +85 °C

Pin Configurations
(top view)

SAE 0532



SAE 0532 G



Pin Description

Pin	Symbol	Function
1	0	Circuit ground
2	N	Line voltage via series resistor
3	S	Start
4	FC	Function changeover
5	A	Programming of basic timing unit
6	B	Programming of basic timing unit
7	C	Programming of basic timing unit
8	R	Reset
9	D	Basic timing unit x 1
10	CO	50/60-Hz changeover
11	FT	Clock input
12	E	Basic timing unit x 2
13	F	Basic timing unit x 4
14	G	Basic timing unit x 8
15	H	Basic timing unit x 16
16	I	Basic timing unit x 32
17	TC	Triac operation mode setting
18	T	Triac triggering
19	TS	Triac synchronization
20	V_S	Positive supply voltage

Circuit Description

The timer's prescaler is changed over by the pin CO, thus all specified times apply to the corresponding line frequency.

CO	Line frequency
L	60 Hz
H	50 Hz

The clock frequency is applied to FT. Normally it is the line frequency that supplies the clock. For this purpose FT is connected to N. In order to obtain an adequate interference suppression, FT is designed as Schmitt Trigger with a hysteresis of about 0.5 V. In case of severe line interference a filter (e.g. RC network) should be placed between N and FT.

Through division of the line frequency into the portions 1:50/60, 1:60, 1:10 and 1:3 the time basis for 8 timing periods is generated. The timing period is selected via inputs A, B and C, according to the following truth table:

Timing period	A	B	C	Basic timing unit	Max. time
1	L	L	L	1"	1' 3"
2	L	L	H	3"	3' 9"
3	L	H	L	10"	10' 30"
4	L	H	H	30"	31' 30"
5	H	L	L	1'	1 h 3'
6	H	L	H	3'	3 h 9'
7	H	H	L	10'	10 h 30'
8	H	H	H	30'	31 h 30'

L and H potentials are referred to terminal 0; e.g. L = 0, H = V_S

The time basis of the set period is multiplied in the flipflops 1, 2, 4, 8, 16, 32. The flipflops are connected to the pins D, E, F, G, H, I in such a way that these get a certain value, i.e. the values 1, 2, 4, 8, 16, 32. The desired delay time at output T derives from the following formula: basic timing unit x value D...I. This time results from connecting the corresponding pins D...I to pin R. Should several of the pins D to I be connected to R, the corresponding delay times are added.

Example

Line frequency = 50 Hz (CO = H); set range 1 (basic timing unit = 1 s); D, F and I are connected to R (value 37); the resulting delay time is 37 s.

Function changeover

The circuit allows two operation modes which are set through pin FC (function changeover):

FC	Function
L	Momentary switching function
H	Switch-off delay

1. **"Momentary switching function"** in acc. with DIN 46120.
   The triac at pin T turns on with the **rising edge** at the start input S and turns off when the set time has passed, independently of the start pulse length.
2. **"Switch-off delay"** in acc. with DIN 46120.
   The triac turns on with the rising edge at S. The **falling edge** at S starts the timing period. The triac remains on until the set period has passed. Both operation modes are **retriggerable** during the timing period.

To protect the start input S against external interference and contact bounce, it has a **dead time** of between 20 and 40 ms (1/60 to 1/30 s)[1], depending on the phase of the 50 or 60-Hz line. To avoid positive and negative voltages the IC is equipped with an internal pull-up resistor and with clamping diodes.

Reset during a timing period is accomplished by interrupting the connection to R or by applying an H potential to R. The reset input R is provided with a dead time of 40 ms (1/30 s)[1].

Application note

If R is connected to one of the pins D through I via a multiposition switch, and if a reset of the timing period is to be avoided during the changeover, a suitable capacitor is required between R and 0. This applies only in cases where the interruption is greater than 40 ms (1/30 s)[1].

When the supply voltage is applied the circuit is automatically reset. Whereas no timing period is started when 0 potential is applied to S, a timing period is initiated upon applying S to V_S.

Triac stage

Pin TS (triac synchronization) is the input of a zero voltage switch and is used to synchronize the output T (open collector) with the load voltage or the load current. With $V_S < 3$ V, the output current is disconnected.

Pin TC has a double function. It serves for changing TS over to voltage synchronization and for adjusting the triac trigger pulse width (by connecting an external capacitor) in case of current synchronization.

Three operation modes are possible by varying the connection of the pins TC and/or TS:

Operation mode 1 (TC to V_S):

Output T is connected to the zero voltage switch. T operates when $V_S - 1.3\ V \leq V_{TS} \leq V_S + 1.3\ V$. Is utilized in case of voltage synchronization; **see application circuit 1.**

Operation mode 2 (TC via C_e to 0):

Output T is connected to the zero voltage switch via a monoflop. The output T releases a triac gate trigger pulse, determined by C_e, as soon as the voltage at TC decreases below $V_S - 1.3$ V or increases above $V_S + 1.3$ V. Is utilized in case of current synchronization; **see application circuit 2.**

Operation mode 3 (TC and TS to V_S):

Output T conducts after release of start pulse. Is utilized for any load in case of continuous triac triggering (e.g. low performance), or if any other load is to be operated instead of the triac **(see application circuits 3, 4, 5).**

[1]) The value in parentheses applies to 60-Hz version.

Operation with line voltage

A series resistor R_S and a charging capacitor C_{ch} serve for line voltage supply. If a diode is connected in series with R_S (anode to N), the rms current consumption is halved. The series resistor may also be an RC network **(see application circuit 6).**

Operation with dc voltage

This IC can also be operated with dc voltage or current **(see application circuits 4 and 5).**

Comments

in general

To obtain better noise immunity the pins D through I, which are not connected, are to be applied to 0.

on C_L

If short-term line failures are to be compensated, C_L has to be accordingly higher.

on application circuit 1 (voltage synchronization for resistive load)

An average I_{TS} of 0.025 mA was inserted into the formula approximating R_{SYN}. As I_{TS+} and I_{TS-} contain production deviations, utilizing the determined R_{SYN} requires certain tolerances to be taken into account for pulse length Z.

on application circuit 2 (current synchronization)

In this circuit, an even shorter pulse length than determined for Z is sufficient to trigger the triac. This is possible by the trigger pulse being automatically repeated until the hold current is reached. Overdimensioning of Z for safety reasons is, therefore, not necessary. The disadvantage of multiple trigger pulses, however, is a somewhat larger interference band during the triggering. The interference band and/or the interference amplitude generated also depend on the amount of the gate trigger voltage necessary to trigger the triac after each current zero passage. That voltage is determined by the size of R_{SYN} and should not exceed 20 V.

on application circuit 6

To limit the inrush current, R_{SS} has to be $\geq 0.2\ R_S$. Otherwise, the circuit might be damaged.

Maximum Ratings

$T_A = -25$ to $+85$ °C

Description	Symbol	min	max	Unit	Notes
Supply voltage[1]	V_S	−0.3	5.5	V	
AC at N[2]	$I_{N\,rms}$		35	mA	RMS value
DC from N[2]	$-I_N$		18	mA	Average value
Peak current at N[2]	I_{Np}	−200	200	mA	2 ms, 100 ms interval
Voltage at A, B, C, FT, FC, N, R, S, TC, CO	$V_{A...}$	−0.3	$V_S+0.3$	V	
Voltage at D, E, F, G, H, I, T	$V_{D...}$	−0.3	20	V	D...T nicht off-state
Voltage at TS	V_{TS}	$V_S-0.7$	$V_S+0.7$	V	
Current in D, E, F, G, H, I	$I_{D...}$		0.5	mA	D...I on-state
Current at S[3]	I_{IS}	−2	2	mA	
Current at FT	I_{FT}	−120	120	µA	
Continuous current in T	I_T		100	mA	T on-state
Peak current in T	I_{Tp}		150	mA	1 ms / 10 ms interval
Current at TS	I_{TS}	−4	4	mA	
Junction temperature	T_j		125	°C	
Storage temperature range	T_{stg}	−55	125	°C	
Thermal resistance system – air	$R_{th\,SA}$		70	K/W	

Operating Range

Supply voltage[4]	V_S	4.5	5.5	V	
Supply current (dc)[4]	$-I_N$	2.5	18	mA	[5]
Supply current (ac)[4]	$I_{N\,rms}$	5	35	mA	[5]
Ambient temperature	T_A	−25	85	°C	

Notes

1) with impressed voltage at V_S
2) with impressed current at N
3) with impressed current at S
4) The IC can be operated with impressed voltage or with impressed current. With impressed voltage at V_S the voltage that is applied can be between 0 and $V_{S\,max}$ V (see maximum ratings).
With impressed dc or ac at N, V_S is internally limited and thus ranges between 6 and 8.2 V (typ. 7.5 V). Operation, however, is also ensured if V_S falls to 4.5 V.
5) Only supply current for I_S, i.e. without triac gate current. The rms gate current additionally flows through N.

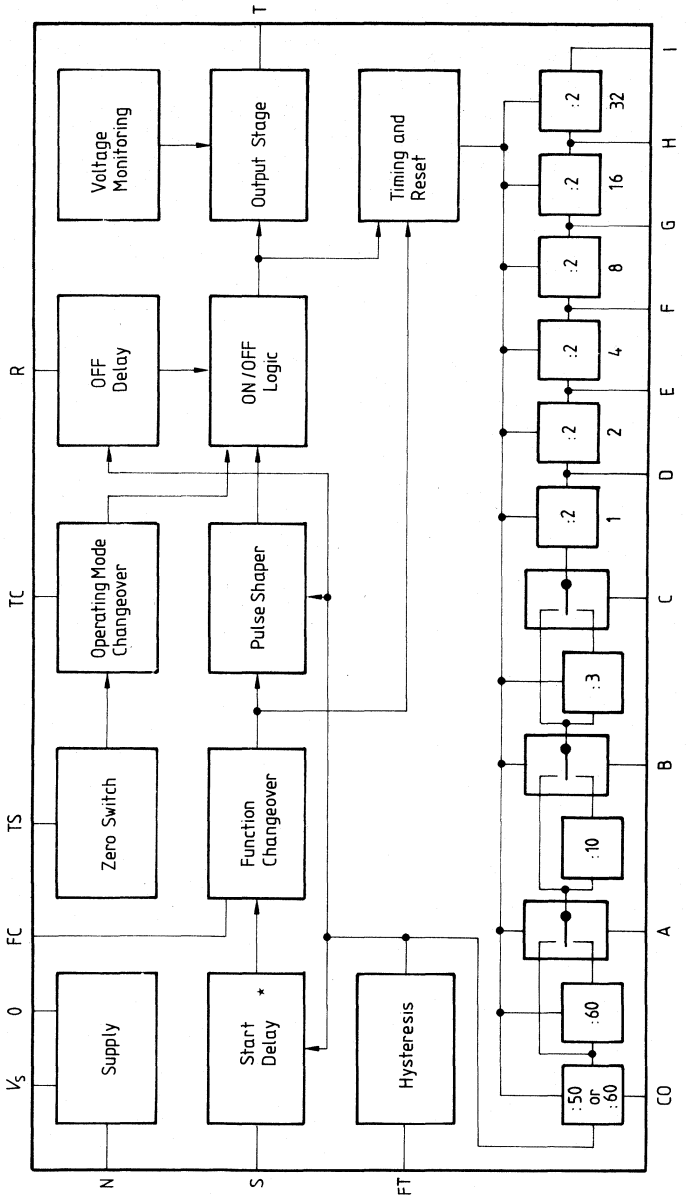
Characteristics

$V_S = 5.5$ V; $T_A = 25$ °C

Description	Symbol	Test conditions	Test circuit	min	typ	max	Unit
Supply current[1]	I_S	$V_{IS} = 0$ V	1		1.5	2.5	mA
V_S (impressed dc)[2]	V_S	$-I_N = 2.5$ mA	1		7.5	8.2	V
V_S (impressed ac)[2]	V_S	$I_{N\,rms} = 5$ mA	1		7.5	8.2	V
Voltage at S[3]	V_{IS}	$I_{IS} = 2$ mA				$V_S+0.9$	V
		$-I_{IS} = 2$ mA		-0.9			V
Voltage at FT	V_{FT}	$I_{FT} = 100$ µA				9.5	V
		$-I_{FT} = 100$ µA		-0.9			V
Switching threshold at A,B,C,S,FC,R,CO	$V_{A...}$		2	1.1	1.8	2.2	V
H switching threshold at FT	V_{FT}		2		1.8	2.4	V
L switching threshold at FT	V_{FT}		2	0.8	1.3		V
Switching hysteresis at FT	V_{HY}		2	0.4	0.5	0.9	V
Switching threshold at TC	V_{TC}		2		3.4	4.5	V
Switching threshold at TS	V_{TS+}	$V_{TS} > V_S$	2		$V_S+1.3$		V
	V_{TS-}	$V_{TS} < V_S$	2		$V_S-1.3$		V
L input current at A,B,C,FC,R,CO	$I_{A...}$	$V_{A...} = 0$ V	1		20	30	µA
L input current at S	$-I_{IS}$	$V_{IS} = 0$ V	1		60	90	µA
L input current at FT	$-I_{FT}$	$V_{FT} = 0$ V	1		40	60	µA
H input current at A,B,C,S,FC,R,CO	$I_{A...}$	$V_{A...} = V_S$	1			1	µA
H input current at FT	I_{FT}	$V_{FT} = V_S$	1			1	µA
H input current at TC	I_{TC}	$4.5 \le V_{TC} \le V_S$	1		20	40	µA
Pos. switch-over current at TS	I_{TS+}	$R_{SYN} = 0$	2	20	25	35	µA
Pos. switching hysteresis at TS	I_{Hy+}	$R_{SYN} = 0$	2	1	2	4	µA
Neg. switch-over current at TS	I_{TS-}	$R_{SYN} = 0$	2	20	25	35	µA
Neg. switching hysteresis at TS	I_{Hy-}	$R_{SYN} = 0$	2	1	2	4	µA
L voltage at D,E,F,G,H,I	$V_{D...}$	$I_{D...} = 0.5$ mA	1		0.2	0.4	V
H reverse current at D,E,F,G,H,I	$I_{D...}$		1			1	µA
L output voltage at T	V_Q	$I_T = 1$ mA	1		0.7	1.1	V
	V_Q	$I_T = 10$ mA	1		0.8	1.2	V
	V_Q	$I_T = 100$ mA	1		1	1.5	V

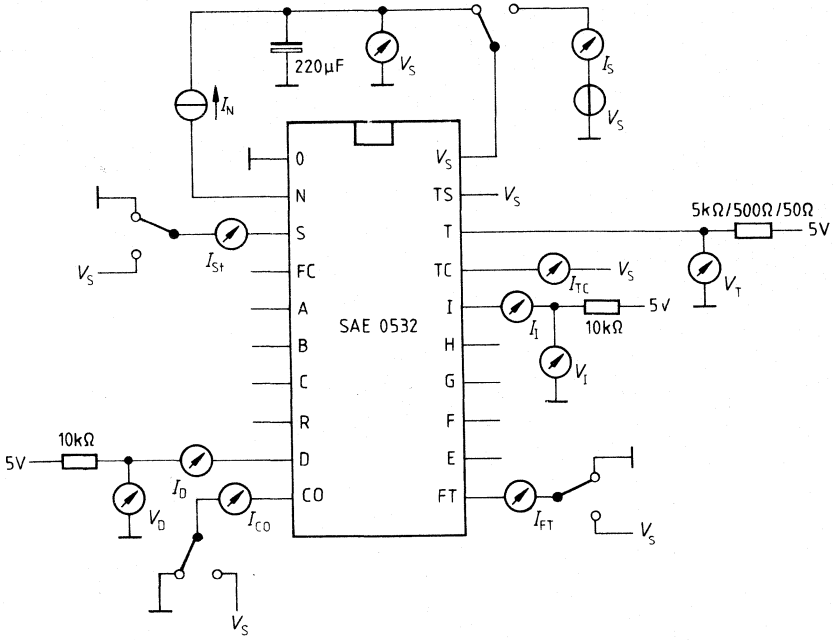
[1]) with impressed voltage at V_S
[2]) with impressed current at N
[3]) with impressed current at S

Block Diagram

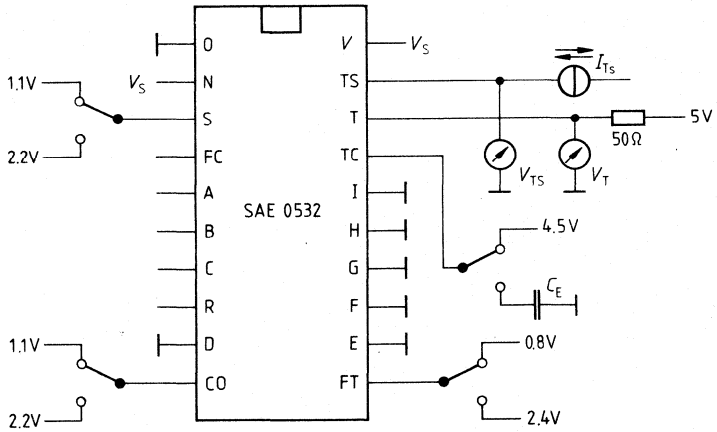


* for positive and negative edge

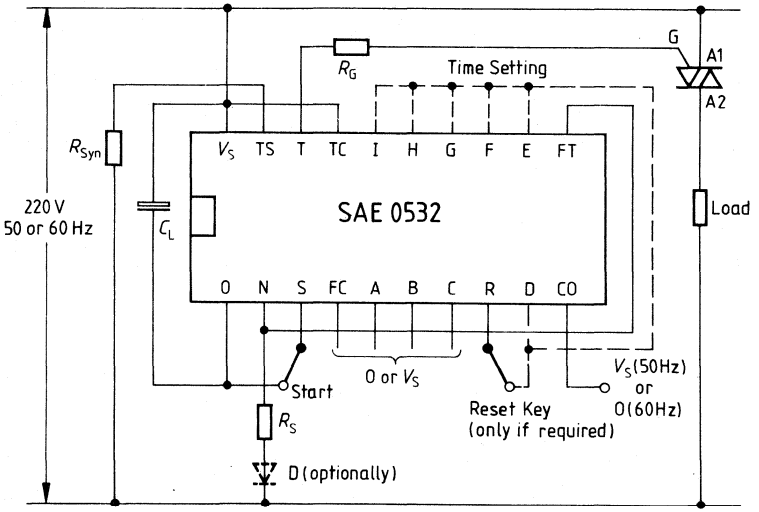
Measuring Circuit 1



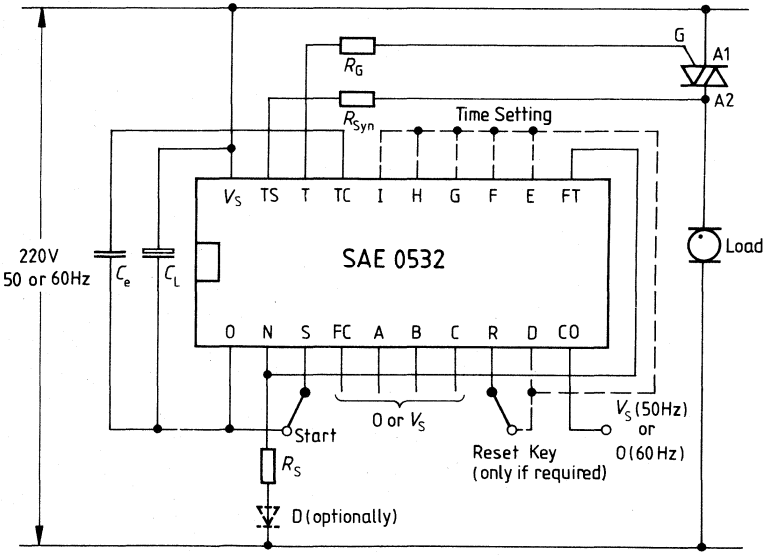
Measuring Circuit 2



Application Circuit 1
Operation with resistive load

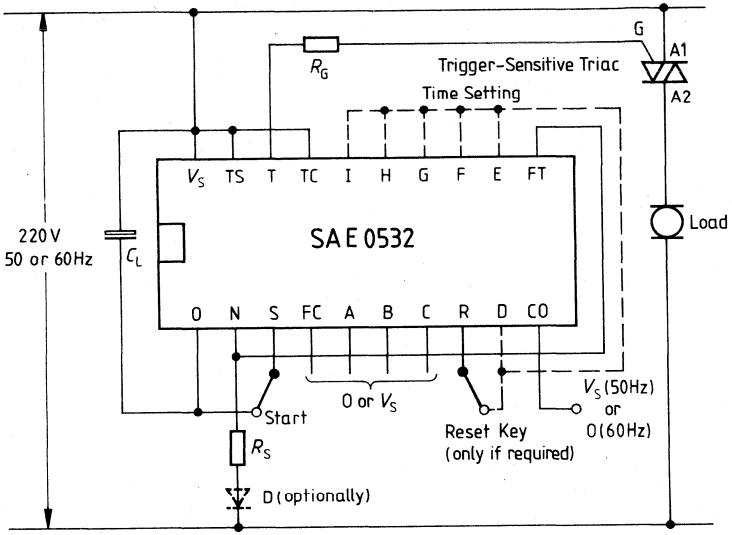


Application Circuit 2
Operation with resistive, capacitive and inductive load



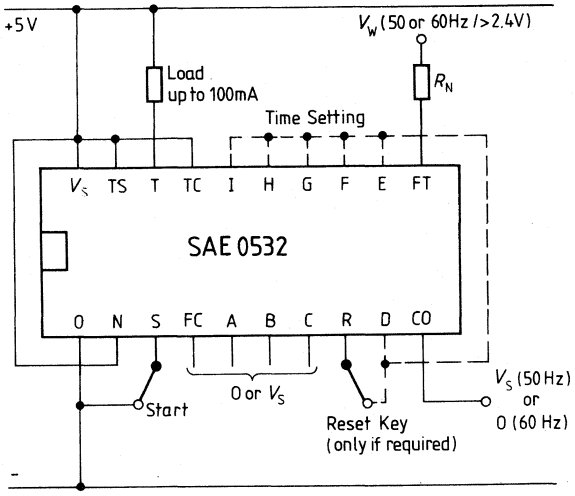
Application Circuit 3

Operation with any load and continuous triac triggering

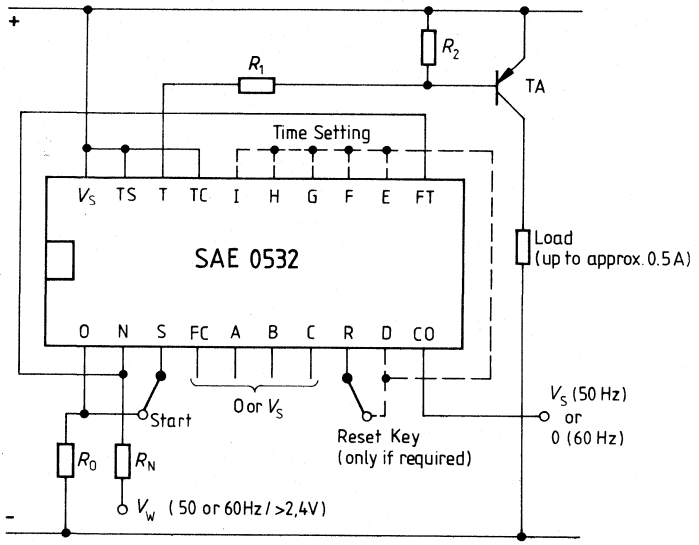


Application Circuit 4

Operation with 5 V dc voltage

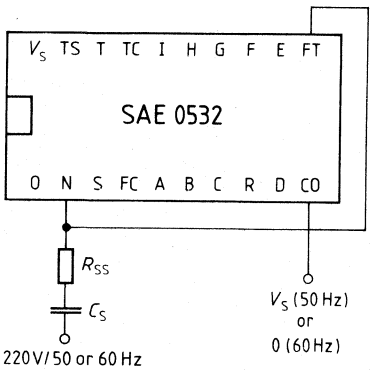


Application Circuit 5
Operation with dc voltage > 5.5 V

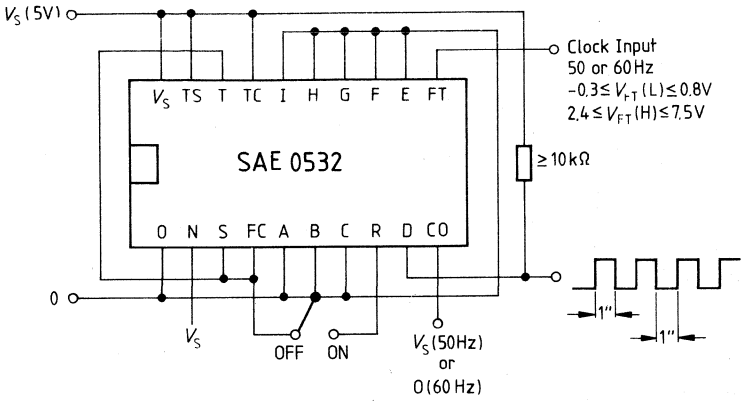


Application Circuit 6
Operation with capacitive series resistor

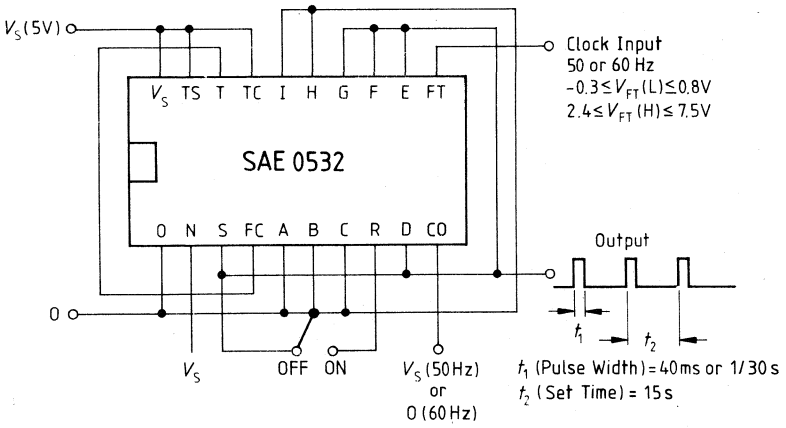
In the application circuits 1 to 3 a series connection of R and C may be utilized instead of R_S or R_S and D.



Application Circuit 7
Square wave generator

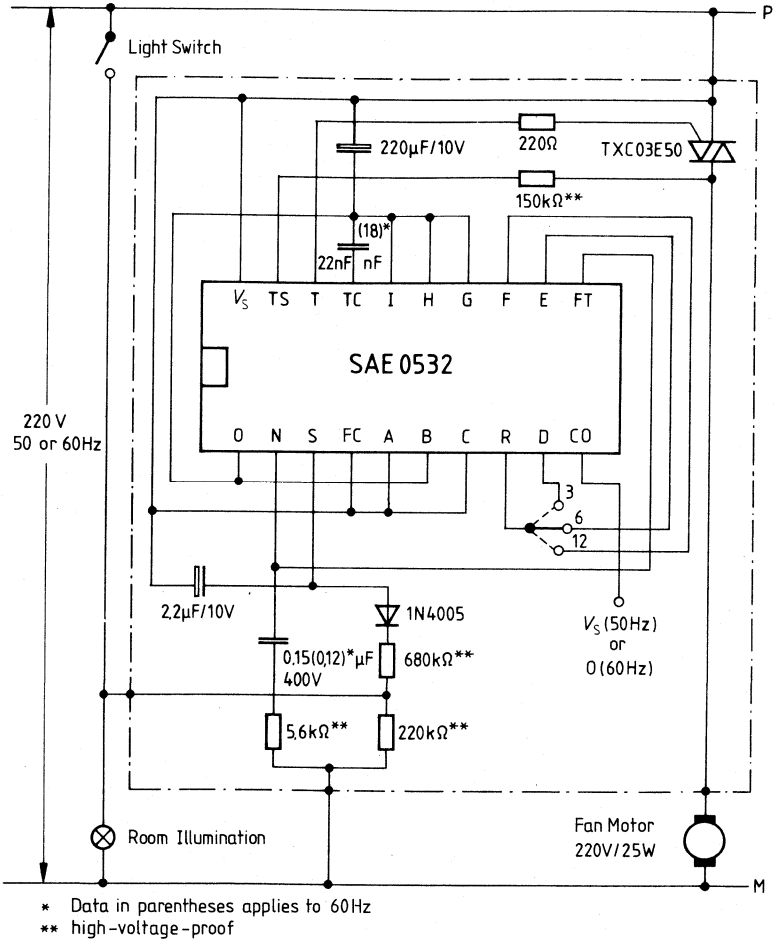


Application Circuit 8
Pulse Generator



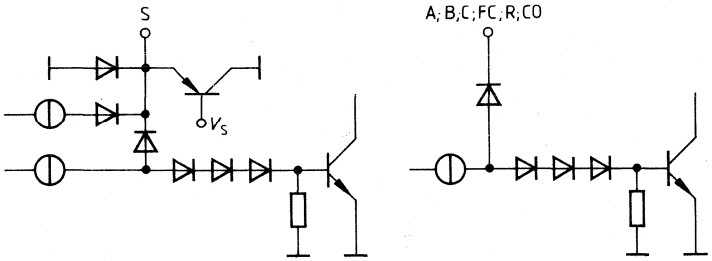
Application Circuit 9

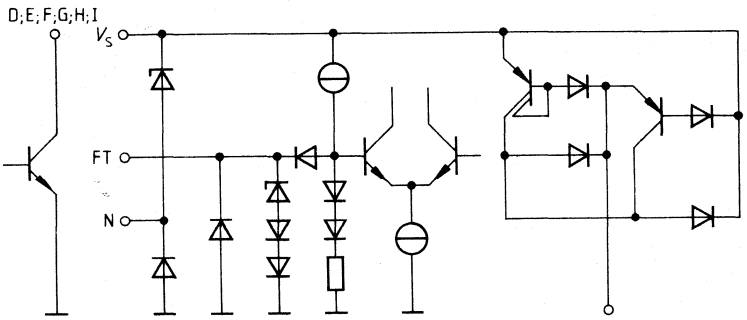
Time control for a ventilation, can be set to 3, 6 or 12 minutes follow-up time

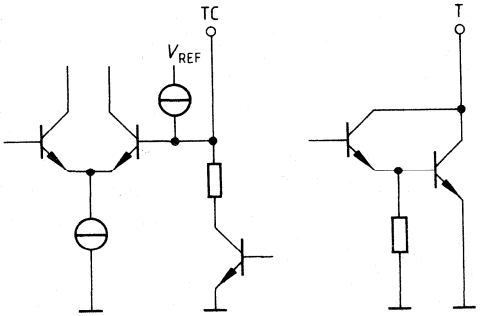


* Data in parentheses applies to 60Hz
** high-voltage-proof

Internal Connection of Inputs, Outputs, and Supply Pins

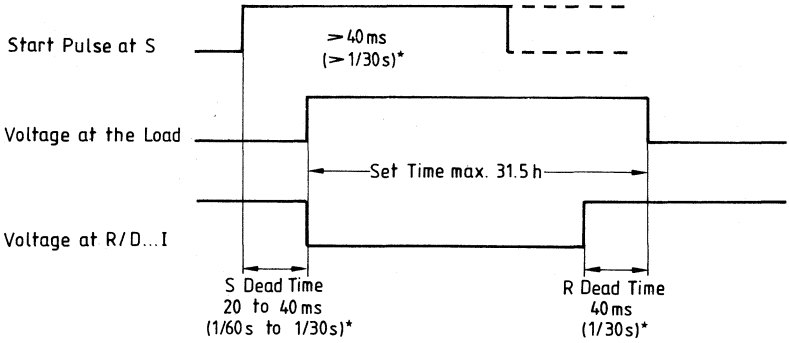






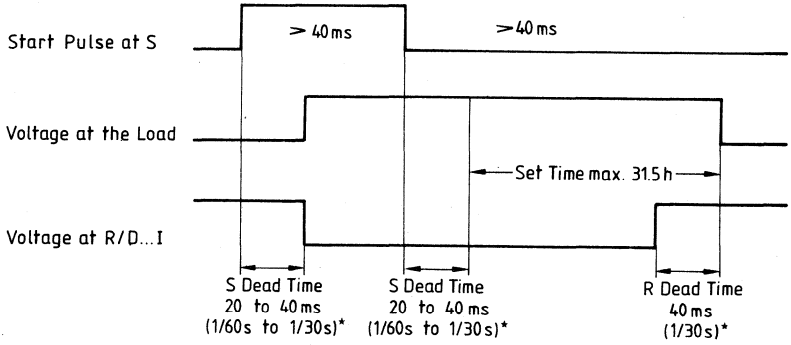
Pulse Diagrams of the Time Operation Mode

Momentary switching function



* Data in Parentheses Applies to 60-Hz Version

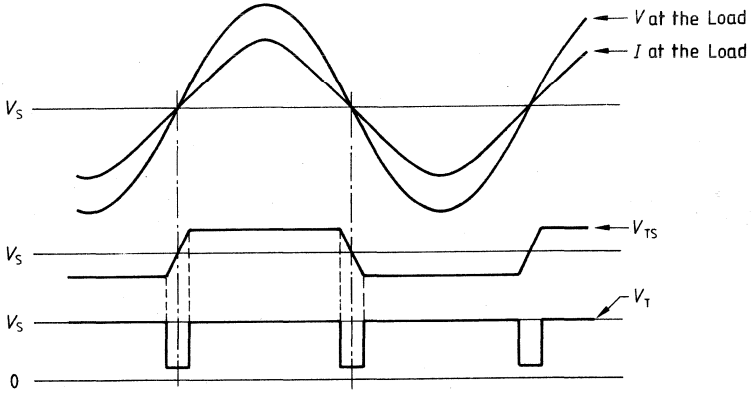
Switch-off delay



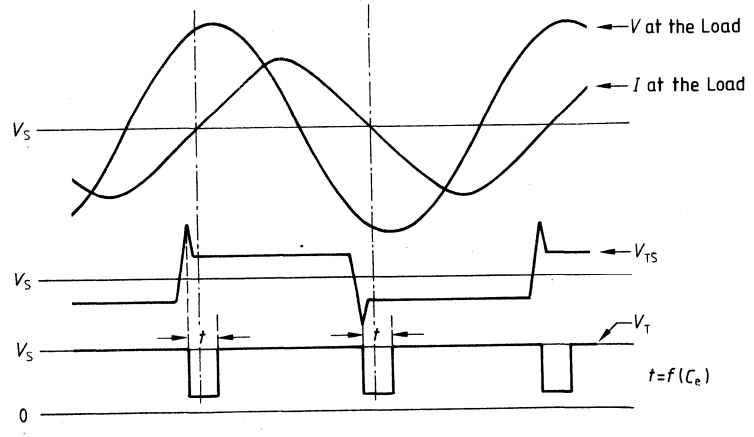
* Data in Parentheses Applies to 60-Hz Version

Pulse Diagrams for Triac Operation Modes 1 and 2

Operation mode 1: Voltage synchronization with resistive loads (TC at V_S)



Operation mode 2: Current synchronization with non-resistive loads
(Capacitance C_e at TC)



Audible Signal ICs

Audible Signal ICs

Selector Guide

Type	Package	Function	Technical Data
Acoustic Signal Generators			
SAB 0600	P-DIP-8	**Three-tone chime IC,** melodious and voluminous three-tone sound, few external components, integrated output stage for 80 Ω loudspeakers	V_S = 7 to 11 V Standby current < 1 µA
SAB 0601		**Single-tone chime**	
SAB 0602		**Double-tone chime**	
SAE 0700	P-DIP-8	**Signal-tone generator,** produces two subsequent, periodical tone frequencies in the ratio 1.4 : 1.	V_S = 9 to 25 V or ac voltage from 10 V_{rms}

Three-Tone Chime
Single-Tone Chime
Dual-Tone Chime

SAB 0600
SAB 0601
SAB 0602

Bipolar IC

Type	Ordering Code	Package
SAB 0600	Q67000-H1948	P-DIP-8
SAB 0601	Q67000-H2312	
SAB 0602	Q67000-H2313	

Three-Tone Chime SAB 0600

This IC generates the tone sequence of a 3-tone chime. The sound pattern is created by three harmonically tuned frequencies which are switched in succession to a summing point and decay individually in amplitude.

The tone color is adjusted by an external *RC* network (R_1, C_1, C_2). An 8 Ω loudspeaker can be connected directly via a 100 µF capacitor.

An appropriate design of the loudspeaker housing (shaped as tube or horn) enhances the volume and tone quality and contributes to a pleasant, melodious sound.

Features

- Melodious sound
- Few components required
- Integrated output stage for 8 Ω loudspeaker
- Standby current < 1 µA

Single-Tone Chime SAB 0601 and Dual-Tone Chime SAB 0602

The two variants SAB 0601 and SAB 0602 were derived from type SAB 0600 by suppressing the last two tones or last tone, respectively, of the three-tone sequence. The SAB 0600 data applies correspondingly.

Maximum Ratings

Description	Symbol	min	max	Unit
Supply voltage Input voltage at E	V_S V_E	−0.5 −0.5	11 V_S	V V
Neg. input current at E	$-I_E$		2	mA
Load resistance at Q	R_L	7		Ω
Current consumption at start of tone sequence end of tone sequence } refer to measurement circuit	I_{SM} I_{SO}		90 35	mA mA
Oscillator frequency at C (due to power dissipation)	f_{OSC}	6		kHz
Junction temperature Storage temperature	T_j T_{stg}	 −55	150 125	°C °C
Thermal resistance (system – air)	$R_{th\ SA}$		120	K/W

Operating Range

Supply voltage	V_S	7	11	V
Ambient temperature	T_A	0	70	°C
Oscillator frequency at C	f_{OSC}	6	100	kHz

Characteristics

$V_S = 7$ V to 10 V; $T_A = +25$ °C

Description	Symbol	min	typ	max	Unit
Standby input current Supply current with open output	I_0 I_{SO}		<1 20	10 35	µA mA
Max. output power at 8Ω (tone 3) Max. output voltage at Q (tone 3	P_Q $V_{Q\ pp}$		0.16 2.8	 4.0	W V
Deviation of the max. individual amplitudes referred to tone 3	ΔV_{QM}		±5		%
Frequency variation of basic oscillator with R_1, C_1 = const.	Δf_o		±5		%
Triggering voltage at E	V_E	1.5		V_S	V
Input current at E ($V_E = 6$ V)	I_E	500	700		µA
Noise voltage immunity at E	$V_{EN\ pp}$		0.3		V
Triggering delay at $f_o = 13.2$ kHz (t_D varies in inverse proportion to f_o)	t_D	2		5	ms
Min. value of external load resistor Max. value of external load resistor	R_1 R_1		10 100		kΩ kΩ

Figure 1
Measurement Circuit

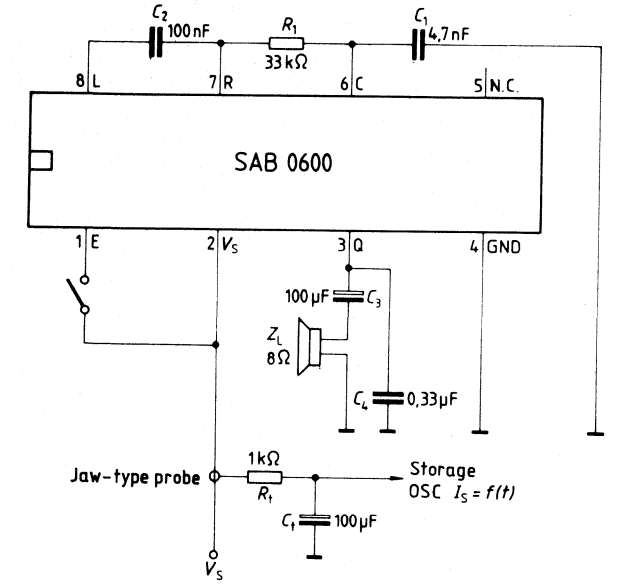


Figure 2
Integral Current Consumption in the Measurement Circuit

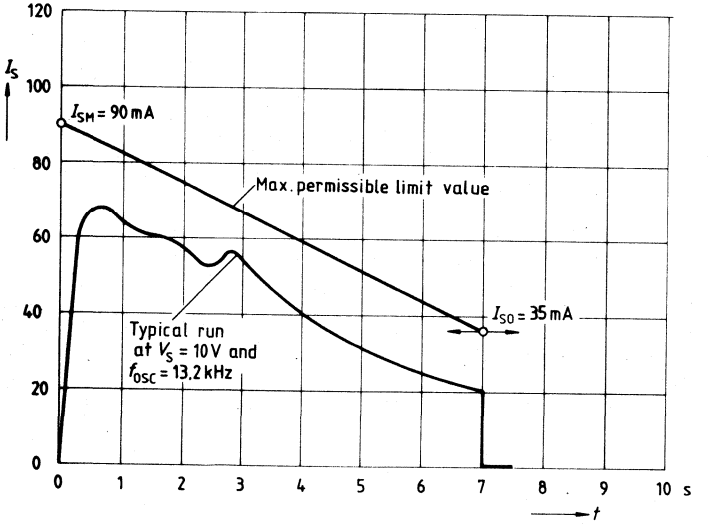


Figure 3
Block Diagram

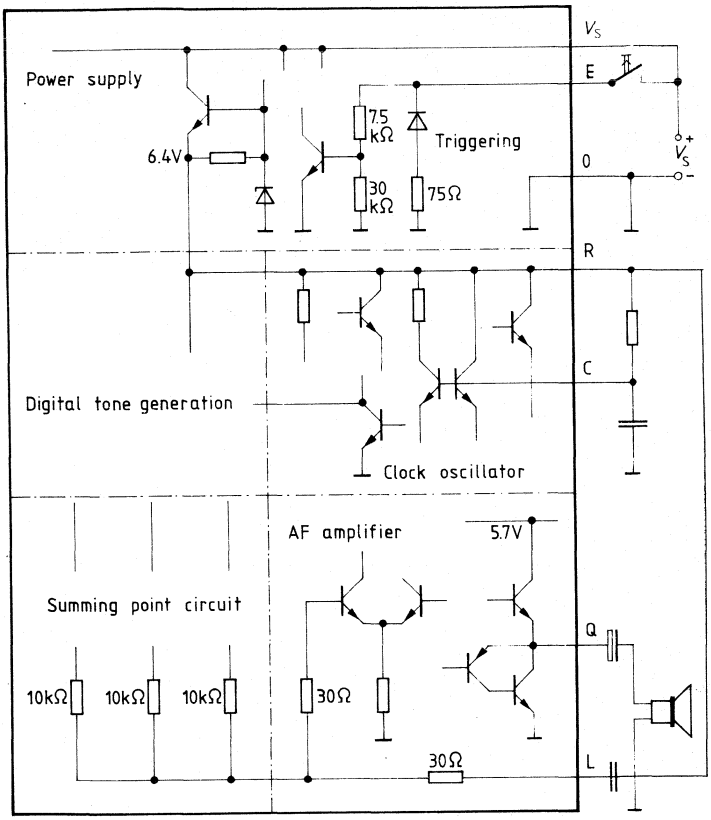
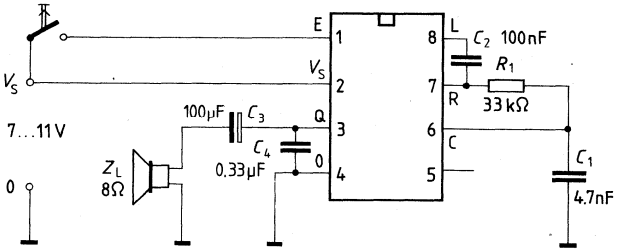


Figure 4
Typical Application Circuit



Functional Description

The three frequencies – 660 Hz, 550 Hz, and 440 Hz – are obtained by dividing the output of a 13.2 kHz oscillator. One of these three frequencies is divided again to obtain the time base for the tone-decay process. From this time base, 4-bit D/A converters (one for each tone) generate the decay voltage with which the three tones are successively activated and, overlapping each other, are attenuated. The basic frequency is determined by an external *RC* network (pins R and C).

The output stage can drive an 8 Ω loudspeaker with approximately 0.16 W via 100 µF. The output voltage is of square shape. To obtain a melodious output tone as required, the higher harmonics may be reduced by shunting pin L through a suitable capacitor to ground. The output volume can be regulated here by means of a potentiometer.

The circuit only draws current in the active state, and automatically switches off after the tones have decayed. The circuit is activated by a short pulse, between 1.5 V and V_S in amplitude, applied to the triggering connection E (pin 1). If the trigger voltage is still, or again, present when the tones have decayed, the three tones are repeated.

The circuit is not activated when a trigger pulse on E is shorter than 2 ms (interference suppression).

To prevent triggering of the circuit by cross-talk voltages, especially in case of long input lines, the noise voltage peaks should be limited to 0.3 V at the IC input. For this purpose the control line (possibly in front of a series resistor) can be shunted to ground through a suitable capacitor.

Application for ac and dc Triggering (Figure 5)

The input can alternatively be triggered with direct or alternating current. An internal diode circuit hereby short-circuits the input for negative halfwaves.

The peak voltage of the positive halfwave is added to the battery voltage. A series resistor must be connected into the trigger line to limit the voltage at input E (pin 1) to a maximum value equal to V_S.

The minimum input current at pin E of the SAB 0600 (pin 1) is 500 µA at 6 V. If the voltage drop occurring at 500 µA at the series resistor R_3 **(figure 5)** amounts to at least the ac peak voltage between A and B ($\hat{V}_{AB}$ ~), the IC will be safe.

The formula $$R_{3\,min} = \frac{\hat{V}_{AB\,max.}}{500\ \mu A}$$

determines the lower limit for R_3.

The upper limit for R_3 is determined by the lowest trigger voltage between A and 0 (pin 4). In the application shown in **figure 5,** this will be the battery voltage if the device is also to be operated independently of the bell system (triggering by short circuit of A and B).

For reliable triggering, the SAB 0600 requires a current of at least 50 µA with approx. 1.5 V at pin E. Assuming this current, the voltage drop at R_3 must, therefore, not exceed $V_S - 1.5$ V.

The formula $$R_{3\,max} = \frac{V_{S\,min.} - 1.5\ V}{50\ \mu A}$$

results in the upper limit for R_3.

Calculation Example for the Circuit in Figure 5

max. $V_{AB\,rms} = 25$ V max. $\hat{V}_{AB} = 25\ V \times \sqrt{2} = 35.4$ V

$$R_{3\,min} = \frac{35.4\ V}{500\ \mu A} = 70.8\ k\Omega$$

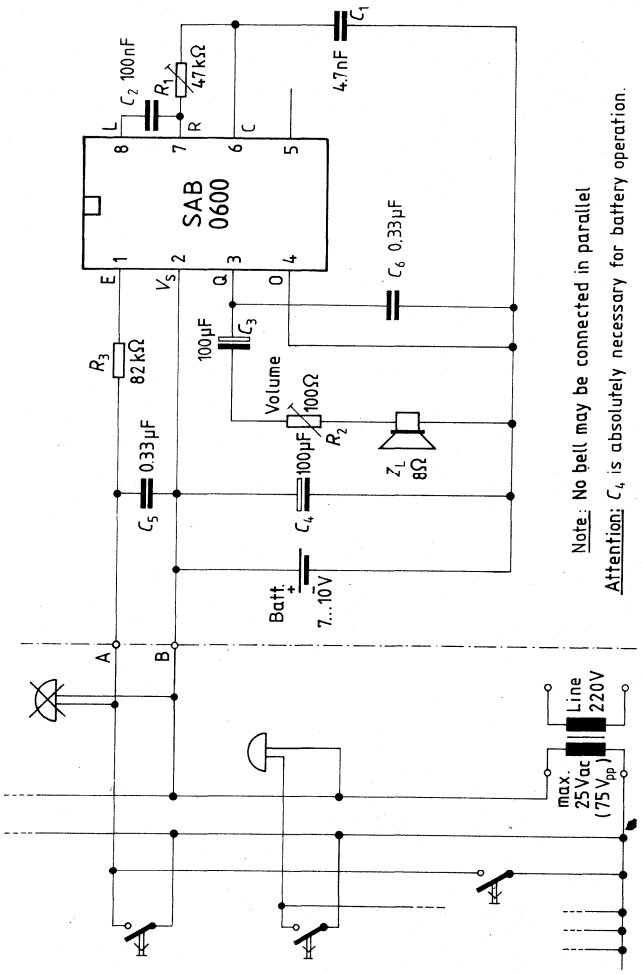
min. $V_S = 6$ V

(The operating range of the SAB 0600 may extend to 6 V for individual components).

$$R_{3\,max} = \frac{6\ V - 1.5}{50\ \mu A} = 90\ k\Omega$$

In this example, a value of 82 kΩ ± 10% would be suitable for R_3.

Figure 5
Circuit for SAB 0600 Application in Home Chime Installations Utilizing AC and DC Triggering; Adjustable Sound and Volume



PCB layout information: Because of the high peak currents at V_S, Q, and 0 (ground) and to avoid RF oscillations, the lines should be designed in a flatspread way or as star pattern. Star points are the terminals of capacitor C_4.

Further Details Regarding the Circuit in Figure 5

Since an ohmic contact between A and B causes triggering of the chime, no bell may be connected in parallel to the chime. However, paralleling several chimes does not cause any problems.

In older batteries, the higher internal resistance of the battery may cause voltage drops becoming apparent as distortions. C_4 serves as a buffer element expanding the service life of the battery.

The trigger line connected to pin A acts – in open state – as antenna for noise pulses which could trigger the chime unintentionally. Capacitor C_5 will largely suppress such interference.

If there is the risk of incorrect polarity connection when changing the battery, the battery line should be protected by a diode.

For the selection of components, the following recommendations are given:

Capacitors:

C_1: 4.7 nF/≥ 10 V, ± 5%; e.g. MKT
C_2: 100 nF/≥ 10 V, ± 20%; e.g. MKT
C_3: 100 µF/≥6.3 V, ± 100/—10%; e.g. aluminum electrolytic
C_4: 100 µF/≥ 10 V, + 100/—10%; e.g. aluminum electrolytic
C_5, C_6: 330 nF/≥ 50 V, + 100/—20%; e.g. ceramic

Resistors:

R_3: 82 kΩ/0.1 W, ± 10%, carbon film resistor
R_1: When a fixed resistor is used, 0.1 W ± 5% metal film resistor.

Bipolar IC

Type	Ordering Code	Package
SAE 0700	Q67000-A2445	P-DIP-8

The audible signal device SAE 0700 generates two tone frequencies in a ratio of approx. 1.4 : 1 that follow one another in a periodic sequence. The tone frequency can be varied throughout a range between 100 Hz and 15 kHz by an external resistor. The switching frequency of 0.5 to 50 Hz is set by an external capacitor. The SAE 0700 can be used to drive either a loudspeaker or a piezo-ceramic transducer. The SAE 0700 can be supplied with voltage in two ways:

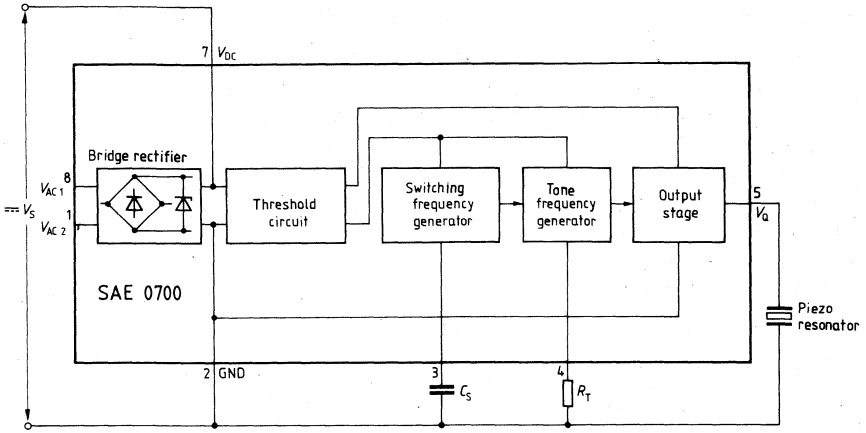
1. rms ac voltage from 10 V
2. dc voltage from 9 to 25 V

The SAE 0700 issues the tone sequence for as long as the supply voltage is applied. After application of the supply voltage, the tone sequence commences with the higher of the two tones.

Features

- Direct ac-voltage feeding possible through integrated bridge rectifier
- Integrated overvoltage protection through Z diode, approx. 28 V
- Bridge rectifier provides for protection against reverse polarity in dc operation
- Few external components (one resistor and one capacitor minimum)

Figure 1
Block Diagram (with external components for dc supply)



Pin Description

Pin	Symbol	Function
1	V_{AC2}	AC-voltage input
2	GND	Ground
3	C_S	Connection for capacitor C_S
4	R_T	Connection for resistor R_T
5	Q	Output
6	N.C.	Not connected
7	V_{DC}	DC-voltage input
8	V_{AC1}	AC-voltage input

Functional Description

The audible signal device SAE 0700 (see block diagram, **fig. 1**) includes the following functional blocks:

- bridge (for voltage supply) and overvoltage protection
- threshold circuit
- switching-frequency generator
- tone-frequency generator
- output stage

Bridge rectifier: The bridge rectifier enables direct feeding with ac voltage or dc voltage (independent of polarity). DC-voltage supply without integrated bridge is also possible via pins V_{DC} and GND.

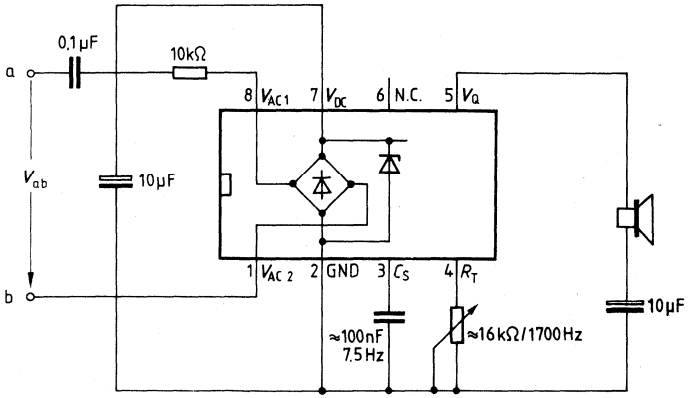
If the voltage is supplied via the bridge, the input voltage V_{81} should be dimensioned such that at least 9 V appear at the pin V_{DC} (also with output loading). It should also be noted that in the case of voltage supply via the bridge, the maximum output current has to be limited to 50 mA.

Response of the SAE 0700 as a result of spikes on the AC line is prevented by a built-in initial resistance R_{INI}. In a voltageless condition R_{INI} provides for discharging the storage capacitor of V_{DC} to ground.

The Z diode following the bridge serves as overvoltage protection. The bridge circuitry shown in **figure 2** efficiently protects the SAE 0700 against damage as a result of the following voltage values:

- overvoltages in acc. with VDE 0433 (2 kV – 10/700 µs)
- ac voltages up to 220 V/50 Hz for a duration of 30 s

Figure 2



Threshold circuit: With a threshold voltage of typically 8.6 V this ensures that the SAE 0700 is not activated by noise pulses.

Switching-frequency generator: This switches periodically between the two frequencies produced by the tone-frequency generator. Wiring with a capacitor C_S produces a switching frequency f_S according to the following formula:

$$f_S\ [\text{Hz}] = \frac{750}{C\ [\text{nF}]} \pm 25\% \quad \text{(valid from 0.5 to 50 Hz)}$$

Tone-frequency generator: This generates a squarewave voltage with the two tone frequencies f_{T1} and f_{T2}. The basic frequency f_{T1} and the second tone frequency f_{T2} are calculated according to the following formulae:

$$f_{T1}\ [\text{Hz}] = \frac{2.72 \times 10^4}{R\ [\text{k}\Omega]} \pm 25\% \quad \text{(valid from 0.1 to 15 kHz)}$$

$$f_{T2}\ [\text{Hz}] = f_{T1} \times (0.725 \pm 5\%)$$

The tone-frequency generator is temperature-compensated for better stability.

Output stage: This boosts the generated tone voltage for direct driving of a piezo-ceramic transducer or a loudspeaker, possibly across a dropping resistor.

Maximum Ratings

Description	Symbol	min	max	Unit
Voltage at pin 7	V_{DC}	−0.5	26	V
Voltage at pin 3	$V_{3\,2}$	−0.5	5.5	V
Voltage at pin 4	$V_{4\,2}$	−0.5	7	V
Output voltage at pin 5	V_Q	−0.5	V_{DC} +0.5	V
AC voltage at pin 8 and 1 (peak value)	V_{AC}		28	V
Input current of bridge	$I_{8\,1}$	−50	50	mA
AC input current of bridge	$I_{8\,1\,rms}$		25	mA
Output current (50 µs, duty cycle 1:10)	I_Q	−100	100	mA
Output current	$I_{Q\,rms}$		50	mA
Total power dissipation ($T_A = 25\,°C$)	P_{tot}		0.8	W
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−40	125	°C
Thermal resistance system – air	$R_{th\,SA}$		120	K/W

Operating Range

Supply voltage	V_{DC}	9	25	V
Tone frequency	f_{T1}	0.1	15	kHz
Ambient temperature	T_A	−25	85	°C

Characteristics

$T_A = -25\,°C$ to $+85\,°C$

Description	Symbol	Test conditions	min	typ	max	Unit
Current consumption	I_{DC}	$V_{DC} = 9$ V to 25 V without load		1.5	1.8	mA
Switching threshold	$V_{DC\,ON/OFF}$		8	8.6	9	V
Initial resistance	R_{INI}	see characteristic, figure 3	3.5	4.7	6	kΩ
Output-voltage swing	V_Q	$I_Q = \pm 10$ mA	V_{DC}−3.7	V_{DC}−3		V
Tone frequency	$f_{T\,1}$	$V_{DC} = 15$ V, $V_{3\,2} = 0$ V $R_T = 16$ kΩ	1.275	1.700	2.125	kHz
Switching frequency	f_S	$V_{DC} = 15$ V, $C_S = 100$ nF	5.6	7.5	9.4	Hz
Tone frequency ratio	$f_{T\,1}/f_{T\,2}$		1.31	1.38	1.45	
Temperature coefficient of tone frequencies	TC_f			8×10^{-4}		K^{-1}

Characteristic Curves

Figure 3
Current consumption versus supply voltage V_{DC} without output load

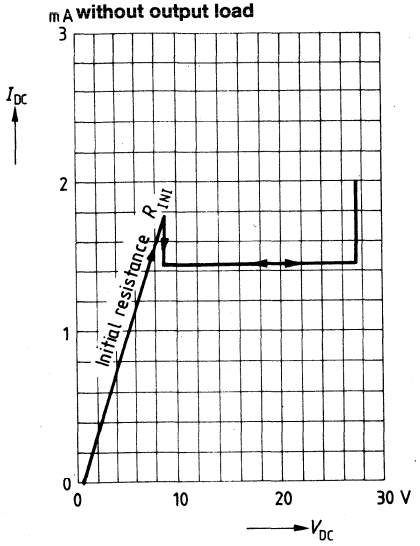


Figure 4
Tone frequencies f_{T1} and f_{T2} versus resistance R_T

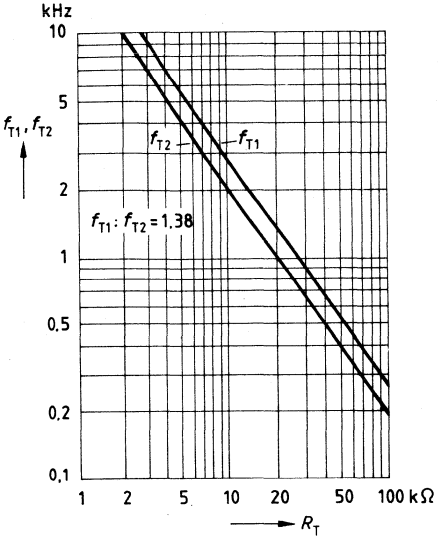
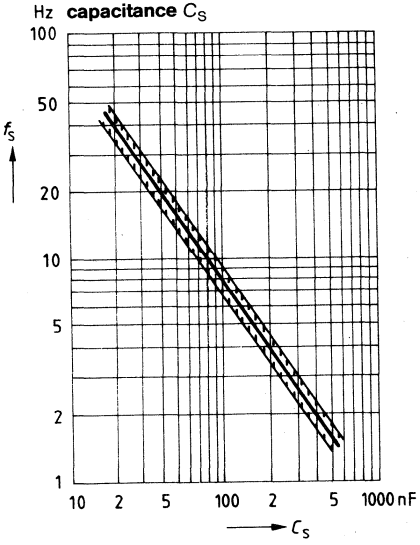


Figure 5
Switching frequency f_S versus capacitance C_S



ICs for RF Communications Applications

Selector Guide

Type	Package	Function
TBB 042 G	P-DSO-14 (SMD)	Mixer
TBB 200	P-DIP-14	PLL frequency synthesizer
TBB 200 G	P-DSO-14 (SMD)	PLL frequency synthesizer
TBB 202	P-DIP-8	Dual modulus divider
TBB 202 G	similar to P-DSO-8 (SMD)	Dual modulus divider
TBB 302	P-DIP-16	Schottky diode matrix, 8 x 6
TBB 303	P-DIP-14	Schottky diode matrix, 7 x 6
TBB 304	P-DIP-14	Schottky diode matrix, 4 x 8
S 89	P-DIP-14	Adjustable divider for 500 MHz
S 1531 G	similar to P-DSO-8 (SMD)	AF amplifier, 1 V

Bipolar IC

Type	Ordering Code	Package
S TBB 042 G	Q67000-A8059	P-DSO-14 (SMD)

The TBB 042 G is a symmetrical mixer applicable for frequencies up to 200 MHz. It can be driven either by an external source or by a built-in oscillator.

Common applications are in receivers, converters, and demodulators for AM and FM signals.

Features

- Wide range of supply voltage
- Few external components
- High conversion transconductance
- High pulse strength
- Low noise

Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	15	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance system – air	$R_{th\ SA}$	125	K/W

Operating Range

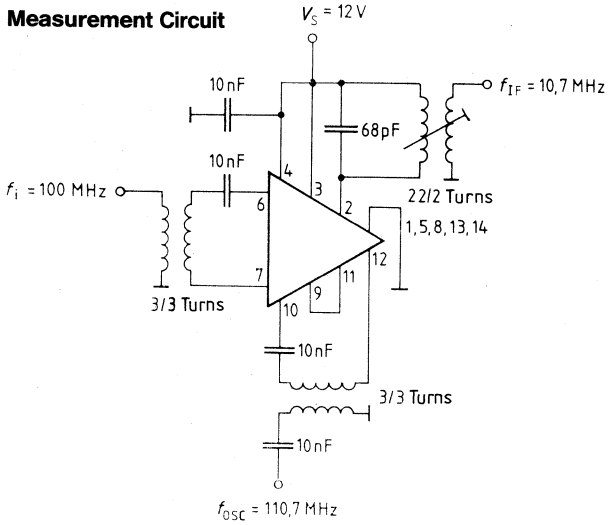
Supply voltage	V_S	4 to 15	V
Ambient temperature	T_A	−15 to 70	°C

Characteristics

$V_S = 12$ V, $T_A = +25$ °C

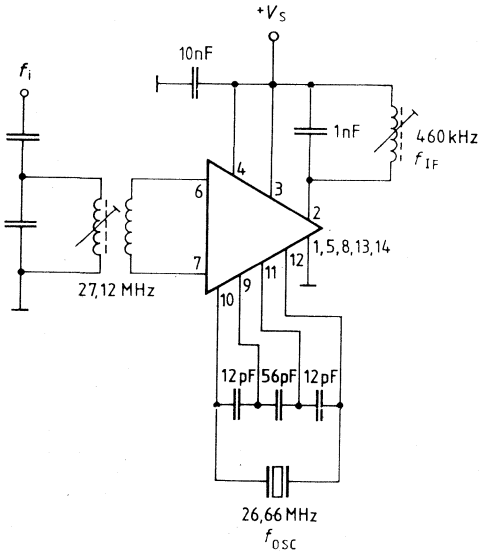
Description	Symbol	min	typ	max	Unit
Current consumption	$I_S = I_2 + I_3 + I_5$	1.4	2.15	2.9	mA
Output current	$I_2 = I_3$	0.36	0.52	0.68	mA
Output current difference	$I_3 - I_2$	−60		60	mA
Supply voltage	I_5	0.7	1.1	1.6	mA
Power gain ($f_i = 100$ MHz, $f_{OSC} = 110.7$ MHz)	G_p	14	16.5		dB
Breakdown voltage ($I_{2,3} = 10$ mA; $V_{7,8} = 0$ V)	V_2, V_3	25			V
Output capacitance	$C_{2\text{-}M}$, $C_{3\text{-}M}$		6		pF
Conversion transconductance ($f = 455$ kHz)	$S = \frac{I_2}{V_7\text{-}V_8} = \frac{I_3}{V_7\text{-}V_8}$		5		mS
Noise figure	F		7		dB

Measurement Circuit



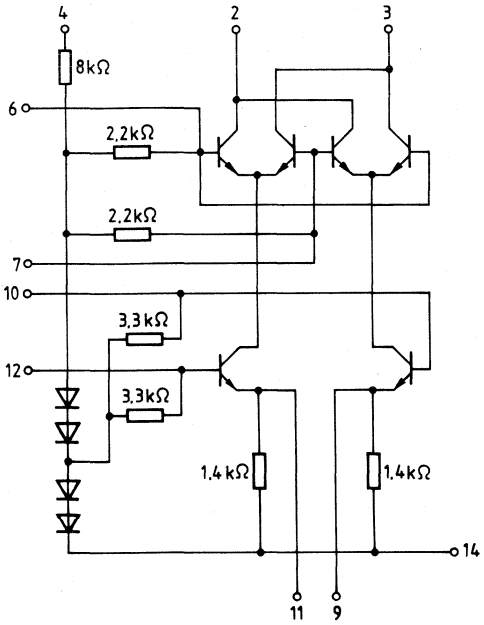
Application Circuit

Mixer for Remote Control Receiver
self-oscillating



For harmonic crystals, an inductor between pins 9 and 11 which will prevent oscillations on the fundamental is recommended.

Circuit Diagram

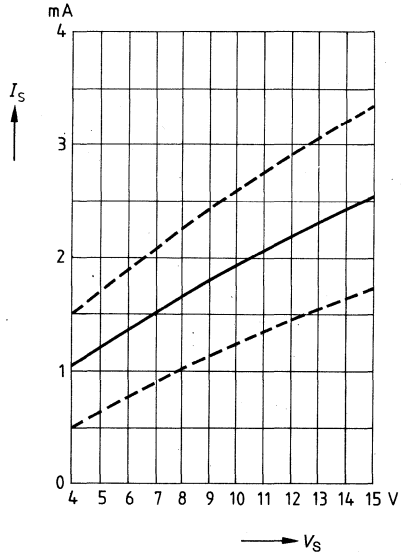


Pins 1, 5, 8 and 13 should be connected to pin 14 (GND) to obtain optimum RF features.

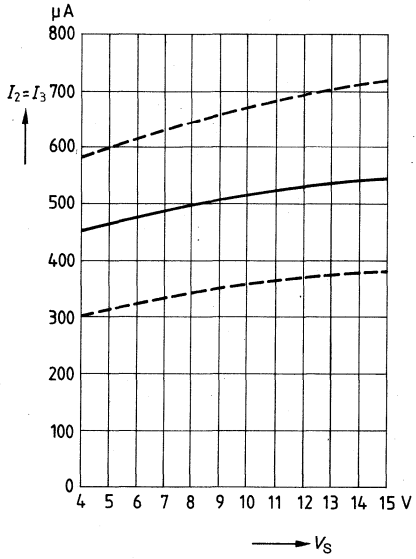
It is recommendable to establish a galvanic connection between pins 6 and 7 and pins 10 and 12 through coupling windings.

A resistor of at least 220 Ω may be connected between pins 9 and 14 (GND) and pins 11 and 14 to increase the currents and thus the conversion transconductance. Pins 9 and 11 may be connected via any impedance. In case of a direct connection between pins 9 and 11 the resistance from this connection to pin 14 may be at least 100 Ω. Depending on the layout, a capacitor (10 to 50 pF) may be required between pins 6 and 7 to prevent oscillations in the VHF band.

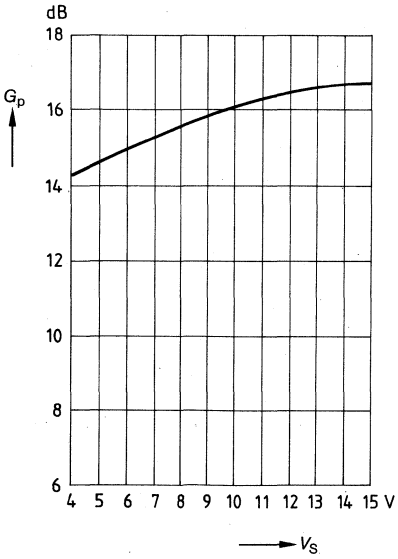
Total current consumption versus supply voltage



Output current versus supply voltage



Power gain versus supply voltage



CMOS IC

Type	Ordering Code	Package
TBB 200	Q67100-H8215	P-DIP-14
S TBB 200 G	Q67100-H8216	P-DSO-14 (SMD)

TBB 200 is a CMOS IC which has been especially developed for use in radio equipment and telephones. It is suited to simple frequency synthesis as well as to dual modulus synthesis.

Features

- Bit serial control with 2 lines (I^2C bus)
- Modulus switching
- Voltage doubler for high phase-detector output voltage
- Linearization of phase detector output by current sources
- High input sensitivity (10 mV), high input frequencies (70 MHz) in single modulus operation
- Low supply voltage, wide temperature range
- Low operating current consumption
- Standby circuit
- Extremely fast phase-detector with very short anti-backlash pulse
- Large dividing ratios
  - A divider 1 to 127
  - N divider 3 to 4095
  - R divider 3 to 65535
- Switchable phase-detector polarity
- Switchable phase-detector retuning rate of rise
- PORT output addressable via I^2C bus
  - for prescaler standby
  - for prescaler programming (128 or 64)

I^2C bus is a patented bus system of Philips.

Circuit Description

TBB 200 is a complex PLL component in CMOS technology for processor controlled frequency synthesis. Pin S/D selects **S**ingle or **D**ual modulus operation. Functions and dividing ratios are selected via an I²C bus interface at pins SDA and SCL. An output port PRT permits control (e.g. standby) of additional circuitry. The reference frequency is applied at input RI; its maximum value is 30 MHz. The VCO frequency is applied at input FI. Its maximum value in single modulus operation is 70 MHz and in dual modulus operation 30 MHz. The PLL can be operated optionally with or without internal voltage doubler, depending on the required frequency variation (Varicap). For operation with voltage doubler, a capacitance of typ. 1 µF (MKH) must be connected at pin C. C must be grounded when the voltage doubler is not in use.

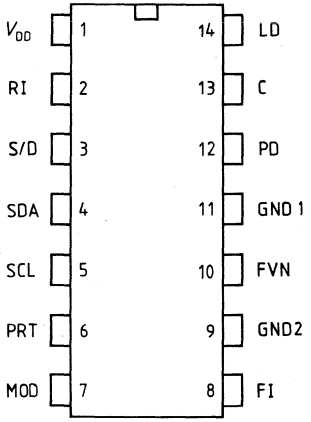
Output PD supplies the phase detector signal with especially short anti-backlash pulses to neutralize even the smallest phase deviations. Output LD supplies a static lock detector signal, and output FV the divided VCO frequency. LD and FVN are open drain outputs.

By means of a short message (3 bytes) via I²C bus the component can be switched to standby mode. Depending on the type of standby the quiescent current consumption is below 1 µA. The PLL can be re-activated from this state by one command. Recharge of the R, N, A dividers and of additional information is not necessary, since they are internally stored.

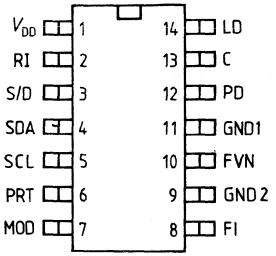
Mode	S/D	MOD
Single modulus	L	(not activated)
Dual modulus	H	L/H

Pin Configurations
(top view)

TBB 200



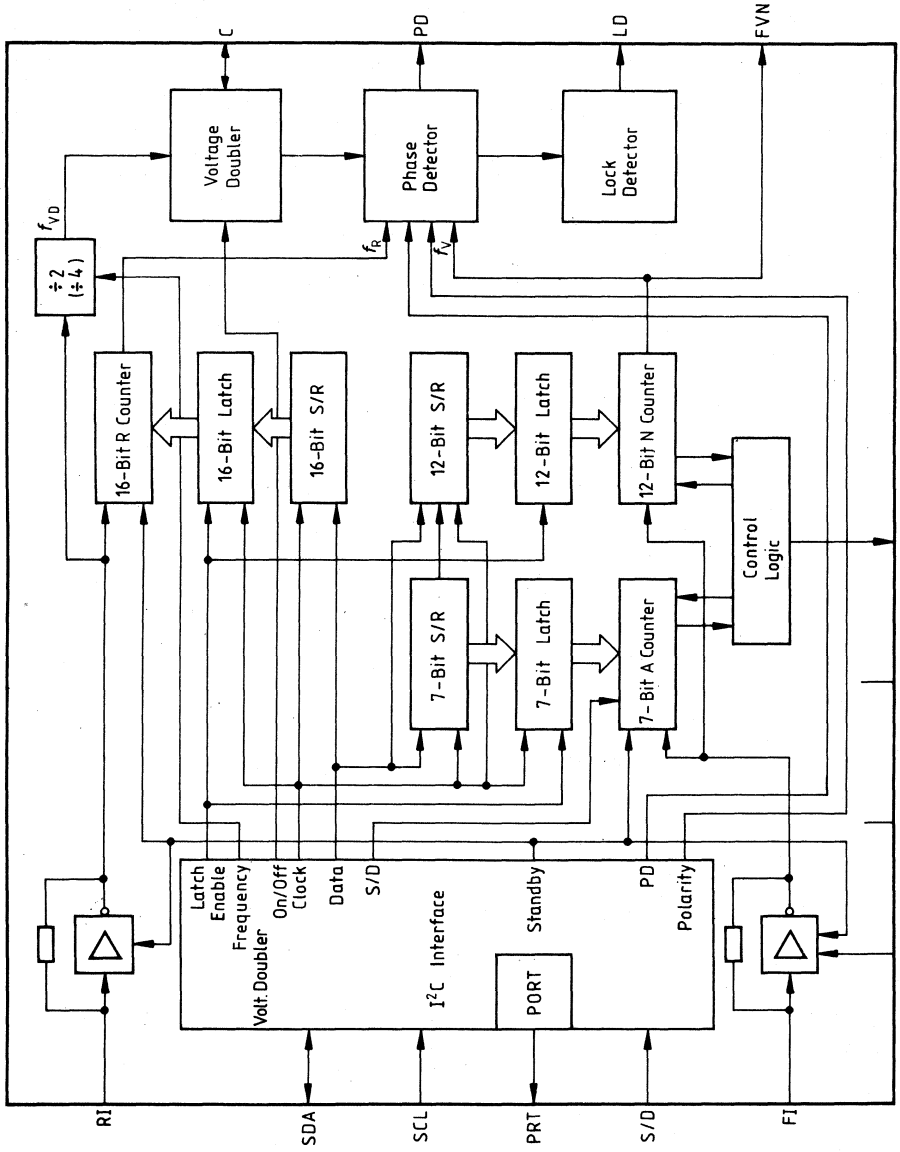
TBB 200 G



Pin Description

Pin	Symbol	Function
1	V_{DD}	Supply voltage
2	RI	Reference frequency
3	S/D	Operating mode (single modulus/dual modulus)
4 5 6	SDA SCL PRT	I²C bus data I²C bus clock I²C PORT
7	MOD	Modulus control
8	FI	VCO frequency
9	GND 2	Ground; FI preamplifier
10	FVN	Comparison frequency
11	GND 1	Ground
12	PD	Phase detector
13	C	Voltage-doubling capacitance
14	LD	Lock detector

Block Diagram



Maximum Ratings

Description	Symbol	min	typ	max	Unit	Notes
Supply voltage	V_{DD}	−0.3		6	V	Exception:
Input voltage	$V_{IM\,1}$	−0.3		V_{DD}+0.3	V	C (internally
Output voltage at C	$V_{IM\,2}$	$-V_{DD}$		0	V	generated)
Power dissipation per output	P_Q			10	mW	
Total power dissipation	P_{tot}			300	mW	
Ambient temperature	T_A	−40		85	°C	
Storage temperature	T_{stg}	−50		125	°C	

Operating Range

Supply voltage		V_{DD}	3	5	5.5	V	
Supply current	single mode	I_{DD}		2.5	3.5	mA	①
	dual mode	I_{DD}		2	3	mA	②
	standby	I_{DD}			1	µA	③
	standby preamplifier on/ divider off	I_{DD}		1.5		mA	④
Ambient temperature		T_A	−40		85	°C	

Test conditions, PLL locked, RI = 10 MHz

①
$f_I = 50$ MHz
$V_{FI\,rms} = 150$ mV
NT, RT > 1000
without voltage doubler

②
$f_I = 10$ MHz
$V_{FI\,rms} = 500$ mV
NT, RT > 1000
without voltage doubler

③
For output wiring refer to test circuit
inputs RI, FI open
$V_{IH\,min}$ (SDA, SCL): V_{DD} −0.5 V
$V_{IH\,max}$ (SDA, SCL): V_{DD}

④
$f_I = 50$ MHz
$V_{FI\,rms} = 150$ mV
NT, RT > 1000

Characteristics

V_{DD} = 4.5 V to 5.5 V; T_A = −40 °C to +85 °C

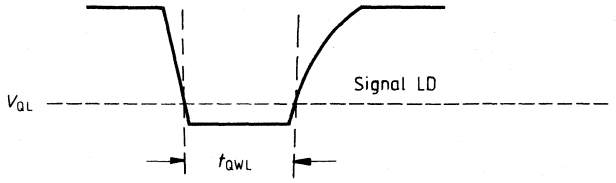
Description	Symbol	Test conditions	min	max	Unit
Input signals SDA, SCL					
H input voltage	V_{IH}		0.7 x V_{DD}	V_{DD}	V
L input voltage	V_{IL}		0	0.3 x V_{DD}	V
Input capacitance	C_I			10	pF
Input current	I_I	$V_I = V_{DD} = 5.5$ V		10	µA
Input signal S/D					
H-input voltage	V_{IH}		0.7 x V_{DD}	V_{DD}	V
L input voltage	V_{IL}		0	0.3 x V_{DD}	V
Input capacitance	C_I			10	pF
Input current	I_I	$V_I = V_{DD} = 5.5$ V		10	µA
Input signal RI					
Input frequency	f_I	$V_{DD} = 4.5$ V		30	MHz
Input voltage	V_I	(sine)	100		mV_{rms}
Input capacitance	C_I			10	pF
Input current	I_I	$V_I = V_{DD} = 4.5$ V		10	µA
Input signal FI (dual modulus)					
Input frequency	f_I	$V_{DD} = 4.5$ V	0.1	30	MHz
Input voltage	V_I	(sine)	50		mV_{rms}
Input capacitance	C_I			10	pF
Input current	I_I	$V_I = V_{DD} = 4.5$ V		10	µA
Input signal FI (single modulus)					
Input frequency	f_I	$V_{DD} = 4.5$ V	70		MHz
Input voltage	V_I	(sine)	10		mV_{rms}
Input frequency	f_I	$V_{DD} = 3$ V		75	MHz
Input voltage	V_I	(sine)	100		mV_{rms}
Input capacitance	C_I			10	pF
Input current	I_I	$V_I = V_{DD} = 4.5$ V		10	µA
Output signal SDA					
L output voltage	V_{QL}	$I_{QL} = 3.0$ mA $V_{DD} = 5$ V $C_L = 400$ pF		0.4	V

Characteristics

V_{DD} = 4.5 V to 5.5 V; T_A = −40 °C to +85 °C

Description	Symbol	Test conditions	min	typ	max	Unit
Output signal PD[1] (Tristate output)						
H current mode	I_{QH}	V_{DD} = 5 V, V_C = 0 V	±1.9	±2.5	±3,1	mA
L current mode	I_{QL}	T_A = −25 °C to 60 °C	±0.475	±0.625	±0.775	mA
Tristate	I_Q			±50		nA
Output signal FVN (Open-drain output)						
L output voltage	V_{QL}	I_{QL} = 1 mA, V_{DD} = 5 V, C_L = 30 pF			0.4	V
L output pulse width	t_{QWL}				1/FI	s
Output signal MOD, PRT						
H output voltage	V_{QH}	I_{QH} = 0.5 mA, V_{DD} = 5 V	V_{DD}−0.4			V
L output voltage	V_{QL}	I_{QL} = 0.5 mA, V_{DD} = 5 V			0.4	V
Output signal MOD (N Channel open-drain)						
L output voltage	V_{QL}	I_{QL} = 0.5 mA, V_{DD} = 5 V			0.4	V
Output signal LD (Open-drain output)						
L output signal	V_{QL}	I_{QL} = 3 mA, V_{DD} = 5 V, C_L = 30 pF			0.4	V
L output pulse width	t_{QWL}			20	40	ns

Pulse diagram



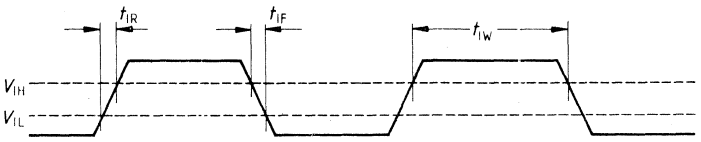
[1]) Symmetry $\frac{|I_{QN} - I_{QP}|}{I_{Q\,typ}} = 20\%$

Dynamic Characteristics

$V_S = 5$ V; $T_A = -40$ to $+85$ °C

Description	Symbol	Test conditions	min	max	Unit
Input signal RI					
Rise time	t_{IR}	$V_{DD} = 5$ V	5		ns
Fall time	t_{IF}	$V_{DD} = 5$ V	5		ns
Pulse width	t_{IW}	$V_{DD} = 5$ V	10		ns
Input signal FI					
Dual Modulus					
Rise time	t_{IR}	$V_{DD} = 5$ V	3.5		ns
Fall time	t_{IF}	$V_{DD} = 5$ V	3.5		ns
Pulse width	t_{IW}	$V_{DD} = 5$ V	3.5		ns
Single Modulus					
Rise time	t_{IR}	$V_{DD} = 5$ V	5		ns
Fall time	t_{IF}	$V_{DD} = 5$ V	5		ns
Pulse width	t_{IW}	$V_{DD} = 5$ V	10		ns

Pulse diagram



Dynamic Characteristics

$V_{DD} = 5$ V; $T_A = -40$ °C to +85 °C

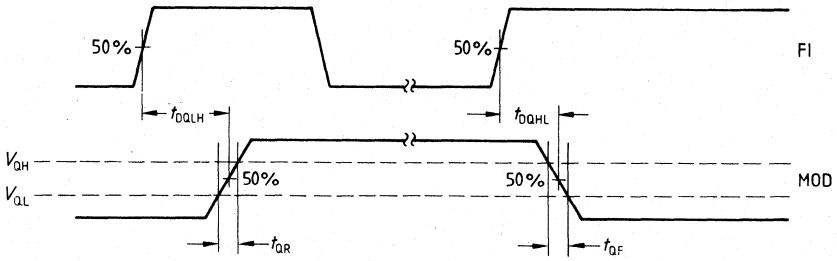
Description	Symbol	Test conditions	min	typ	max	Unit
Voltage doubler						
Output voltage	V_{QC}	$f_{VD} = 2$ MHz $I_{QC} = 0$ µA $V_{DD} = 5$ V	$-V_{DD} + 0.8$ V		$-V_{DD}$	V
	V_{QC}	$f_{VD} = 2$ MHz $I_{QC} = 100$ µA $V_{DD} = 5$ V	$-V_{DD} + 1.5$ V		$-V_{DD}$	V
	V_{QC}	$f_{VD} = 2$ MHz $I_{QC} = 0$ µA $V_{DD} = 3$ V	$-V_{DD} + 0.8$ V		$-V_{DD}$	V
	V_{QC}	$f_{VD} = 2$ MHz $I_{QC} = 100$ µA $V_{DD} = 3$ V	$-V_{DD} + 1.5$ V		$-V_{DD}$	V
Current consumption	I_{VD}	$V_{DD} = 5$ V $I_{QC} = 0$ µA $f_{VD} = 2$ MHz		250		µA
	I_{VD}	$V_{DD} = 3$ V $I_{QC} = 0$ µA $f_{VD} = 2$ MHz		180		µA

Dynamic Characteristics

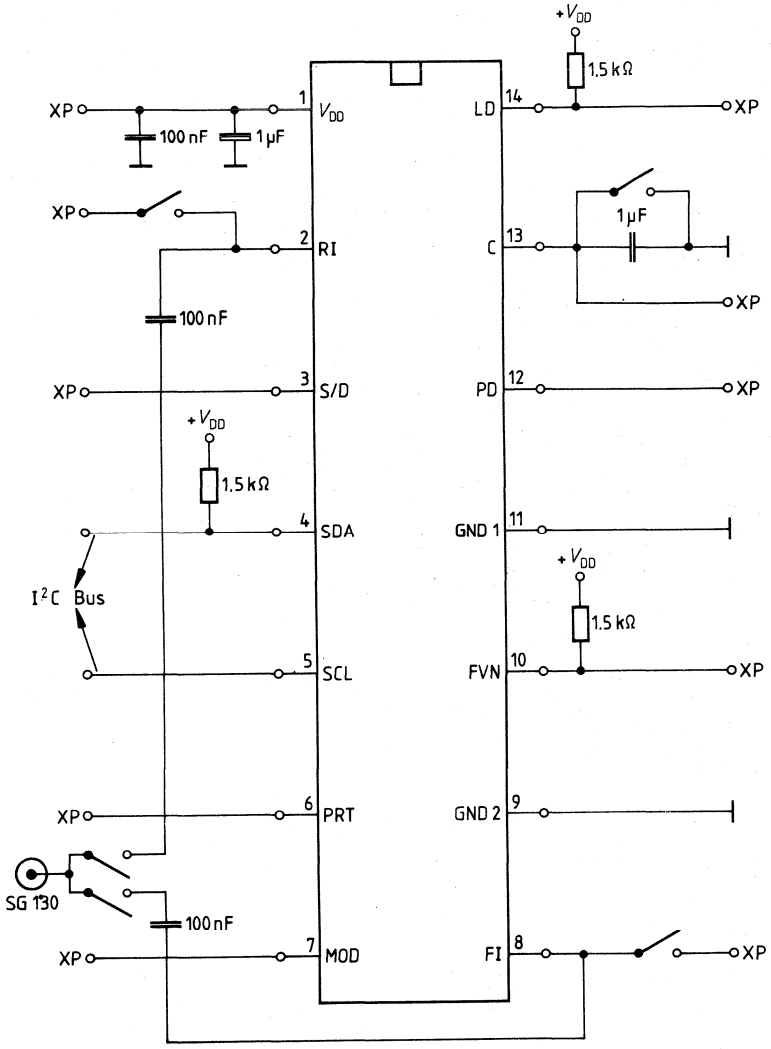
$V_S = 5$ V; $T_A = -40$ to $+85$ °C

Description	Symbol	Test conditions	min	max	Unit
Output signal PRT					
Rise time	t_{QR}	$C_L = 30$ pF		1	µs
Fall time	t_{QF}	$C_L = 30$ pF		1	µs
Output signal FV					
Fall time	t_{QF}	$C_L = 30$ pF		20	ns
Output signal MOD					
Rise time	t_{QR}	$C_L = 30$ pF		10	ns
Fall time	t_{QF}	$C_L = 30$ pF		10	ns
Delay time L-H to FI	t_{DQLH}	$C_L = 30$ pF		25	ns
Delay time H-L to FI	t_{DQHL}	$C_L = 30$ pF		15	ns

Pulse Diagram

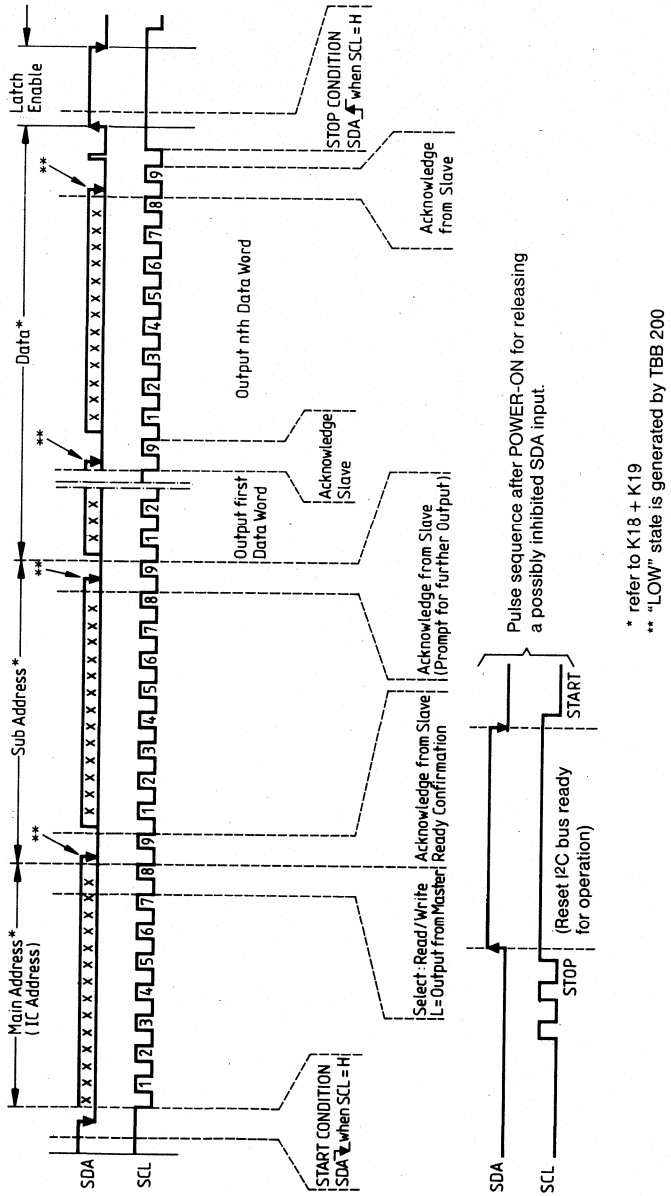


Measurement Circuit



XP = Matrix Pin

I²C Bus Transmission Protocol



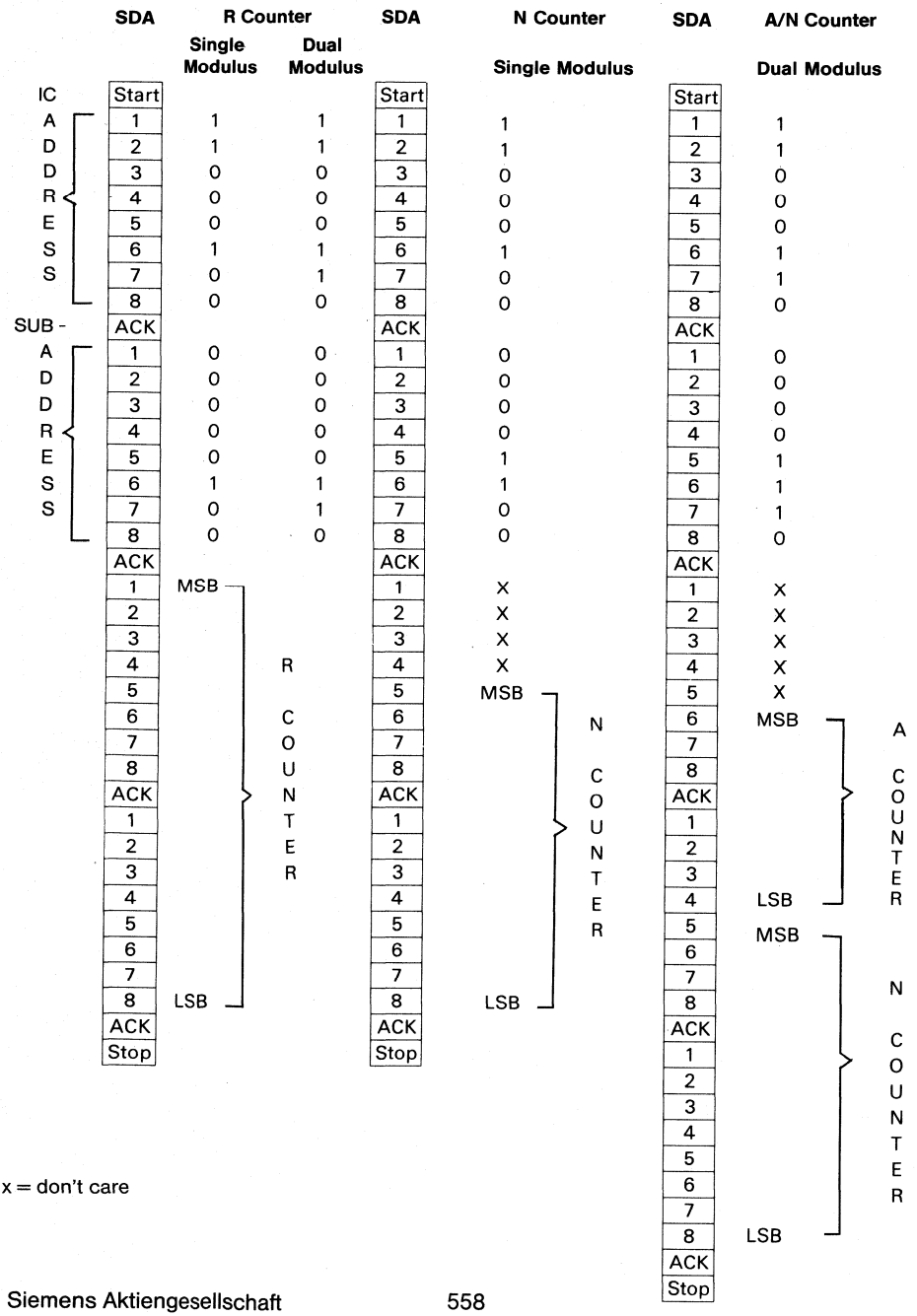
Transmission Protocol for Programming

SDA		STATUS Single Modulus	Dual Modulus
Start			
1	IC	1	1
2	A	1	1
3	D	0	0
4	D	0	0
5	R	0	0
6	E	1	1
7	S	0	1
8	S	0	0
ACK			
1	SUB-	0	0
2	A	0	0
3	D	0	0
4	D	0	0
5	R	1	1
6	E	0	0
7	S	0	1
8	S	0	0
ACK			
1		PORT	
2	S	Counter	
3	T	FI, RI	
4	A	PD Polarity	
5	T	PD Current	
6	U	Voltage-Doubler Frequency	
7	S	Voltage-Doubler Status	
8		Modulus Output	
ACK			
Stop			

Status bit 0	1
Low**	High**
off*	on
off*	on
neg.	pos.
0,625 mA	2,5 mA
÷ 2	÷ 4
off	on
push pull	open drain

* Standby d, f, FVN, LD, MOD are in H state, PD is in tristate.
** PORT output state

Transmission Protocol for Programming

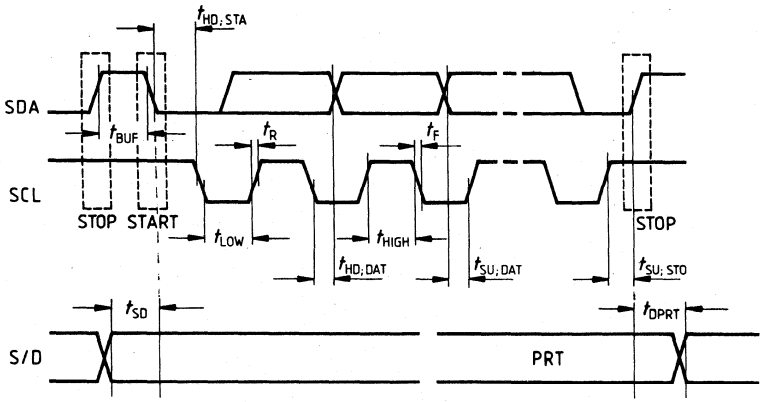


x = don't care

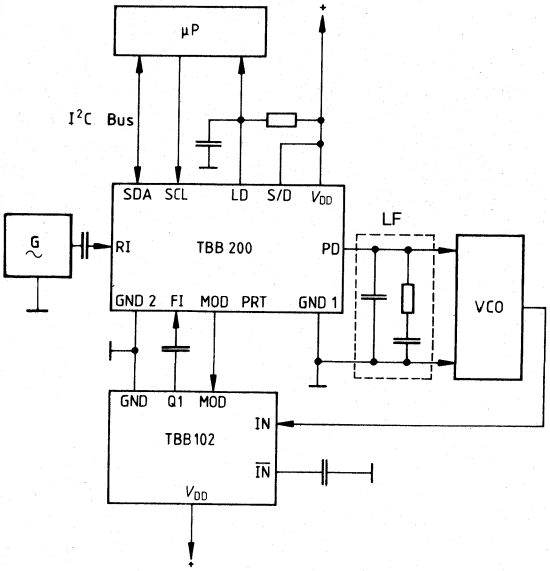
Description	Symbol	min	max	Unit
Clock frequency	f_{SCL}	0	100	kHz
Hold time data to SCL LOW	$t_{HD;\,DAT}$	0		µs
Inactive time prior to next transmission	t_{BUF}	4.7		µs
Start condition hold time (first CLOCK pulse is generated after this time period)	$t_{HD;\,STA}$	4.0		µs
Clock LOW phase	t_L	4.7		µs
Clock HIGH phase	t_H	4.0		µs
DATA set-up time	$t_{SU;\,DAT}$	250		ns
SDA and SCL signal rise time	t_R		1	µs
SDA and SCL signal fall time	t_F		300	ns
SCL pulse set-up time with Stop condition	$t_{SU;\,STO}$	4.7		µs
Status programming set-up time (S/D)	t_{SD}	500		ns
PRT delay time relative to Stop condition	t_{DPRT}		500	ns

All times with reference to specified input levels V_{IH} and V_{IL}.

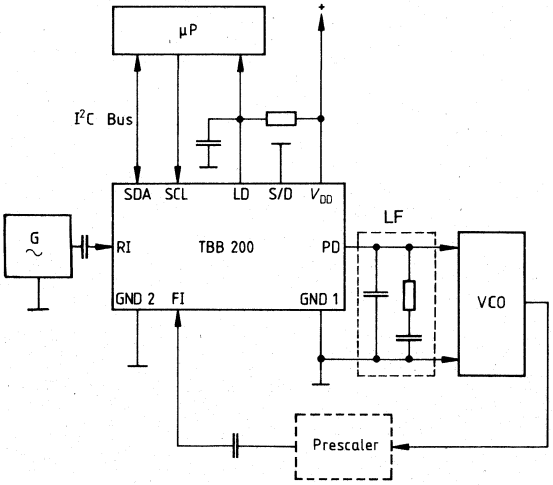
Pulse Diagrams for I²C Bus, S/D, PRT



Application Circuits

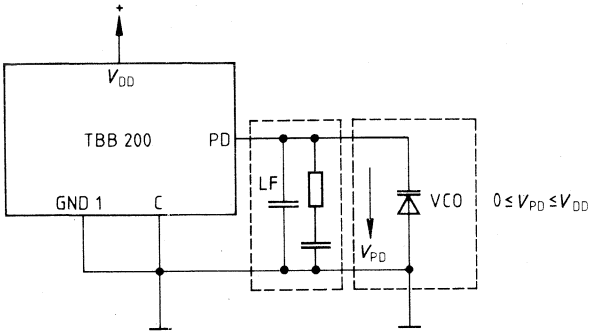


Operation: dual modulus (f_{max} = 30 MHz at FI)

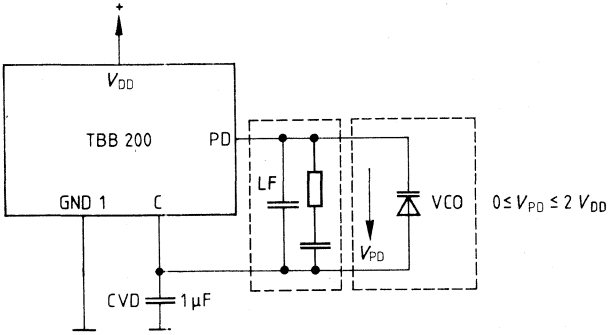


Operation: single modulus (f_{max} = 70 MHz at FI)
LF: loop filter

Application Circuits VCO Coupling

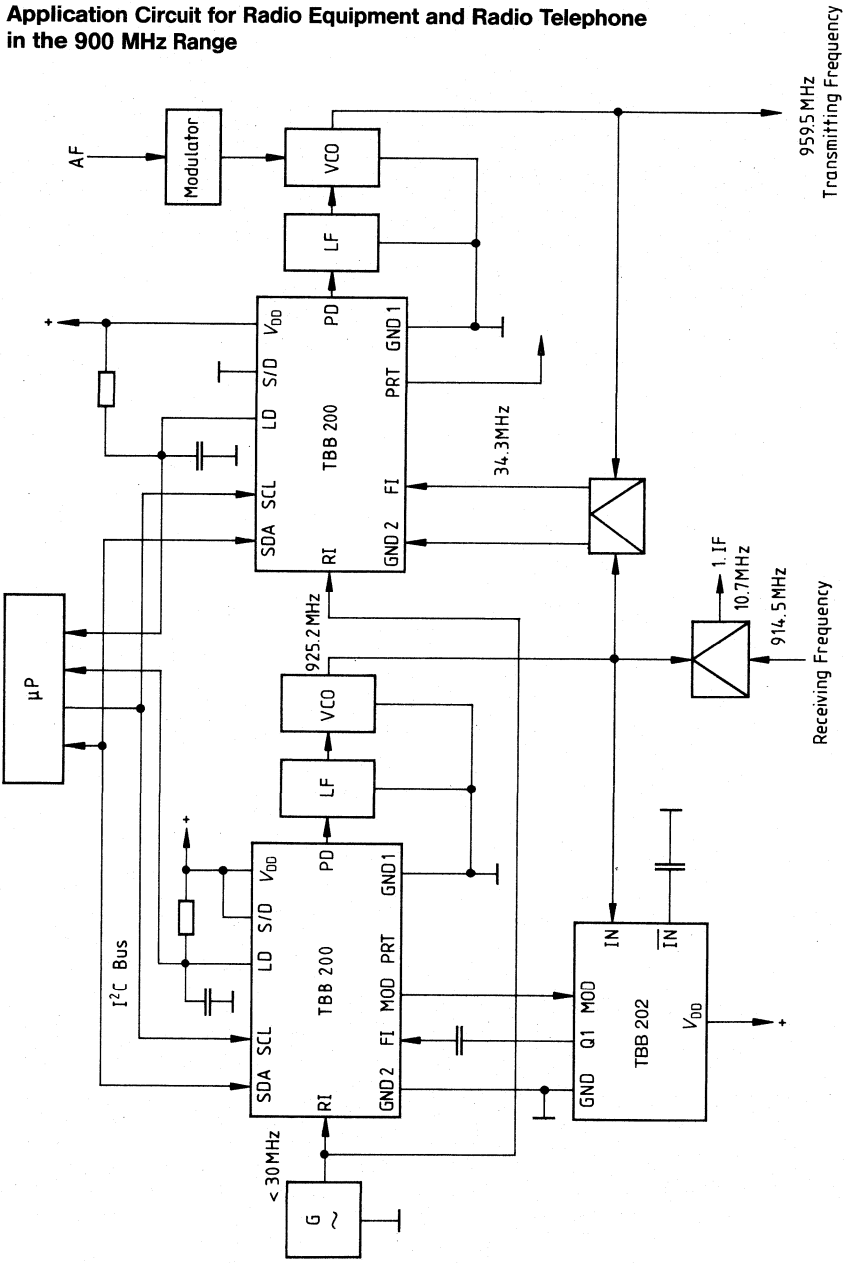


Operation without voltage doubler (status bit 7 = 0)



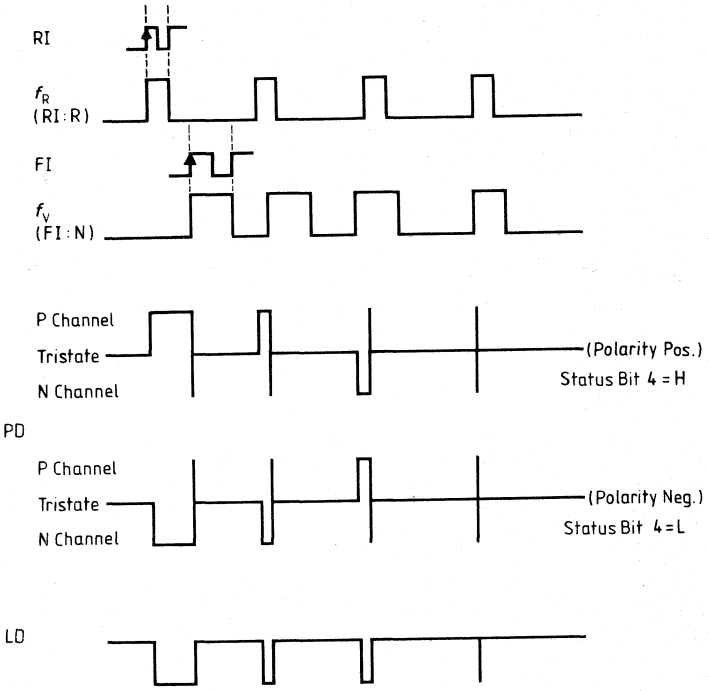
Operation with voltage doubler (status bit 7 = 1)
LF: loop filter

Application Circuit for Radio Equipment and Radio Telephone in the 900 MHz Range



Pulse Diagram

Phase Detector/Lock Detector



Preliminary Data **Bipolar IC**

Type	Ordering Code	Package
TBB 202	Q67000-H8217	P-DIP-8
TBB 202 G	Q67000-H8218	similar to P-DSO-8 (SMD)

The TBB 202 is especially assigned for applications in radiotelephone apparatus. It contains several ECL divider stages, which have a total divider ratio of 1:128/129, depending on the control of the MOD input. It can be employed in standby-mode (input STB = low).

Circuit Description

The component has symmetrical push-pull inputs. If control is unsymmetrical, the unused input has to be blocked by a capacitor (approx. 1.5 nF) with low series inductance. The divider of the component consists of several status-controlled master-slave flipflops, which have a total divider ratio of 1:128/129. The MOD inputs (divider ratio changeover input) and STB (input for standby mode) are controllable with TTL levels. The ECL output of the divider is CMOS-compatible in correspondance with the application circuit (refer to page 568). The typical deviation is 250 mV_{pp}.

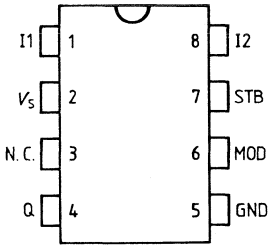
Truth Table for Operating Modes

Operating mode	STB	MOD	Q
Divider 1:128	H	H	H/L
Divider 1:129	H	L	H/L
Standby	L	H/L	H

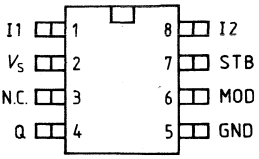
Input	Level	Function
MOD	HIGH LOW	1:128 1:129
STB	HIGH LOW	NORMAL HIGH, STANDBY

Pin Configurations
(top view)

TBB 202



TBB 202 G



Pin Description

Pin	Symbol	Function
1	I1	Input
2	V_S	Supply voltage
3	N.C.	not connected
4	Q	Output
5	GND	Ground
6	MOD	Input for changeover 1:128/129
7	STB	Input for standby mode
8	I2	Input

Maximum Ratings

T_A −40 °C to +85 °C

Description	Symbol	min	max	Unit
Supply voltage	V_S	−0.3	6	V
Input voltage (pin 1; pin 8)	V_I	−0.3	2.5	V
Input voltage (pin 6; pin 7)	V_{MOD}, V_{STB}	−0.3	6	V
Output voltage (pin 4)	V_Q		V_S	V
Output current (pin 4)	$-I_Q$		10	mA
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−65	125	°C
Thermal resistance				
system – air P-DIP-8	$R_{th\ SA}$		115	K/W
P-DSO-8	$R_{th\ SA}$		180	K/W

Operating Range

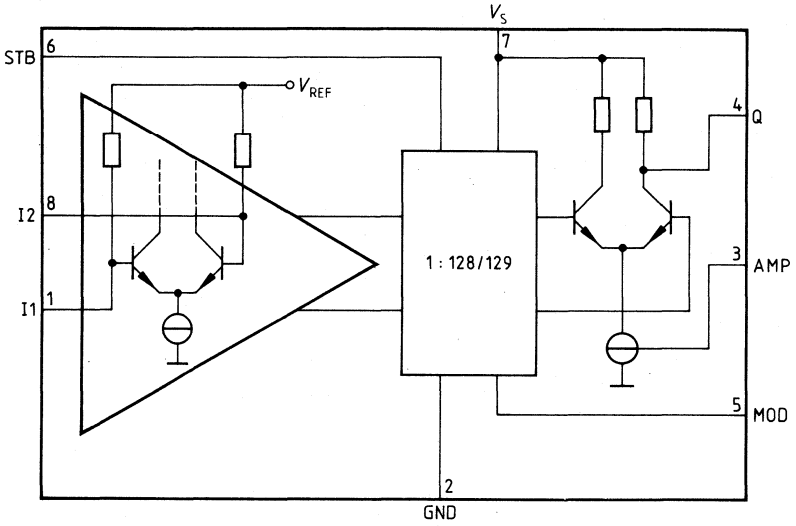
Supply voltage	V_S	3.0	5.5	V
Input frequency	f	200	1100	MHz
Ambient temperature	T_A	−40	85	°C

Characteristics

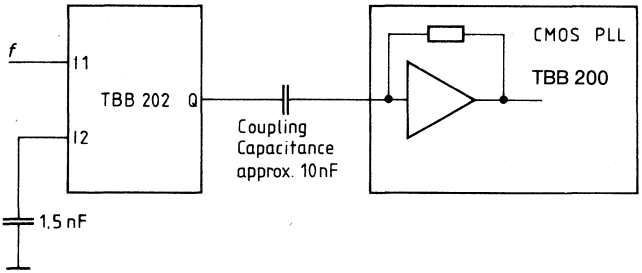
$V_S = 3.0$ to 5.5 V, $T_A = -40\,°C$ to $+85\,°C$

Description	Symbol	Measuring conditions	Meas. circuit	min	typ	max	Unit
Current consumption during operation	I_S	Inputs blocked Output n.c.	1		7		mA
during standby operation	I_S	STB = V_S inputs blocked	1		1.3		mA
Input level (input sensitivity)	V_I	Output n.c., STB = ground					
		200 MHz (sine voltage)	1	20		315	mV_{rms}
		400 MHz	1	17		315	mV_{rms}
		600 MHz	1	14		315	mV_{rms}
		800 MHz	1	14		315	mV_{rms}
		900 MHz	1	14		315	mV_{rms}
		1000 MHz	1	20		315	mV_{rms}
MOD input							
Switching threshold	V_I		1		0.6		V
H-input current	I_{IH}	MOD = V_S (1:128)	1		0	50	µA
L-input current	$-I_{IL}$	MOD = ground (1:129)	1		110	200	µA
Standby input							
H-input voltage (normal operation)	V_{IH}		1	2.0			V
L-input voltage (standby operation)	V_{IL}		1			0.8	V
H-input current	I_{IH}	STB = V_S	1		100	150	µA
L-input current	$-I_{IL}$	STB = ground	1		0	50	µA
Output							
Output voltage swing	V_Q	$C_L \leq 15$ pF	1	150	250		mV_{pp}
Output resistance	R				1		kΩ
Switching times							
Setup time	$t_{Setup\,1}$, $t_{Setup\,2}$				5		ns
Hold time	$t_{Hold\,1}$, $t_{Hold\,2}$				5		ns

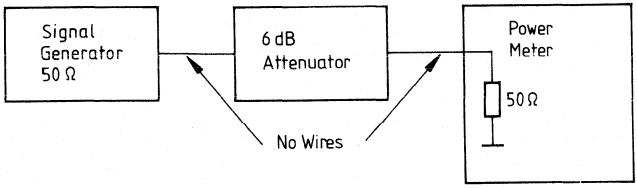
Block Diagram

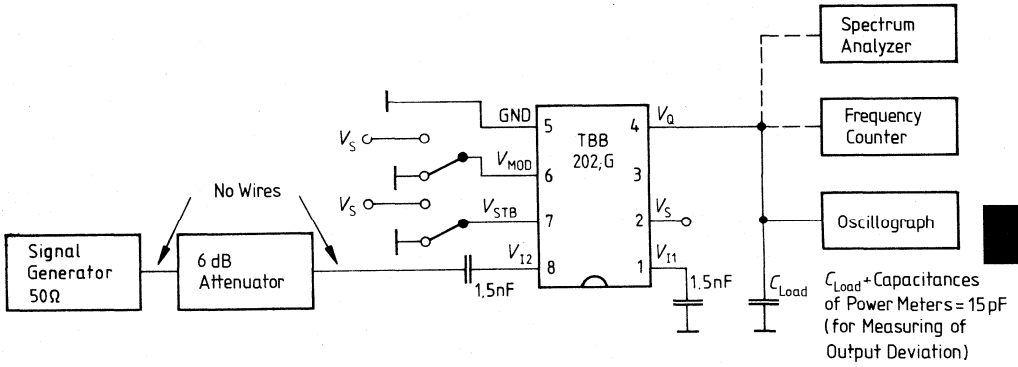


Application Circuit

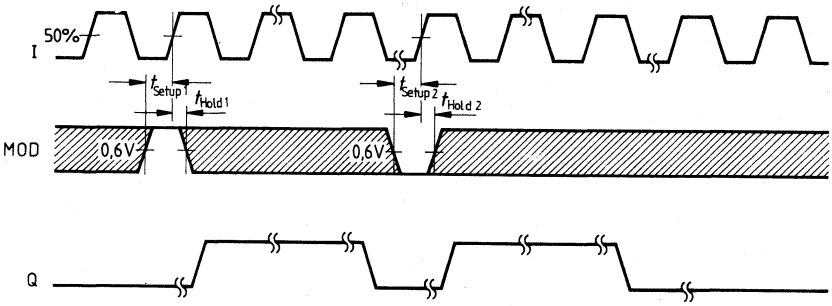


Measuring Circuit 1





Diagram



Preliminary Data **Bipolar IC**

Type	Ordering Code	Package
TBB 30x		Chip
TBB 302	Q67000-R263	P-DIP-16
TBB 303	Q67000-R264	P-DIP-14
TBB 304	Q67000-R266	P-DIP-14

Functional Description

The TBB 30x contains an array of 10x10 Schottky diodes (see block diagram).

A NiCr fuse is serially connected to the diode, which can be fused by a current pulse. This provides for a one-time programming of the matrix by the user.

The diodes have Schottky characteristics with low forward voltage. The matrix is thus particularly suitable for applications in low voltage equipment (e.g. 3 V battery-operated supplies).

The matrix is intended for applications where an electronic identity is required without supply voltage and with high reliability such as pagers, portable radio phones, electricity meters.

The chip has been designed such that arrays of up to 9x10 or 10x9 diodes can be bonded in various packages. One row or column is used for testing.

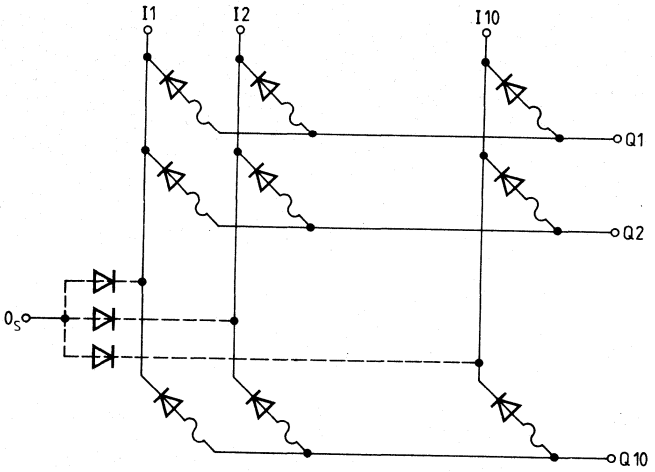
Application Notes

Programming of the matrix has to be done separately for each diode otherwise the diodes might not be properly programmed.

Programming can be accomplished either by means of a voltage-limited current source or a current-limited voltage source. A programming duration of 10 ms is sufficient. The rise time of the required peak value of the programming current or voltage respectively must be $< 1\,\mu s$.

The connection 0_S (substrate of the chip) must be supplied with negative potential with regard to any other matrix connection. Normally, it is connected to ground of the application or programming circuit.

Block Diagram



~ = Fuse

I = Inputs (Cathodes)
Q = Outputs (Anodes)

Due to the integrated structure there are substrate diodes between the inputs and 0_S substrate terminal.
In order not to influence the circuit, 0_S must be connected to the most negative potential
One row or column is used for testing.

Maximum Ratings

$T_A = -25\,°C$ to $+85\,°C$

Description	Symbol	min	max	Unit	Notes
Voltage between I und 0_S	V_{I0}	0	20	V	Isolation breakdown voltage
Voltage between Q and 0_S	V_{Q0}	0	20	V	Isolation breakdown voltage
Voltage between I and Q	V_{IQ}	0	20	V	at $T_A = 25\,°C$
Diode forward current	I_{QI}	0	1	mA	
Programming current	I_{QIP}		70	mA	at $T_A = 25\,°C$
Junction temperature	T_j		125	°C	
Storage temperature	T_{stg}	−40	125	°C	

Operating Range

Voltage between I and 0_S	V_{I0}	0	20	V	
Voltage between Q and 0_S	V_{Q0}	0	20	V	
Voltage between I and Q	V_{IQ}	0	7	V	1)
Diode forward current	I_{QI}	0	1	mA	
Programming current	I_{QIP}	60	70	mA	2)
Rise time of the programming pulse	t_r		1	µs	
Duration of the programming pulse	t_P	10		ms	
Ambient temperature	T_A	−25	85	°C	

1) During programming V_{IQ} must not exceed 20 V at $T_A = 25\,°C$
2) Setting of the current limitation during programming

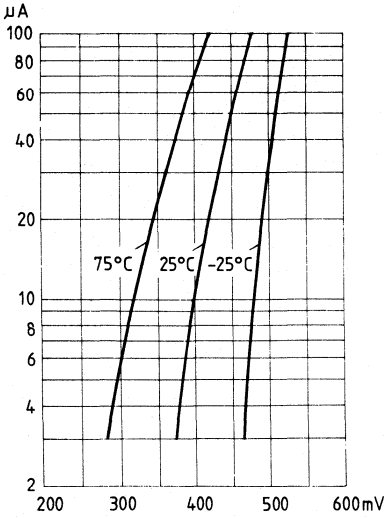
Characteristics

$T_A = 25\,°C$

Description	Symbol	Test condition	min	typ	max	Unit
Diode forward voltage	V_{IQ}	$T_A = 25\,°C$, $I_{IQ} = 10\,\mu A$ $T_A = -25\,°C$, $I_{IQ} = 10\,\mu A$		400 480		mV[1] mV[1]
Diode reverse current Substrate reverse current	I_{IQ} I_{IOS}	$V_{IQ} = 5.5$ V $V_{IOS} = 5.5$ V			100 500	nA nA
Resistance of the fuse programmed as specified	R	$\lvert V_I - V_Q \rvert \leq 5.5$ V	20			MΩ

[1]) see forward characteristics

Forward characteristics Q-I
(typical values)



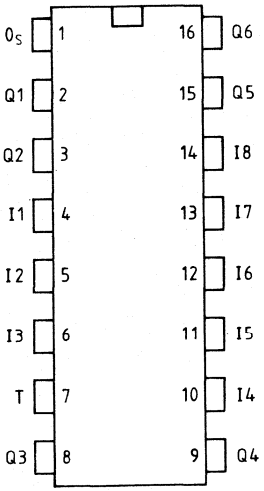
Standard versions available

Functional Description

The circuit contains 8 x 6 Schottky diodes in an array of
8 columns (8 cathodes or 8 inputs) and
6 rows (6 anodes or 6 outputs)

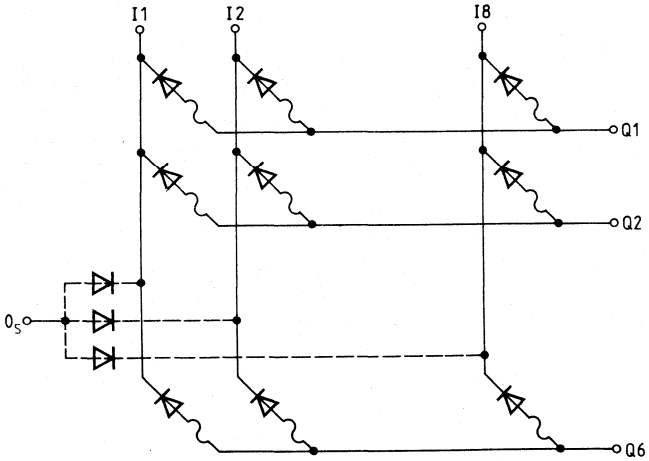
Pin Configuration

(top view)



Pin T is provided for testing only and must not be connected.
I = Input
Q = Output
0_S = Substrate

Block Diagram

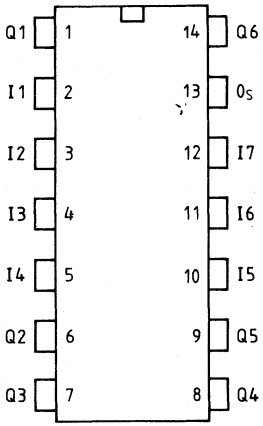


Functional Description

The circuit contains 7 x 6 Schottky diodes in an array of
7 columns (7 cathodes or 7 inputs) and
6 rows (6 anodes or 6 outputs)

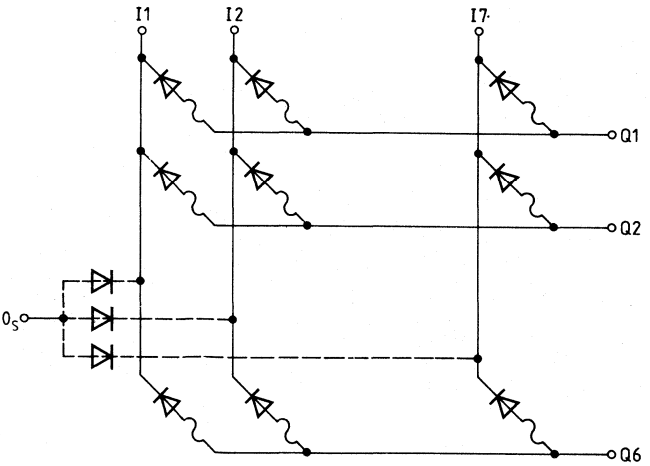
Pin Configuration

(top view)



I = Input
Q = Output
0_S = Substrate

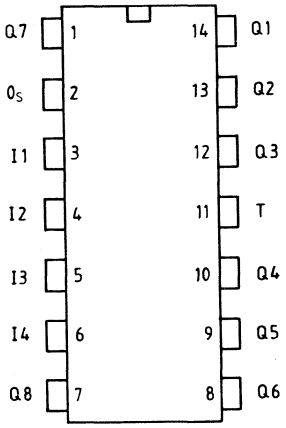
Block Diagram



Functional Description

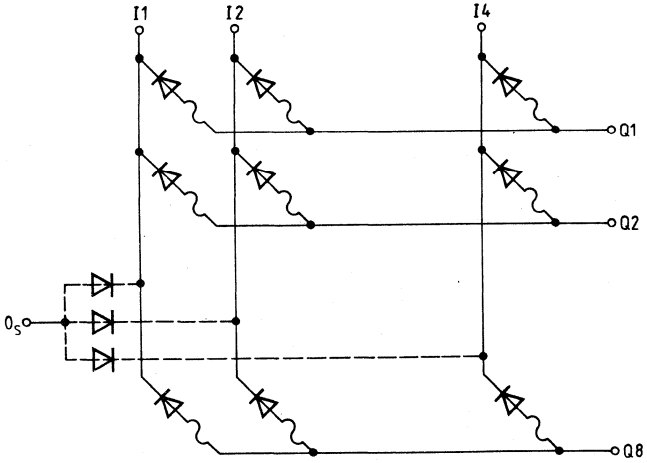
The circuit contains 4 x 8 Schottky diodes in an array of
4 columns (4 cathodes or 4 inputs) and
8 rows (8 anodes or 8 outputs)
The TBB 304 is pin-compatible with the S 1353.

Pin Cinfiguration
(top view)



Pin T is provided for testing only and must not be connected.
I = Input
Q = Output
0_S = Substrate

Block Diagram



Bipolar IC

Type	Ordering Code	Package
S 89	Q67000-H1694	P-DIP-14

Frequency divider with the preselectable divider ratios 50/51, 100/101, 100/102, 200/202.

Maximum input frequency is 500 MHz for divider ratios 100/102 and 200/202, or 250 MHz for divider ratios 50/51 and 100/101.

The S 89 is particularly intended as prescaler for the S 187 B.

Main application: Prescaler in dual-modulus frequency dividers.

Maximum Ratings

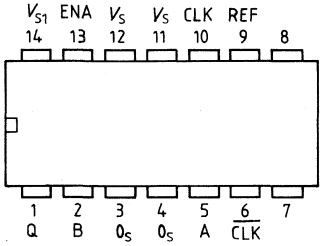
Description	Symbol	min	max	Unit
Supply voltage	V_S	−0.3	7	V
Input voltage ENA Input voltage A, B Input voltage CLK	V_I V_I V_I	−0.3 −0.3 −0.3	15 7 V_S +0.3	V V V
Output voltage Q1, output disabled	V_{Q1}	−0.3	12	V
External voltage at REF	V_I	−0.3	V_S +0.3	V
Output current at Q1 output conducting, V_{S1} open	I_{Q1}		4	mA
Junction temperature Storage temperature range Ambient temperature range	T_j T_{stg} T_A	 −55 −30	125 125 80	°C °C °C
Thermal resistance system – air	$R_{th\ SA}$		75	K/W

Function Data

Description	Symbol	Conditions	min	max	Unit
Supply voltage	V_S		4.5	5.5	V
Input frequency	f_{CLK}	ratios 50/51, 100/101		300[1])	MHz
Input frequency	f_{CLK}	ratios 100/102, 200/202		500[1])	MHz
Input frequency, sinusoidal	f_{CLK}	ratios 50/51, 100/101	20[1])		MHz
Input frequency, sinusoidal	f_{CLK}	ratios 100/102, 200/202	20[1])		MHz

Pin Configuration

(top view)



[1]) Amplitude (peak-to-peak) at CLK: 250 mV ≤ V_{CLKpp} ≤ 400 mV; V_S: 4.75 ≤ V_S ≤ 5.5 V.

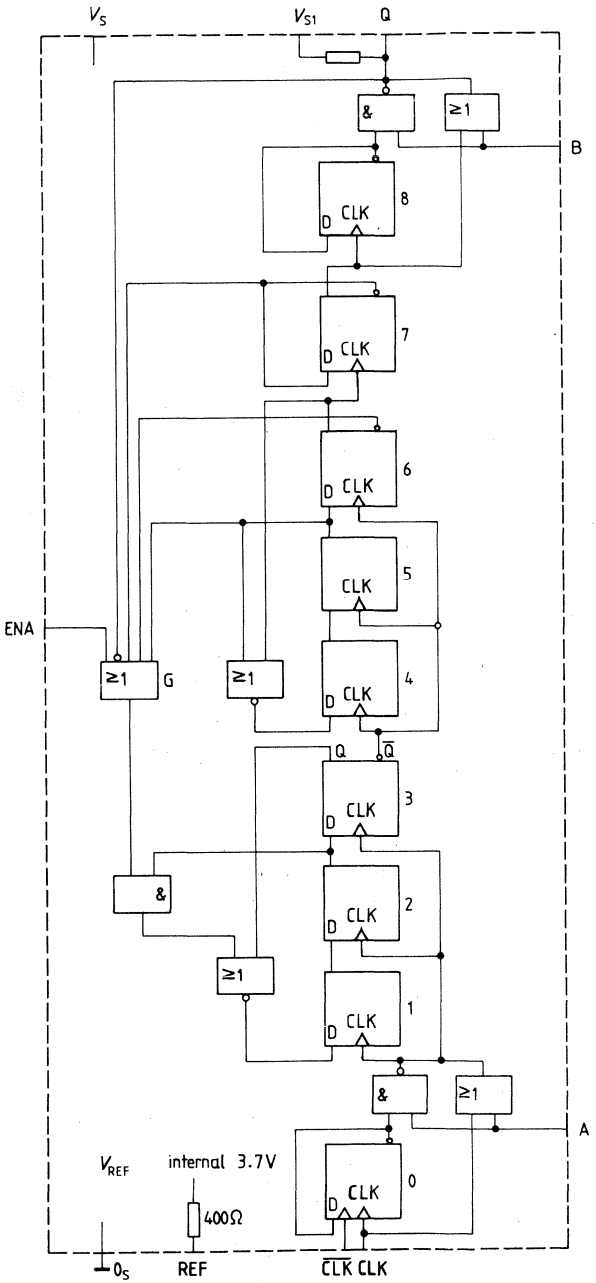
Characteristics
throughout the operating range
$V_S = 5$ V, $T_A = -30$ °C to +80 °C

Description	Symbol	Test conditions	min	typ	max	Unit
Supply voltage	V_S		4.75	5	5.25	V
Supply current	I_S	inputs and outputs open		55	85	mA
L input voltage at ENA	V_{IL}				1	V
H input voltage at ENA	V_{IH}	$T_A = -30$ °C	3.2			V
H input voltage at ENA	V_{IH}	$T_A = 25$ °C	3.0			V
H input voltage at ENA	V_{IH}	$T_A = 80$ °C	2.8			V
H input current at ENA	I_{IH}	$V_{ENA} = V_{ENA\,H} = f(T_A)$		0.17	0.3	mA
H input current at ENA	I_{IH}	$V_{ENA} = 9$ V		1.7	3	mA
L input voltage at A or B	V_{IL}				1.5	V
H input voltage at A or B	V_{IH}		$V_S - 0.1$		$V_S + 0.1$	V
H input current at A or B	I_{IH}	$V_{AB} = V_S$		0.5	1	mA
Threshold voltage at CLK	V_{CLK}	$V_S = 5$ V		3.7		V
Switching voltage deviation at CLK, static (CLK and REF connected)	$V_{CLK\,pp}$	$V_S = 5$ V	250		1600	mV
Switching voltage deviation at CLK at 500 MHz (CLK and REF connected)	$V_{CLK\,pp}$	$V_S = 5$ V	250		400	mV
Output voltage at Q	V_Q	$I_{Q1} = 3.2$ mA			0.5	V
	V_Q	$V_{S1} = 11.5$ V			2	V
		$I_{S1} < 100$ µA				
R between Q and V_{S1}	R_Q	$T_A = 25$ °C	2.0	2.5	3.2	kΩ

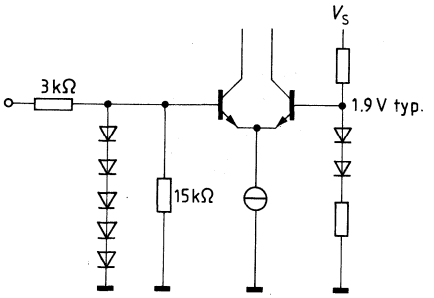
Truth Table

A	B	ENA	f_{CLK}/f_Q	Input frequency MHz min	Input frequency MHz max
H	H	H	200	40	500
H	H	L	202		
H	L	H	100		
H	L	L	102		
L	H	H	100	20	250
L	H	L	101		
L	L	H	50		
L	L	L	51		

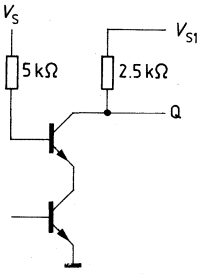
Block Diagram



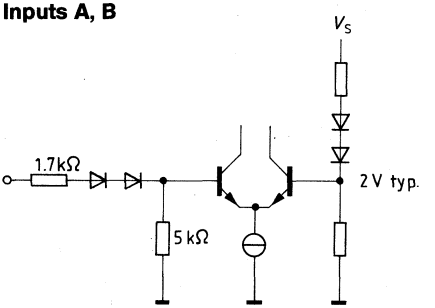
Input ENA



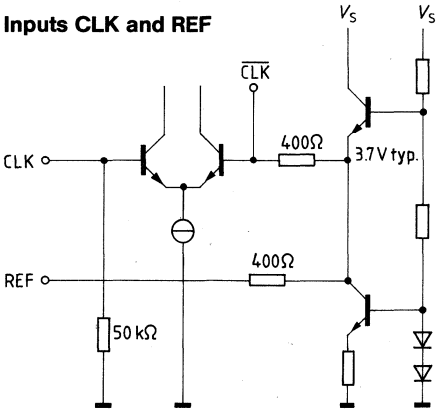
Outputs Q and V_{S1}



Inputs A, B

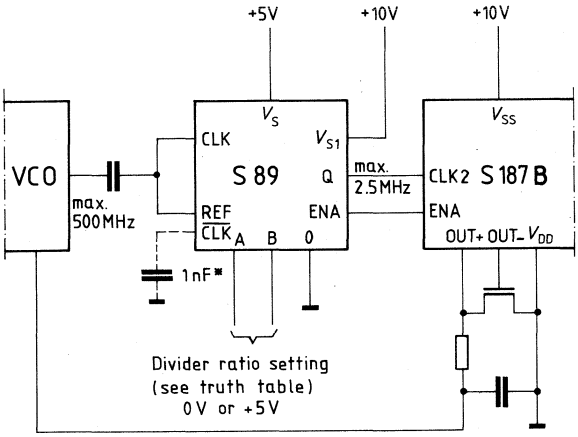


Inputs CLK and REF



Typical Application

Prescaler for PLL circuits S 187 B/C



*) Capacitor is only necessary for operation close to the maximum frequency and maximum input sensitivity

Bipolar IC

Type	Ordering Code	Package	Color Code
S 1531 G	Q67000-A2063	similar to P-DSO-8 (SMD)	orange/green

Functional Description

The AF amplifier was designed for small operating voltages. It is, therefore, specially suited for use in battery-operated equipment.

The open collector outputs can be used to drive center-tapped speakers.

Circuit Description

An unsymmetrically driven differential amplifier with negative feedback to achieve 20 dB voltage gain, is followed by a second differential amplifier that determines the upper cut-off frequency by means of integrated low-pass filters.

Current-controlled booster amplifiers with high current gain are connected to the antiphase outputs of this differential amplifier.

A negative feedback branch to the input of the second differential amplifiers sets the total gain of the circuit to 40 dB $\pm$ 3 dB.

Additional circuitry prevents saturation of the prestage transistors, thereby achieving maximum output power at low harmonic distortion.

A regulating loop serves to make the quiescent current of the output transistors independent of temperature.

The amplifier can be switched on by a muting voltage; with no muting voltage, the amplifier is switched off, except for quiescent currents of some μA.

Maximum Ratings

Description	Symbol	min	typ	max	Unit
Supply voltage	V_S	−0.3		2.0	V
Peak output current	I_Q			250	mA
Muting input voltage	V_M			V_S	V
Junction temperature Storage temperature Ambient temperature	T_j T_{stg} T_A	 −40 −20		125 125 60	°C °C °C
Thermal resistance system – air	$R_{th\ SA}$			200	K/W

Operating Range

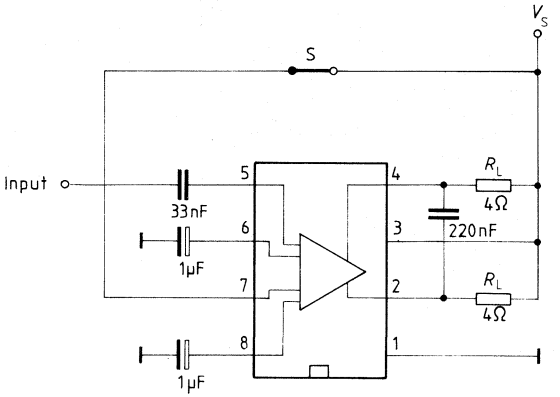
Supply voltage	V_S	1		1.7	V

Characteristics

$V_S = 1.2$ V; $T_A = -10$ °C to +40 °C

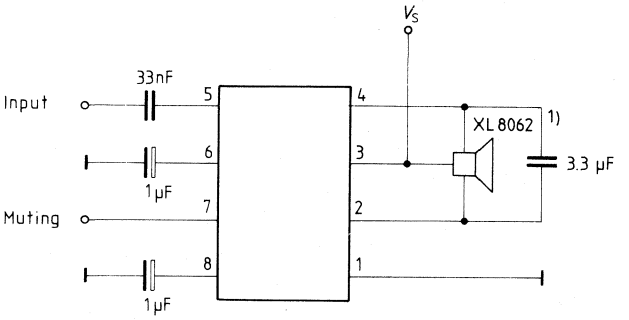
Description	Symbol	Test conditions	Test circuit	min	typ	max	Unit
Quiescent current	I_S I_S	$V_M = V_S$ $V_M = 0$	1 1		5	20 20	mA µA
Output power	P_Q	f=1kHz, THD=10% $R_L = 4\ \Omega$	1		120		mW
Voltage gain	G_V G_V	$T_A = 25$ °C	1 1	37 35	40 40	43 45	dB dB
Cut-off frequency	f_l f_u	−3 dB	1 1	200 5			Hz kHz
Input resistance	R_I		1	30	50		kΩ
Saturation voltage	$V_{CE\ sat}$	$I_Q = 225$ mA	1		300		mV
Muting control current enabled disabled	 I_M I_M			 50		 5	 µA µA
Signal-to-noise ratio	S/N	$P_Q = 50$ mW $R_L = 4\ \Omega$	1		50		dB
Current consumption	I_S	$P_Q = 80$ mW $R_L = 4\ \Omega$	1		140		mA
Efficiency	η	$P_Q = 80$ mW $R_L = 4\ \Omega$	1		48		%
Total harmonic distortion Total harmonic distortion	THD THD	$f = 0.2$ to 5 kHz $P_Q = 80$ mW $f = 0.5$ to 2 kHz $P_Q = 80$ mW	1 2		5 1.5		% %

Figure 1
Measurement Circuit



S closed : amplifier enabled
S open : amplifier disabled

Figure 2
Application Circuit



1) Designation of Messrs. Knowtes, USA.

Power Operational Amplifiers, DC Motor Drivers, Control ICs

Selector Guide

Type			Features							
			Max. output current	Operating range V_S	Max. dielectric strength V_S	Short-circuit proof to $+V_S$	Short-circuit proof to $-V_S$	Free-wheel diodes to $+V_S$	Inhibit	Package
Power operational amplifiers	Single	TCA 365	3 A	36 V	36 V	$V_S < 30$V ●	$V_S < 30$V ●			P-T66-5-H
		TCA 365 B	4 A	40 V	42 V	●	●	●		P-T66-5-H
		TCA 1365 B	4 A	40 V	42 V	●	●	●	●	P-T66-7-H
	Dual	TCA 2365	2.5 A	30 V	36 V	●	●		●	P-SIP-9
		TCA 2365 A	2.5 A	30 V	36 V	●	●		●	P-DIP-18-L9
		TCA 2465	2.5 A	40 V	42 V	●	●	●	●	P-SIP-9
		TCA 2465 A	2.5 A	40 V	42 V	●	●	●	●	P-DIP-16-L10
Full-bridge dc motor drivers	DC motor ICs	TLE 4201 A1	1 A	17 V	36 V		●			P-DIP-18-L9
		TLE 4201 S1	1 A	17 V	36 V		●			P-SIP-9
		TLE 4202	1.5 A	17 V	36 V		●			P-T66-7-H
		TLE 4202 B	2 A	17 V	36 V		●	●		P-T66-7-H
		TLE 4204	3 A	24 V	45 V	●	●	●		P-T66-7-H
	Stepper motor ICs	TCA 1560 B	1.25 A	40 V	45 V	●		●	●	P-DIP-18-L9
		TCA 1561 B	2.5 A	40 V	45 V	●		●	●	P-SIP-9

Bipolar IC

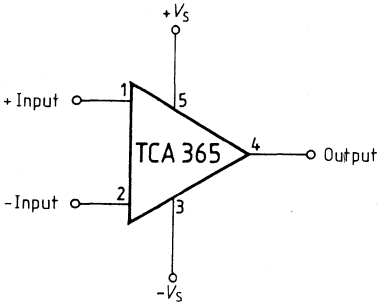
Type	Ordering Code	Package
■ TCA 365	Q67000-A1875	Plastic power package P-T66-5-H
■ TCA 365 H	Q67000-A2145	Plastic power package P-T66-5-J (similar to TO-220)

The TCA 365 ICs are power op amps in a P-T66-5-H or a P-T66-5-J package. At a maximum supply voltage of ±18 V, the ICs deliver a high output current of 3.0 A. The op amps are protected against thermal overload.

Features

- High peak output current, up to 3.0 A
- High supply voltage, up to 36 V
- Fast slew rate of 5 V/µs
- Thermal overload protection
- Internal power limitation

Pin Configuration



Pin 3 is electrically connected to cooling fin.

■ Not for new design

Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	±18	V
Differential input voltage	V_{ID}	$\pm V_S$	V
Peak output current	I_Q	3.0	A
Junction temperature Storage temperature range	T_j T_{stg}	150 −55 to 125	°C °C
Total power dissipation (at $T_C = 90$ °C)	P_{tot}	15	W
Thermal resistance system - case	$R_{th\ SC}$	5	K/W

Operating Range

Supply voltage	V_S	±4 to ±18	V
Ambient temperature	T_A	−25 to 85	°C
Voltage gain	$G_{V\ min}$	20	dB

Characteristics

$V_S = \pm 15$ V, $T_C = +25$ °C

Description	Symbol	Test circuit	min	typ	max	Unit
Open-loop supply current consumption	I_S	1		20	40	mA
Input offset voltage	V_{I0}	2	−10		10	mV
Input offset current Input current	I_{I0} I_I	3 3	−100	 0.2	100 1	nA µA
Output voltage $R_L = 13\ \Omega$ $R_L = 4.7\ \Omega$ Output voltage ($R_L = 470\ \Omega$, $f = 100$ kHz, $G_V = 30$ dB)	$V_{Q\ pp}$ $V_{Q\ pp}$	4 4	±12.5 ±11.7	±13 ±12 ±10		V V V
Input resistance ($f = 1$ kHz)	R_I	4	1	5		MΩ
Open-loop voltage gain ($R_L = 8.2\ \Omega$, $f = 100$ Hz)	G_{V0}	5	80	90		dB
Common-mode input voltage range	V_{IC}	6	+13.4/−15	+13.5/−15.1		V
Common-mode rejection Supply voltage rejection	k_{CMR} k_{SVR}	6 7	75 70	83 80		dB dB
Temperature coefficient of V_{I0} $-25 \le T_C \le 85$ °C Temperature coefficient of I_{I0} $-25 \le T_C \le 85$ °C	α_{VIO} α_{IIO}	2 3		50 0.4		µV/K nA/K
Slew rate of V_Q for non-inverting operation[1]) Slew rate of V_Q for inverting operation[1])	SR SR	8 9		5 5.5		V/µs V/µs
Equivalent input noise voltage	V_n	1		3		µV

[1]) For the relationship between power bandwidth and slew rate refer to **"General Information"**

Test Circuits

Figure 1
Open-loop supply current consumption, equivalent input noise voltage

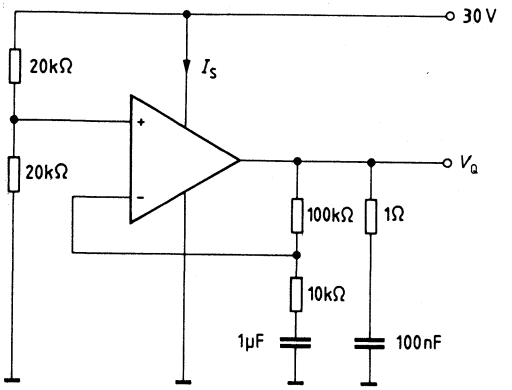


Figure 2
Input offset voltage, *TC* of V_{IO}

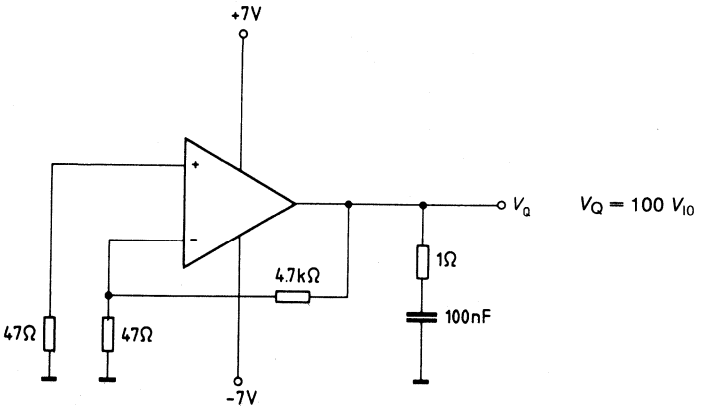
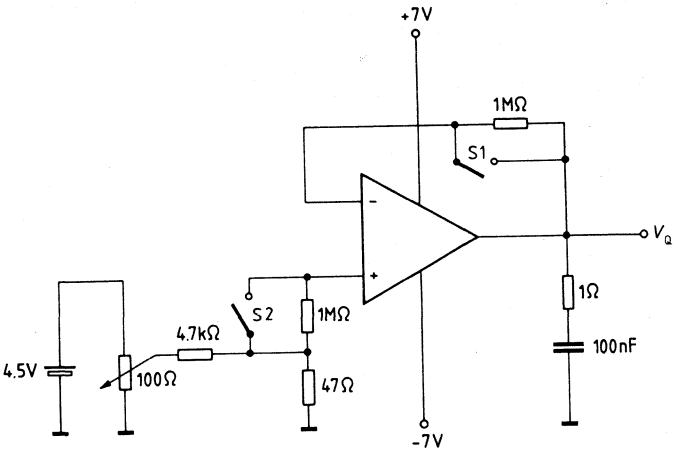


Figure 3
Input offset current; input current, temperature coefficient of I_{IO}



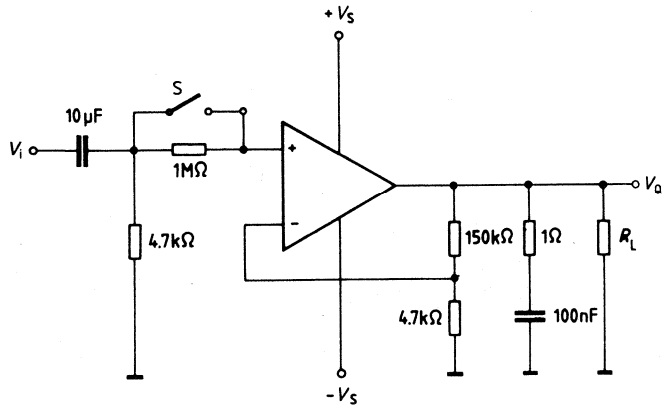
S1 open – S2 closed: $I_{I-} = \frac{V_Q}{1\,M\Omega}$

S2 open – S1 closed: $I_{I+} = \frac{V_Q}{1\,M\Omega}$

S1 open – S2 open: $I_{IO} = \frac{V_Q}{1\,M\Omega}$

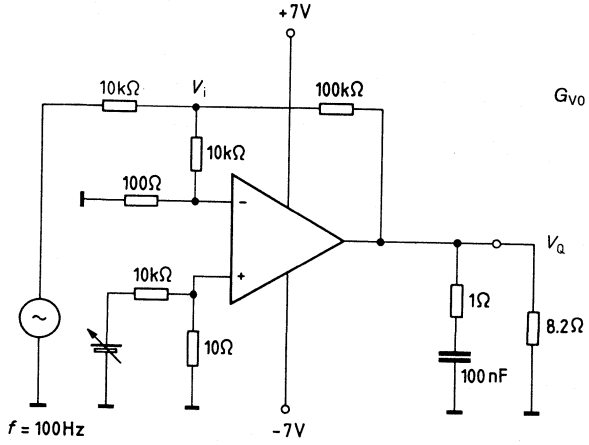
S1 closed – S2 closed: offset alignment

Figure 4
Output voltage, input resistance



S closed: to measure V_{Qpp}
S open/closed: to measure R_I

Figure 5
Open-loop voltage gain



$$G_{V0} = \left| 20 \log 101 \times \frac{V_Q}{V_i} \right|$$

Figure 6
Common-mode voltage gain G_{VC}
Common-mode rejection k_{CMR} (dB) = G_{V0} (dB) − G_{VC} (dB)

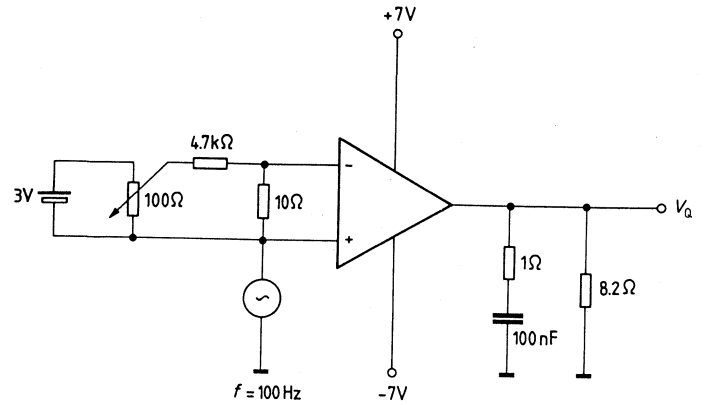
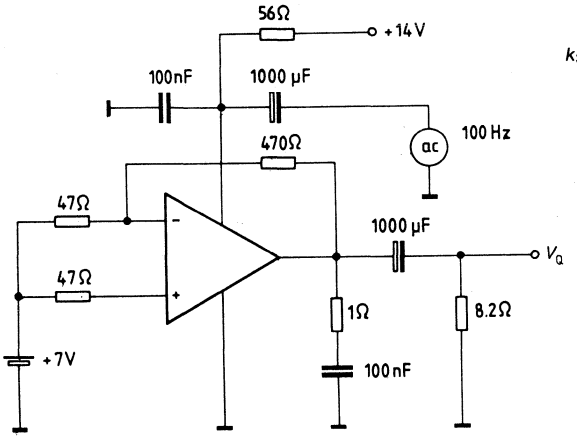


Figure 7
Supply voltage rejection



$$k_{SVR} = 20 \log \frac{\Delta V_Q}{G_V \times \Delta V_S} \text{ [dB]}$$

Figure 8
Slew rate for non-inverting operation

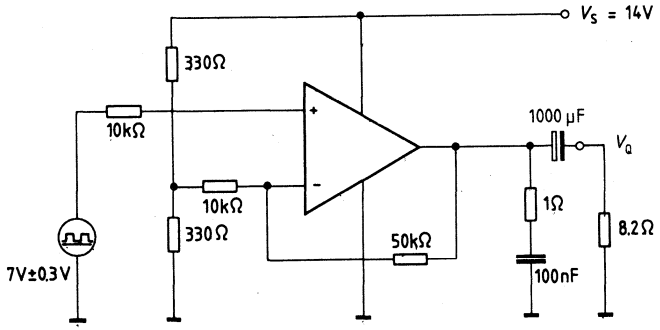
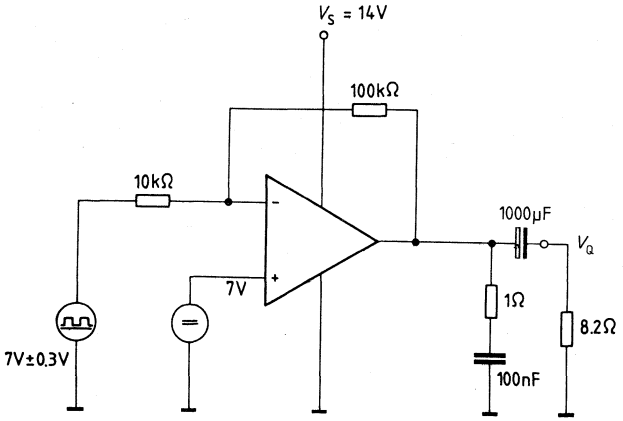
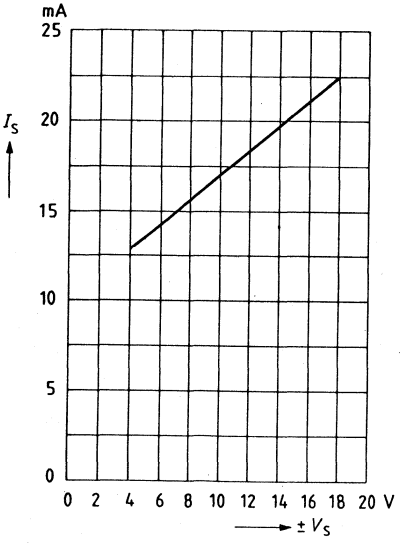


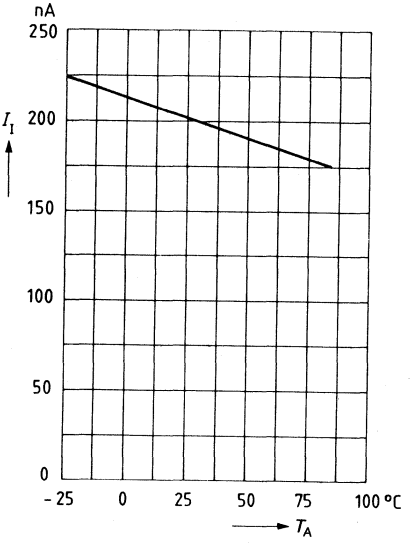
Figure 9
Slew rate for inverting operation



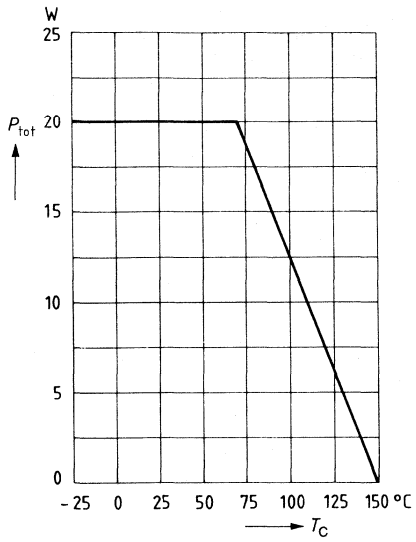
Supply current versus supply voltage



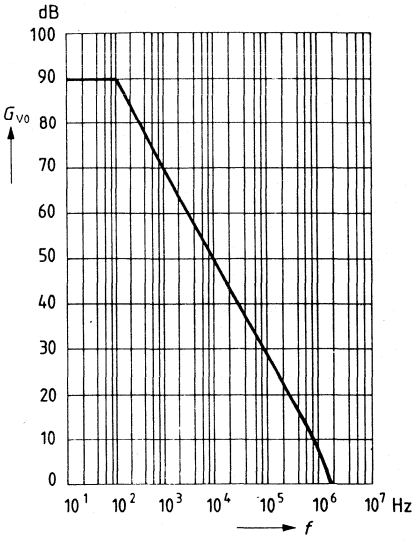
Input current versus ambient temperature



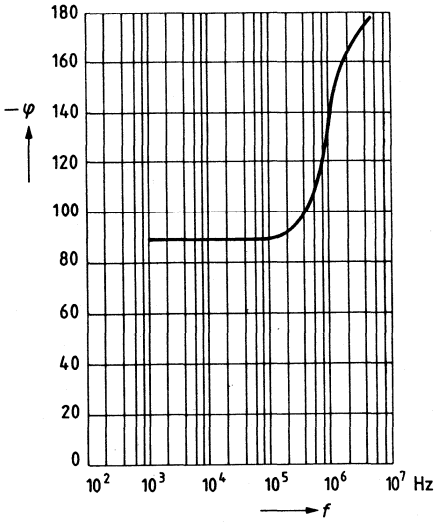
Total power dissipation versus case temperature



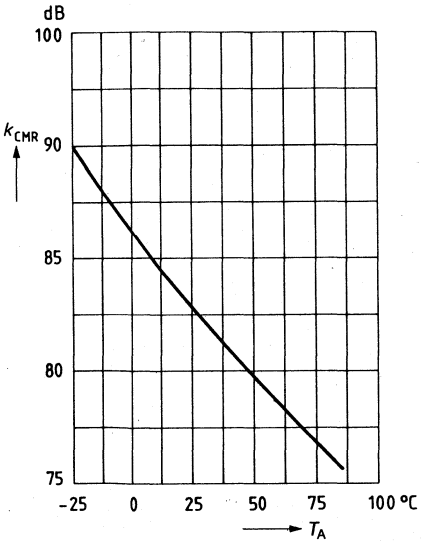
Open-loop voltage gain versus frequency



Phase response versus frequency



Common-mode rejection versus ambient temperature



Preliminary Data **Bipolar IC**

Type	Ordering Code	Package
TCA 365 B	Q67000-A8189	Plastic power package P-T66-5-H (similar to TO-220)

The TCA 365 B is a power op amp in a plastic package P-T66-5-H. At a maximum supply voltage of ±21 V, the IC delivers a high output current of 4 A. The op amp is protected against thermal overload and short circuits.

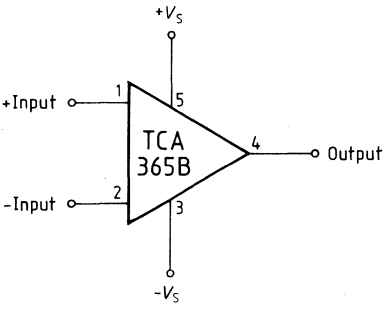
Features

- High peak output current, up to 4 A
- High supply voltage, up to 42 V
- Thermal overload protection
- Internal power limitation
- DC voltage short-circuit proof to $+V_S$ and $-V_S$
- Integrated free-wheel diodes

Applications

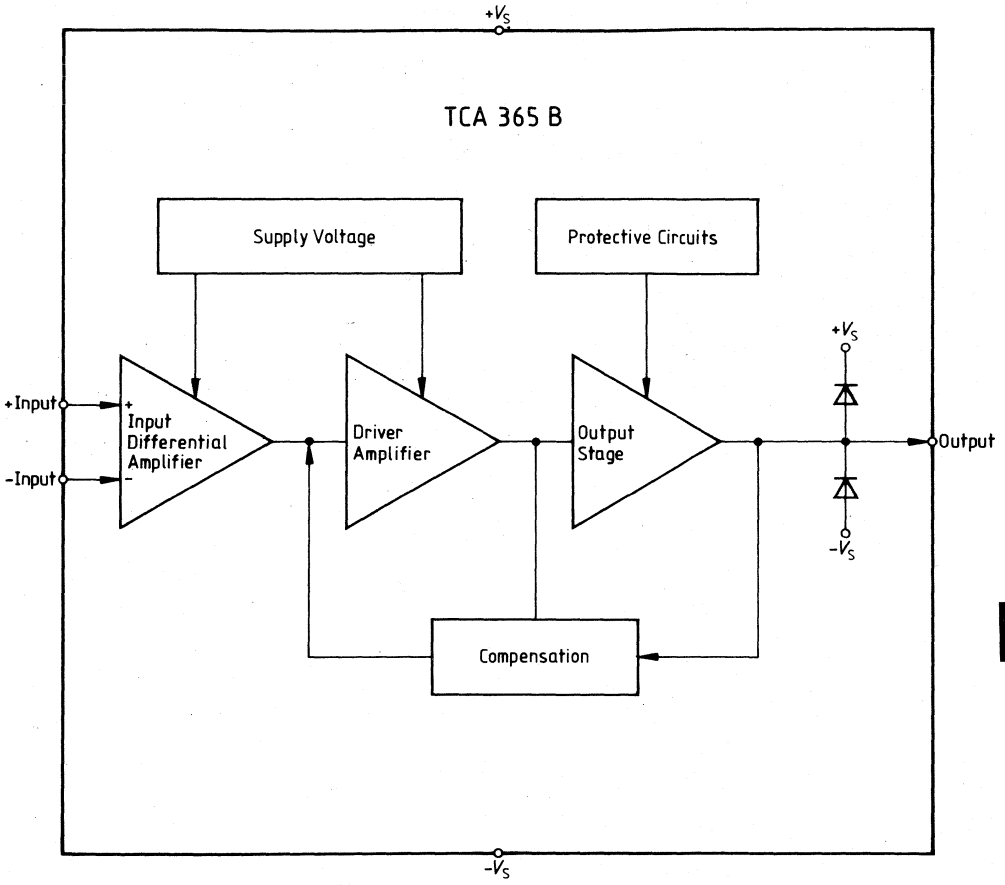
- Power comparator
- Power Schmitt trigger
- Speed control of dc motors

Pin Configuration



Pin 3 is electrically connected to cooling fin.

Block Diagram



Maximum Ratings

$T_C = -25\,°C$ to $+85\,°C$

Description	Symbol	min	max	Unit	Notes
Supply voltage	V_S	0	±21	V	
Differential input voltage	V_{ID}	$-V_S$	$+V_S$	V	
Supply current	I_S	−3.5	4.0	A	
Output current	I_Q	−4.0	4.0	A	
Output current	I_Q	−2.0		A	$V_S \geq \pm 15$ V, $V_Q < -V_S$
Output current	I_Q	−3.0		A	$V_S \geq \pm 10$ V, $V_Q < -V_S$
Ground current	I_{GND}	−4.0	3.5	A	
Power dissipation at $T_C = 85\,°C$	P_D		20	W	
Junction temperature	T_j		150	°C	
Storage temperature range	T_{stg}	−50	150	°C	

Operating Range

Supply voltage	V_S	±3	±20	V	
Case temperature	T_C	−25	85	°C	$P_D = 13$ W
Voltage gain	$G_{V\,min}$	20		dB	
Forward current of free-wheel diode	I_F		3	A	$T_{j\,max} = 125\,°C$
Thermal resistance					
system – air	$R_{th\,SA}$		65	K/W	
system – case	$R_{th\,SC}$		3	K/W	

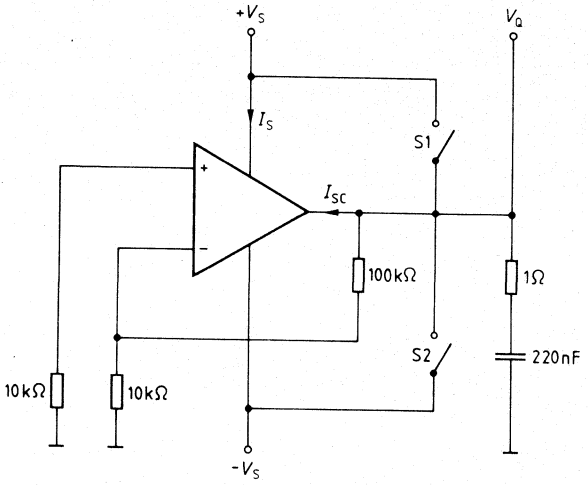
Characteristics

$V_S = \pm 15$ V, $T_C = 25$ °C

Description	Symbol	Test circuit	min	typ	max	Unit
Open-loop supply current consumption	I_S	1		20	40	mA
Input offset voltage	V_{IO}	2	−10		10	mV
Input offset current Input current	I_{IO} I_I	3 3	−100	 0.2	100 1	nA µA
Output voltage $R_L = 12\ \Omega$; $f = 1$ kHz $R_L = 4\ \Omega$; $f = 1$ kHz	 $V_{Q\,pp}$ $V_{Q\,pp}$	 4	 ±13.0 ±12.5	 ±13.5 ±13.0		 V V
Input resistance $f = 1$ kHz	R_I	4	1	5		MΩ
Open-loop voltage gain $f = 100$ Hz	G_{VO}	5	70	80		dB
Common-mode input voltage range	V_{IC}	6	+13/−15	+13.5/−15.1		V
Common-mode rejection Supply voltage rejection	k_{CMR} k_{SVR}	6 7	70 −70	80 −80		dB dB
Temperature coefficient of V_{IO} $-25\,°C \le T_C \le +85\,°C$ Temperature coefficient of I_{IO} $-25\,°C \le T_C \le +85\,°C$	α_{VIO} α_{IIO}	2 3		50 0.4		µV/K nA/K
Slew rate of V_Q for non-inverting operation Slew rate of V_Q for inverting operation	SR SR	8 9		2 2		V/µs V/µs
Noise voltage referred to input (DIN 45405)	V_n	1		2	5	µV
Short-circuit current (S1 closed) (S2 closed)	 I_{SC} I_{SC}	 1 1	 	 0.75 −0.75	 	 A A

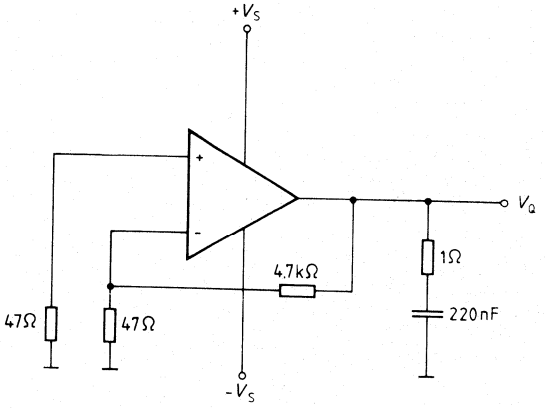
Test and Measurement Circuits

Figure 1
Open-loop supply current consumption, noise voltage



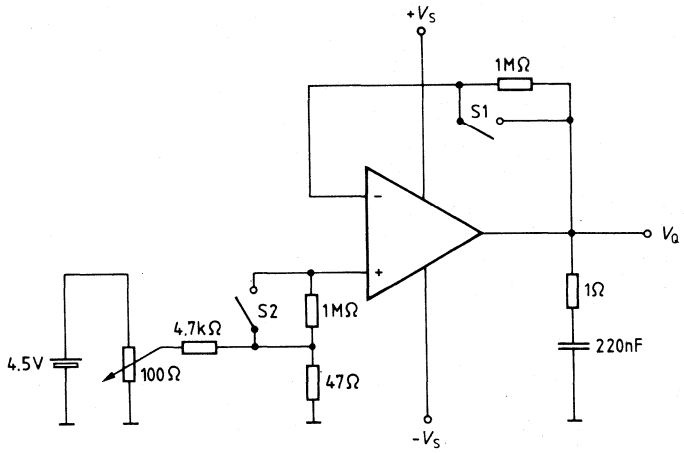
S1 and S2 as shown unless otherwise specified

Figure 2
Input offset voltage, temperature coefficient of V_{IO}



$V_Q = 100\ V_{IO}$

Figure 3
Input offset current; input current, temperature coefficient of I_{IO}



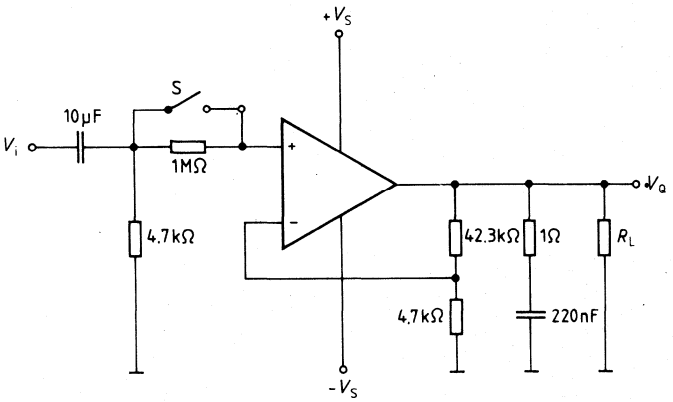
S1 open – S2 closed: $I_{I-} = \frac{V_Q}{1\,M\Omega}$

S2 open – S1 closed: $I_{I+} = \frac{V_Q}{1\,M\Omega}$

S1 open – S2 open: $I_{IO} = \frac{V_Q}{1\,M\Omega}$

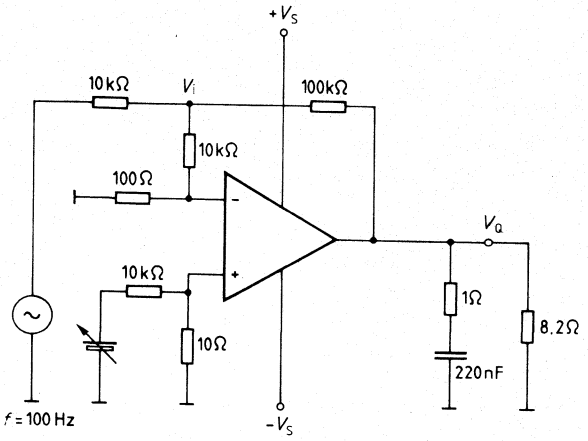
S1 closed – S2 closed: offset alignment

Figure 4
Output voltage, input resistance



S closed: to measure V_{Qpp}
S open/closed: to measure R_I

Figure 5
Open-loop voltage gain



$$G_{V0} = \left| 20 \log 101 \frac{V_Q}{V_I} \right| \text{(dB)}$$

Figure 6
Common-mode voltage gain G_{VC}
Common-mode rejection k_{CMR} (dB) = G_{V0} (dB) − G_{VC} (dB)

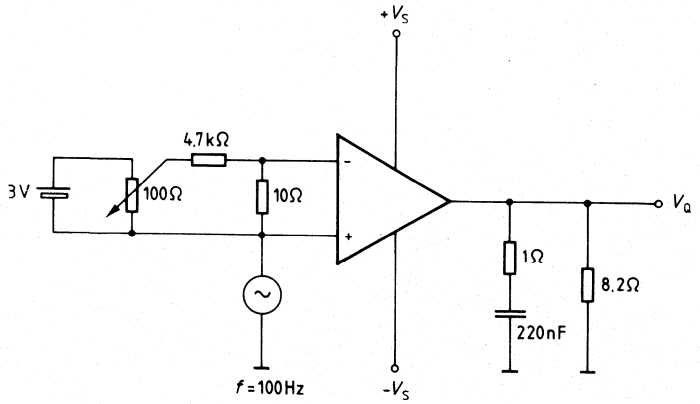
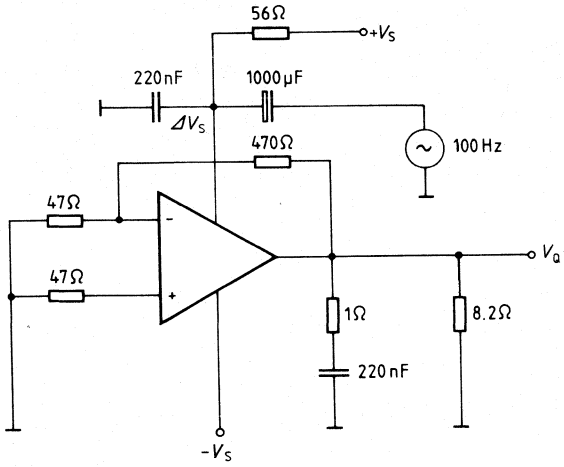


Figure 7
Supply voltage rejection



$$k_{SVR} = 20 \log \frac{\Delta V_Q}{G_V \times \Delta V_S} \text{ (dB)}$$

Figure 8
Slew rate for non-inverting operation

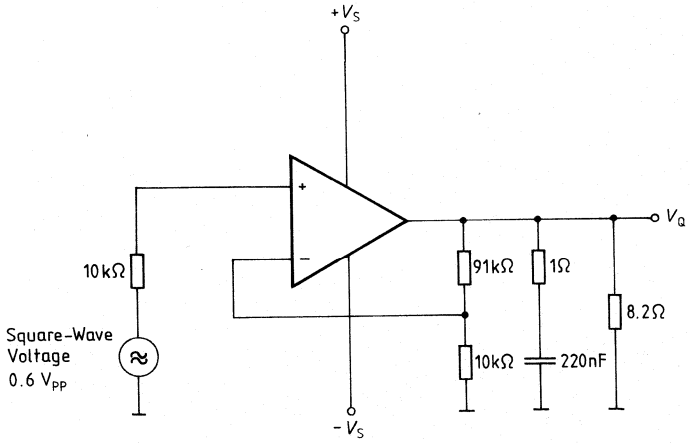
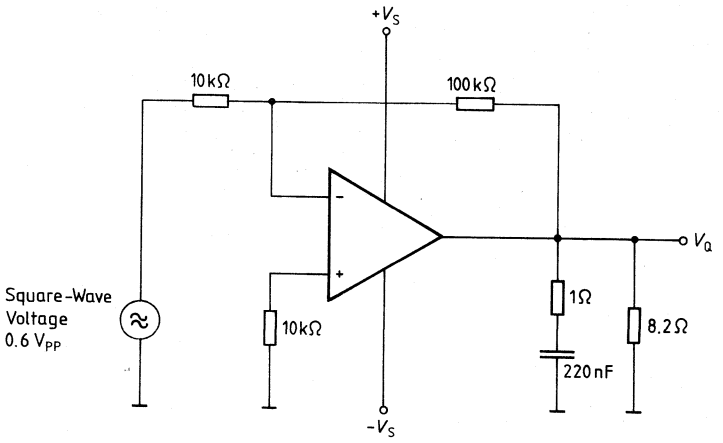
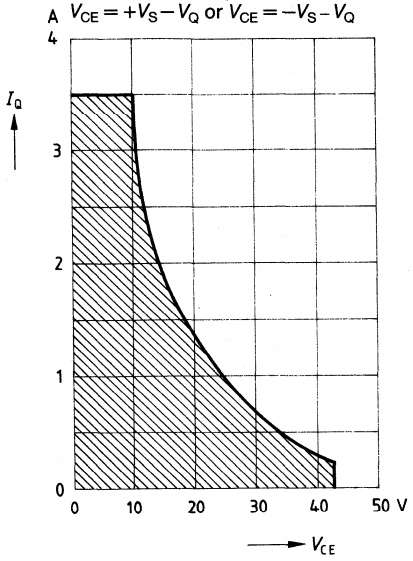


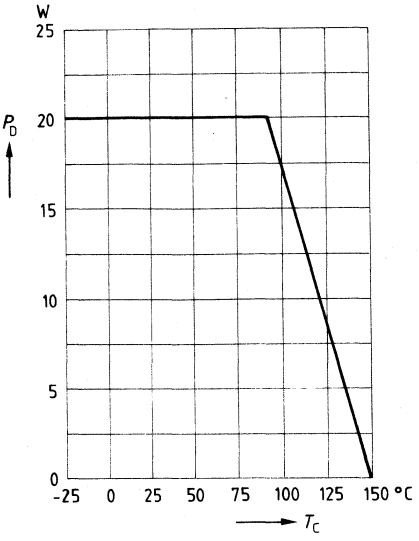
Figure 9
Slew rate for inverting operation



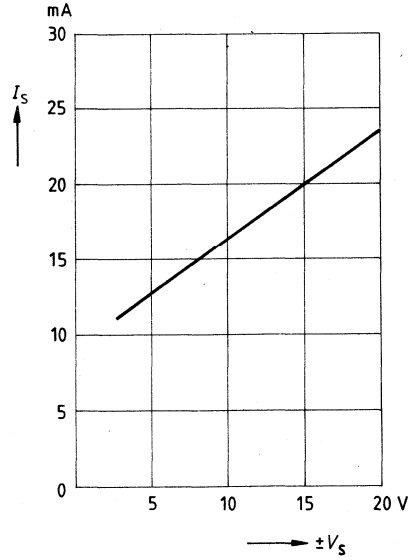
Safe operating area of output stage
Output current versus collector emitter voltage $T_C = 25\,°C$
$V_{CE} = +V_S - V_Q$ or $V_{CE} = -V_S - V_Q$



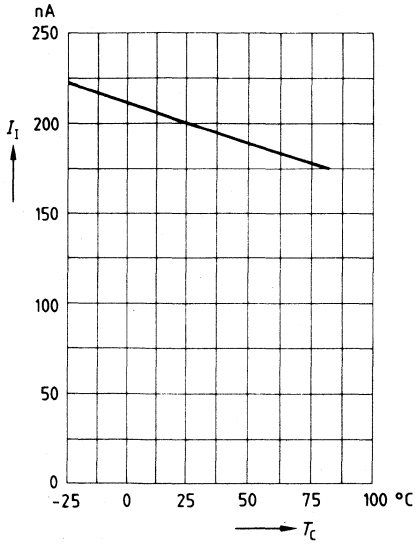
Maximum permissible power dissipation versus case temperature



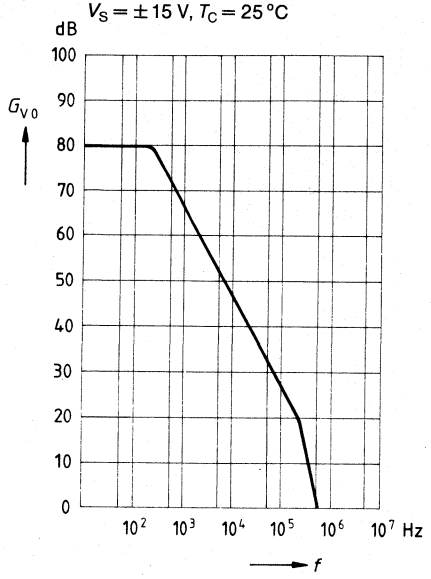
Supply current versus supply voltage
$T_C = 25\,°C$



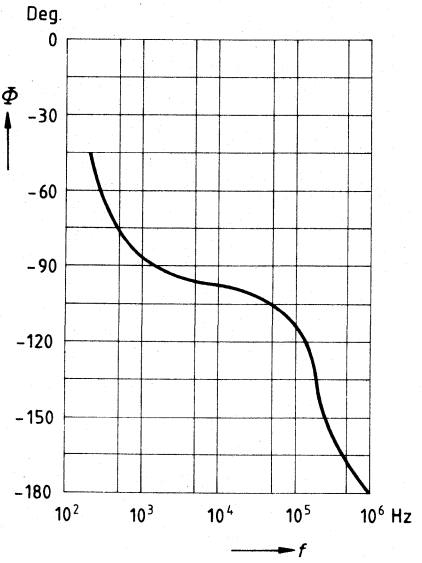
Input current versus case temperature
$V_S = \pm 15\,V$



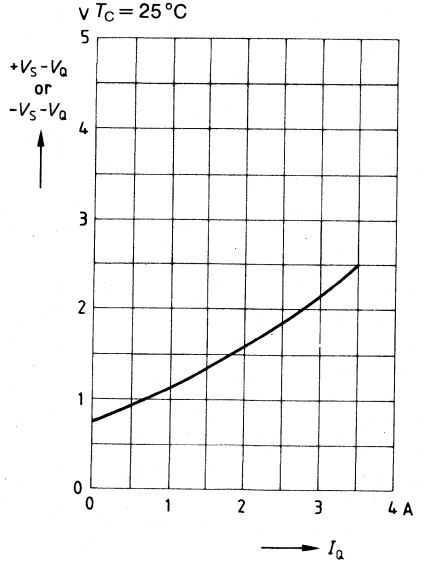
Open-loop voltage gain versus frequency
$V_S = \pm 15$ V, $T_C = 25$ °C



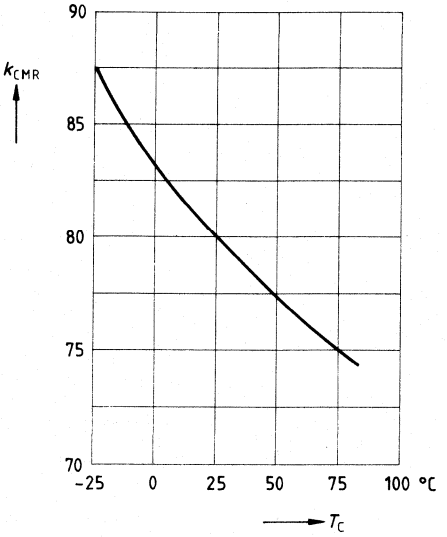
Phase response versus frequency
$V_S = \pm 15$ V, $T_C = 25$ °C



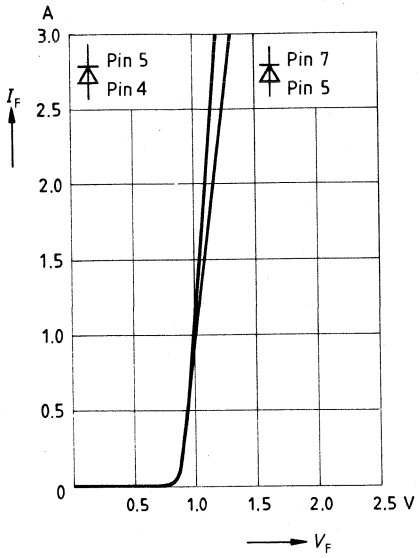
Saturation voltage versus output current
$T_C = 25$ °C



Common-mode rejection versus case temperature
$V = \pm 15$ V



Forward current versus forward voltage
$T_C = 25\,°C$



Preliminary Data **Bipolar IC**

Type	Ordering Code	Package
S TCA 1365 B	Q67000-A8190	Plastic power package P-T66-7-H (similar to TO-220)

The TCA 1365 B is a power op amp in a plastic power package P-T66-7. At maximum supply voltage of ±21 V it delivers a high output current of 4 A. The op amp is protected against short circuits and thermal overload.

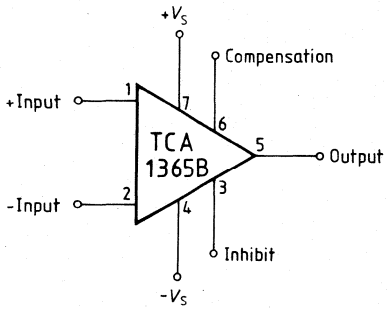
Features

- High peak output current up to 4 A
- High supply voltage up to 42 V
- Suitable up to gain of 1
- Thermal overload protection
- Internal power limiting
- External compensation
- Inhibit input (TTL-compatible)
- DC short-circuit protection to $+V_S$ and $-V_S$
- Integrated free-wheel diodes

Applications

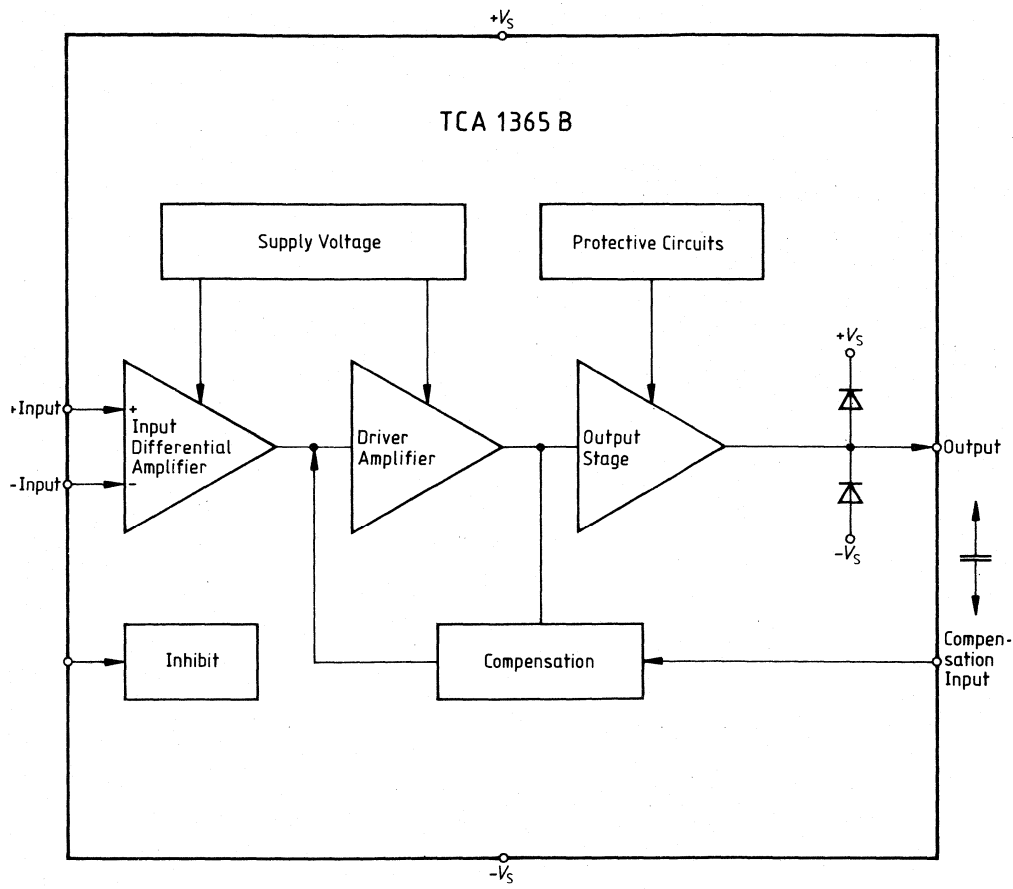
- Power comparator
- Power Schmitt-trigger
- Speed control of dc motors
- Power buffer

Pin Configuration



Pin 4 is electrically connected to cooling fin.

Block Diagram



Maximum Ratings

$T_A = -25\,°C$ to $+85\,°C$

Description	Symbol	min	max	Unit	Notes
Supply voltage	V_S	0	±21	V	
Differential input voltage	V_{ID}	$-V_S$	$+V_S$	V	
Supply current	I_S	−3.5	+4.0	A	
Output current	I_Q	−4	+4	A	
Output current	I_Q	−2		A	$V_S \geq \pm 15$ V; $V_Q < -V_S$
Output current	I_Q	−3		A	$V_S \geq \pm 10$ V; $V_Q < -V_S$
Ground current	I_{GND}	−4.0	+3.5	A	
Current Pin 3, 6	$I_{3,6}$	0	5	mA	
Power dissipation at $T_C = 85\,°C$	P_D		20	W	
Junction temperature	T_j		150	°C	
Storage temperature range	T_{stg}	−50	150	°C	

Operating Range

Supply voltage	V_S	±3	±20	V	
Case temperature	T_C	−25	85	°C	$P_D = 13$ W
Forward current of free-wheel diode	I_F		3	A	$T_{j\,max} = 125\,°C$
Thermal resistance					
system – air	$R_{th\,SA}$		65	K/W	
system – case	$R_{th\,SC}$		3	K/W	

Characteristics $V_S = \pm 15$ V, $T_C = 25$ °C

Description	Symbol	Test circuit	min	typ	max	Unit
Open-loop supply current consumption	I_S	1		20	40	mA
Input offset voltage	V_{IO}	2	−10		10	mV
Input offset current	I_{IO}	3	−100		100	nA
Input current	I_I	3		0.2	1	µA
Output voltage						
$R_L = 12\ \Omega$; $f = 1$ kHz	$V_{Q\ pp}$	4	±13.0	±13.5		V
$R_L = 4\ \Omega$; $f = 1$ kHz	$V_{Q\ pp}$		±12.5	±13.0		V
Input resistance $f = 1$ kHz	R_I	4	1	5		MΩ
Open-loop voltage gain $f = 100$ Hz	G_{VO}	5	70	80		dB
Common-mode input voltage	V_{IC}	6	+13/−15	+13.5/−15.1		V
Common-mode rejection	k_{CMR}	6	70	80		dB
Supply voltage rejection	k_{SVR}	7	−70	−80		dB
Temperature coefficient of V_{IO} $-25\ °C \le T_C \le +85\ °C$	α_{VIO}	2		50		µV/K
Temperature coefficient of I_{IO} $-25\ °C \le T_C \le +85\ °C$	α_{IIO}	3		0.4		nA/K
Slew rate of V_Q for non-inverting operation	SR	8		0.5		V/µs
Slew rate of V_Q for inverting operation	SR	9		0.5		V/µs
Noise voltage referred to input DIN 45405	V_n	1		2	5	µV
Short-circuit current						
(S1 closed)	I_{SC}	1		0,75		A
(S2 closed)	I_{SC}	1		−0.75		A
Open-loop supply current consumption (S3 open; $V_3 \ge 2$ V[1])	I_S	1		1.5	3.5	mA

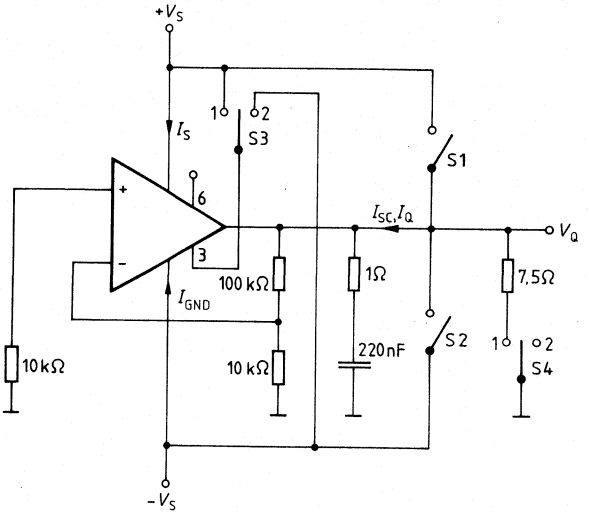
Inhibit input (pin 3)

V_3 for amp off	$V_{3\ OFF}$	1	2			V
V_3 for amp on[1])	$V_{3\ ON}$	1			0.5	V
Turn-on dead time $I_Q \ge 1$ A[2])	$t_{D\ ON}$	1		2	5	µs
Turn-off dead time $I_Q \le 1$ A[2])	$t_{D\ OFF}$	1		50	100	µs

[1]) referred to $-V_S$
[2]) S4 closed

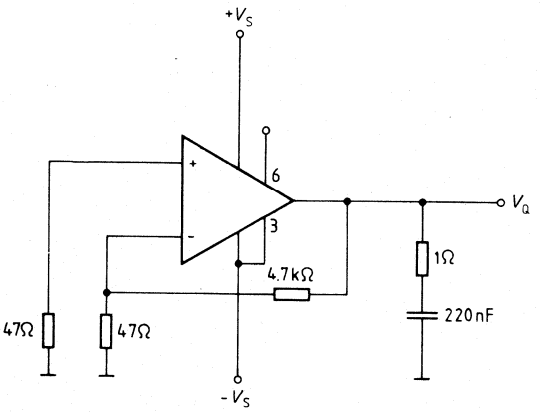
Test and Measurement Circuits

Figure 1
Open-loop supply current consumption; noise voltage



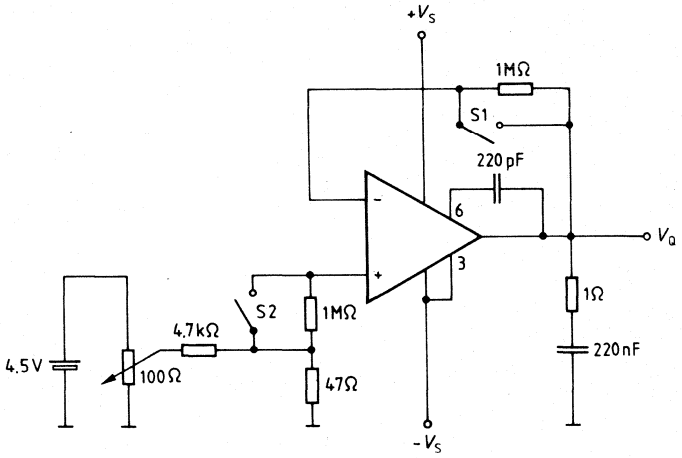
S1 to S4 as shown
unless otherwise specified

Figure 2
Input offset voltage, temperature coefficient of V_{IO}



$V_Q = 100\ V_{IO}$

Figure 3
Input offset current; input current, temperature coefficient of I_{IO}



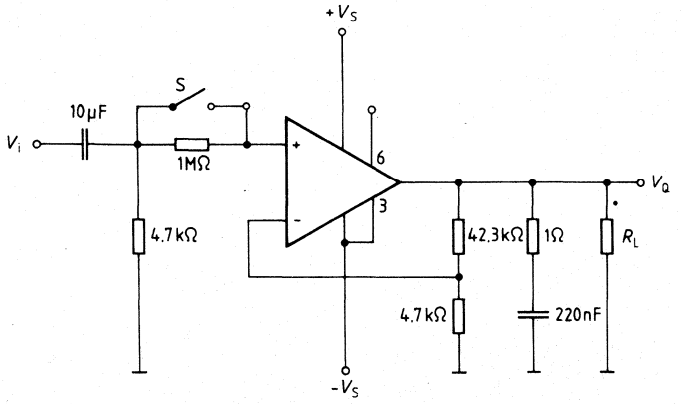
S1 open – S2 closed: $I_{I-} = \frac{V_Q}{1\,M\Omega}$

S2 open – S1 closed: $I_{I+} = \frac{V_Q}{1\,M\Omega}$

S1 open – S2 open: $I_{IO} = \frac{V_Q}{1\,M\Omega}$

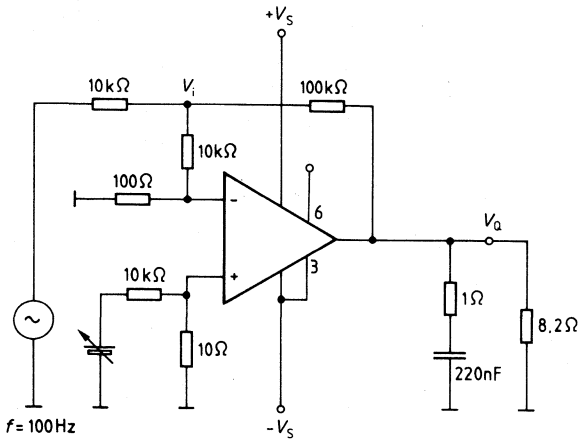
S1 closed – S2 closed: offset alignment

Figure 4
Output voltage, input resistance



S closed: to measure V_{Qpp}
S open/closed: to measure R_I

Figure 5
Open-loop voltage gain



$$G_{V0} = \left| 20 \log 101 \frac{V_Q}{V_I} \right| \text{ [dB]}$$

Figure 6
Common-mode voltage gain G_{VC}
Common-mode rejection k_{CMR} (dB) = G_{V0} (dB) − G_{VC} (dB)

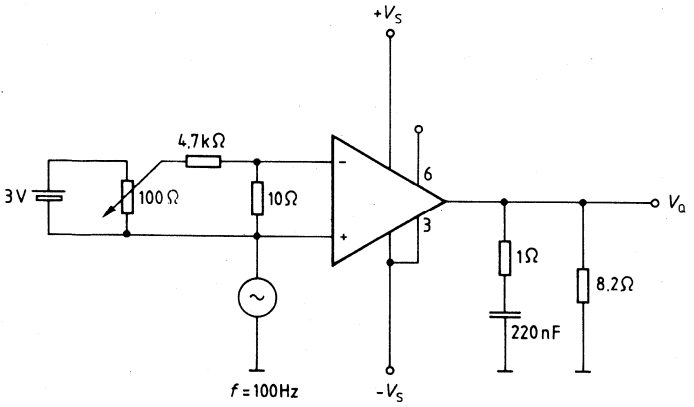
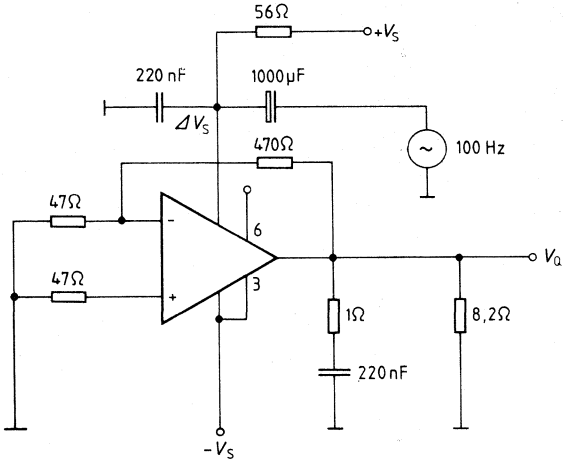


Figure 7
Supply-voltage rejection



$$k_{SVR} = 20 \log \frac{\Delta V_Q}{G_V \times \Delta V_S} \text{ [dB]}$$

Figure 8
Slew rate for non-inverting operation

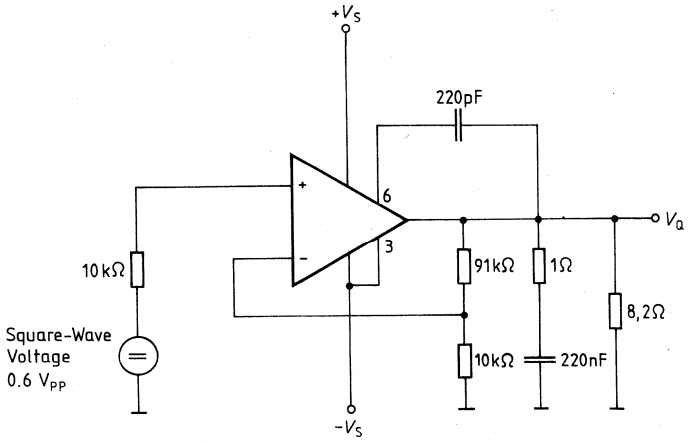
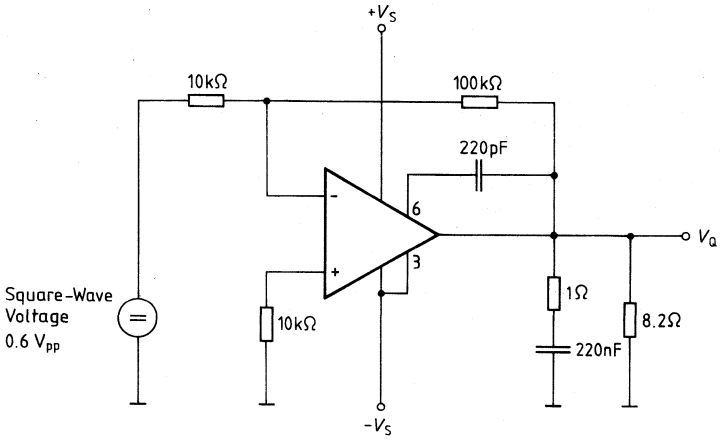
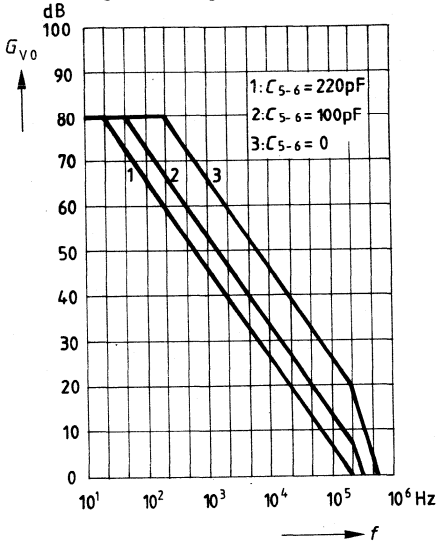


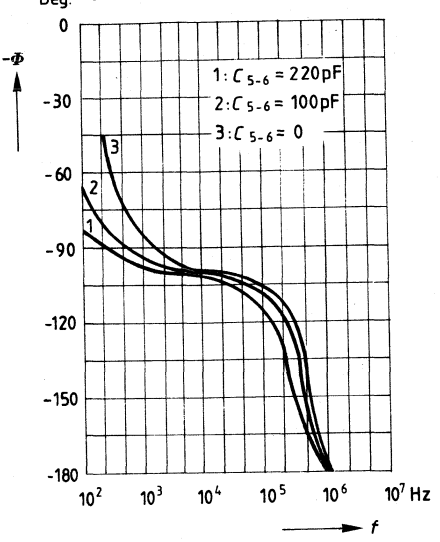
Figure 9
Slew rate for inverting operation



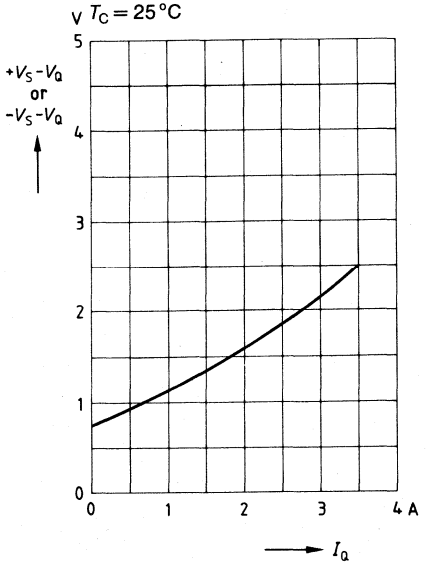
Open-loop voltage gain versus frequency
$T_C = 25\,°C$; $V_S = \pm 15$ V



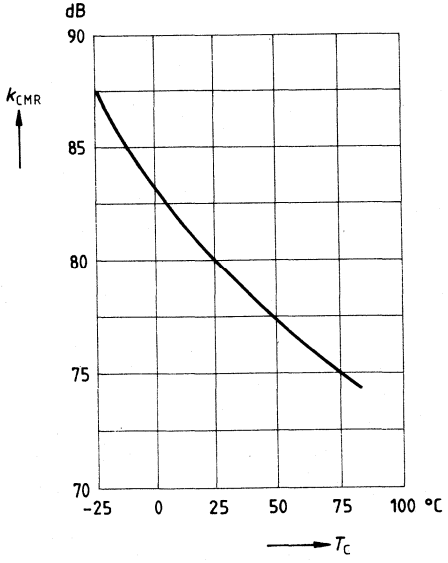
Phase response versus frequency
$T_C = 25\,°C$; $V_S = \pm 15$ V



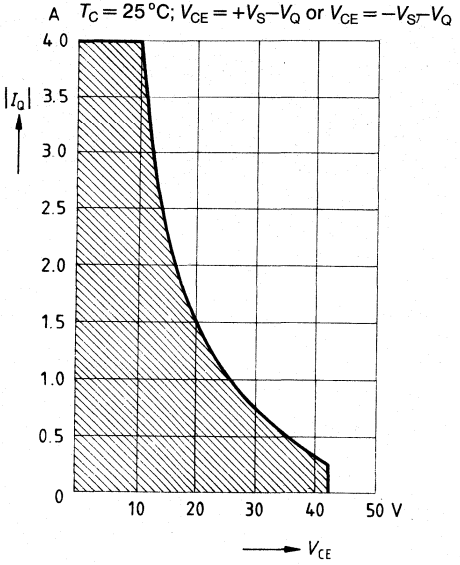
Saturation voltage versus output current
$T_C = 25\,°C$



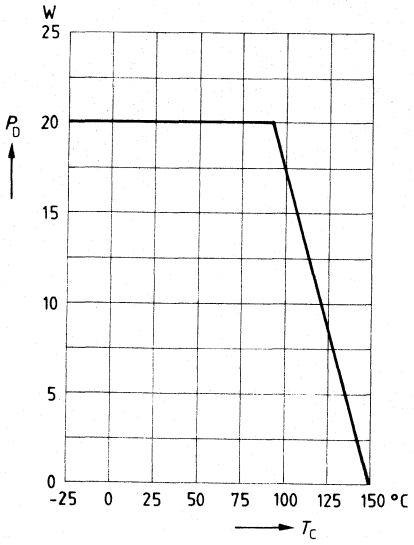
Common-mode rejection versus case temperature



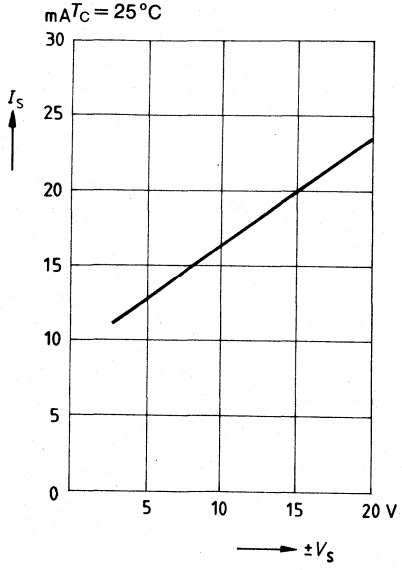
Safe operating area of output stage
Output current versus collector emitter voltage



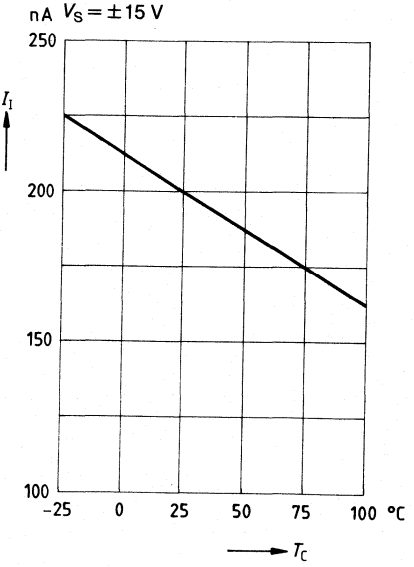
Maximum permissible power dissipation versus case temperature



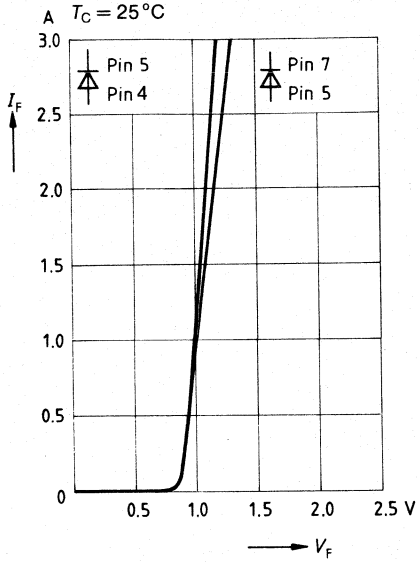
Supply current versus supply voltage



Input current versus case temperature



Forward current versus forward voltage



Bipolar IC

Type	Ordering Code	Package
TCA 2365	Q67000-A1876	P-SIP-9
TCA 2365 A	Q67000-A8017	P-DIP-18-L9

The TCA 2365 is a dual power op amp in a P-SIP-9 or P-DIP-18L9 package. The IC contains two identical op amps, each supplying a high output current of 2.5 A at supply voltages between ±4 V and ±15 V. Both amplifiers can be disconnected simultaneously (tristate; $Z_Q \approx 4$ kΩ) via an inhibit input. Integrated protective circuits protect the outputs against short circuit to $+V_S$ and $-V_S$ and prevent a thermal overloading of the IC.

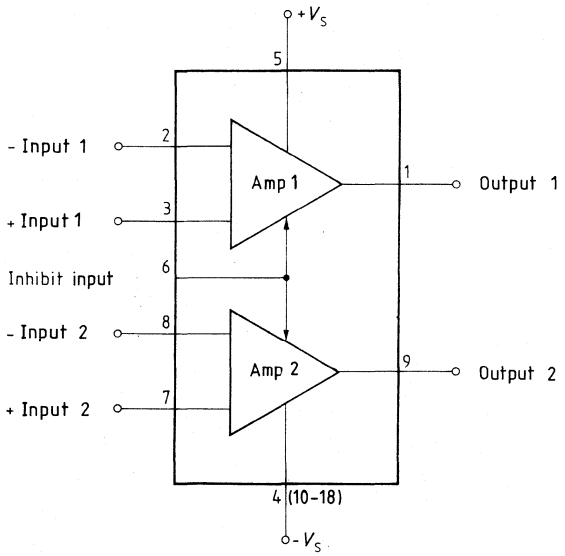
Features

- High output current of twice 2.5 A
- Wide supply voltage range, 8 V to 32 V
- High slew rate 4 V/µs
- Outputs entirely protected (dc short-circuit proof)
- Thermal overload protection
- Inhibit input enables "tristate" outputs

Applications

- Power comparator
- Power Schmitt trigger
- Speed control of dc motors

Pin Configuration TCA 2365 (TCA 2365 A)



Pin 4 is electrically connected to cooling fin.
(Establish external connection between pin 4 and pin 10-18)

Maximum Ratings

Description	Symbol	TCA 2365	TCA 2365 A	Unit
Supply voltage	V_S	±16	±16	V
$t = 50$ ms	V_S	±18	±18	V
Differential input voltage	V_{ID}	$\pm V_S$	$\pm V_S$	V
Output voltage range	V_Q	$-V_S-1$ to $+V_S+1$		V
Peak output current	I_Q	±2.5	±2.5	A
Supply current	I_S	5.5	5.5	A
Junction temperature	T_j	150	150	°C
Storage temperature range	T_{stg}	−55 to 150	−55 to 150	°C
Thermal resistance				
system – air	$R_{th\ SA}$	65	60	K/W
system – case	$R_{th\ SC}$	6	10	K/W

Operating Range

Supply voltage	V_S	±4 to ±15	±4 to ±15	V
Case temperature $P_{tot} = 10.0$ W	T_C	−25 to 85	−25 to 85	°C
Voltage gain	$G_{V\ min}$	10	10	dB

Characteristics

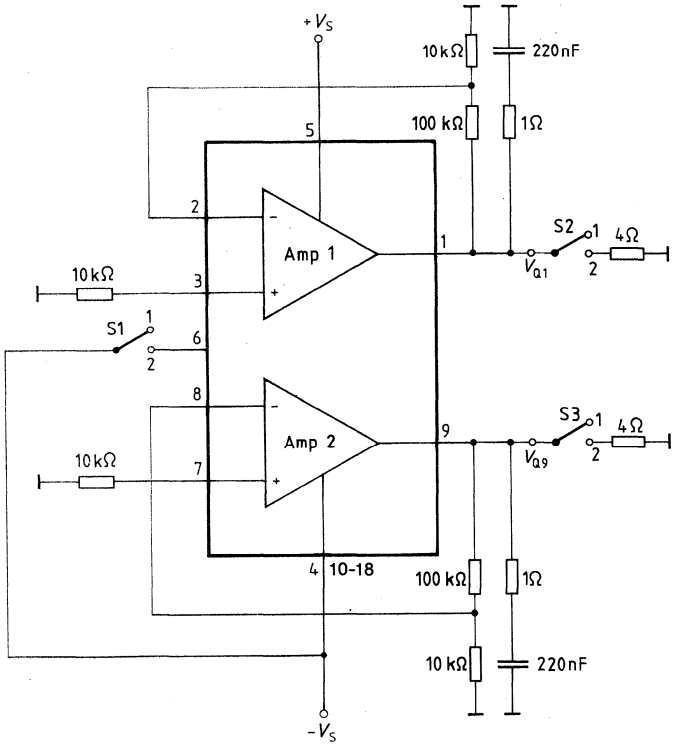
$V_S = \pm 10$ V; $T_C = 25$ °C

Description	Symbol	Test circuit	min	typ	max	Unit
Open-loop supply current consumption						
S1 in position 1	I_S	1		30	50	mA
S1 in position 2	I_{SM}	1		5	8	mA
Input offset voltage	V_{IO}	2	−10		10	mV
Input offset current	I_{IO}	3	−100		100	nA
Input current	I_I	3		0.25	1	µA
Output voltage						
($R_L = 12\ \Omega$; $f = 1$ kHz)	$V_{Q\ pp}$	4	±8.5	±9.0		V
($R_L = 4\ \Omega$; $f = 1$ kHz)	$V_{Q\ pp}$	4	±8.0	±8.5		V
($R_L = 470\ \Omega$; $f = 50$ kHz)	$V_{Q\ pp}$	4		±6.0		V
Input resistance ($f = 1$ kHz)	R_I	4	1	5		MΩ
Open-loop voltage gain ($f = 100$ Hz)	G_{V0}	5	70	80		dB
Common-mode input voltage range	V_{IC}	6	+7/−10	+7.5/−10.5		V
Common-mode rejection	k_{CMR}	6	70	80		dB
Supply voltage rejection	k_{SVR}	7	70	80		dB
Temperature coefficient of V_{IO} $-25\ °C \leq T_C \leq +85\ °C$	α_{VIO}	2		50		µV/K
Temperature coefficient of I_{IO} $-25\ °C \leq T_C \leq +85\ °C$	α_{IIO}	3		0.4		nA/K
Slew rate of V_q for non-inverting operation[1])	SR	8		4		V/µs
Slew rate of V_q for inverting operation[1])	SR	9		4		V/µs
Noise voltage referred to input	V_n	1		3		µV
Inhibit input (referred to $-V_S$)						
V_6 for IC turned off	$V_{6\ OFF}$	1	0		1.0	V
V_6 for IC turned on	$V_{6\ ON}$	1	3.0		6	V
Turn-on time $\lvert I_{1;9} \rvert > 1$ A	$t_{D\ ON}$	1		2	5	µs
Turn-off time $\lvert I_{1;9} \rvert < 1$ A (referred to $V_{6\ OFF/ON}$)	$t_{D\ OFF}$	1		15	30	µs
S2 and S3 in position 2						

[1]) For the relationship between power bandwidth and slew rate refer to **"General Information"**

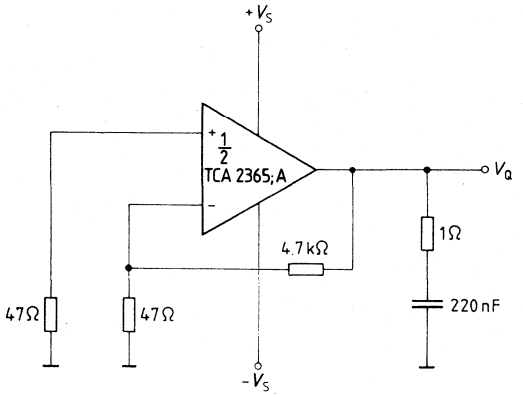
Test Circuits

Figure 1
Open-loop supply current consumption, noise voltage, turn-off voltage



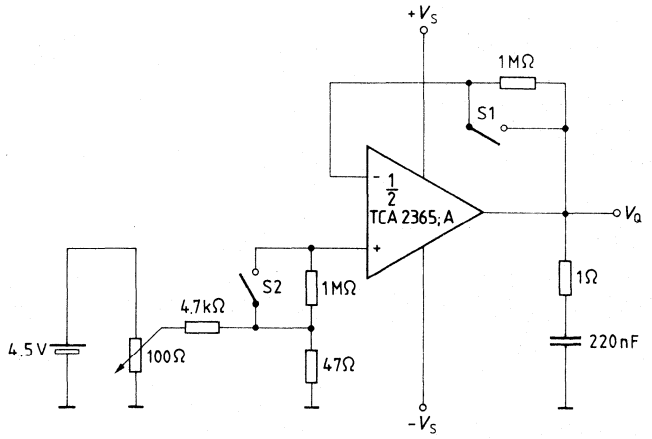
Switch as drawn unless otherwise specified

Figure 2
Input offset voltage, temperature coefficient of V_{IO}



$V_Q = 100 \times V_{IO}$

Figure 3
Input offset current, input current, temperature coefficient of I_{IO}



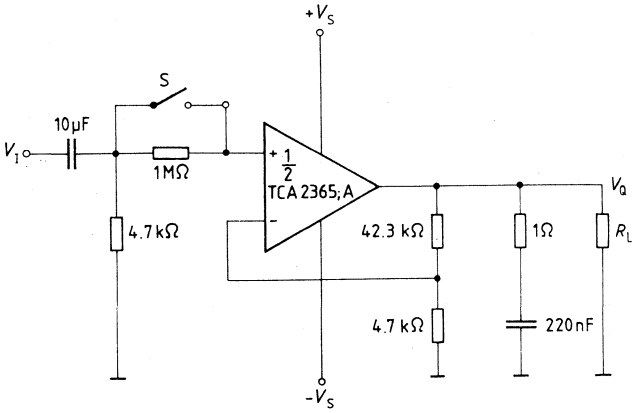
S1 open – S2 closed: $I_{I-} = \frac{V_Q}{1\ M\Omega}$

S2 open – S1 closed: $I_{I+} = \frac{V_Q}{1\ M\Omega}$

S1 open – S2 open: $I_{IO} = \frac{V_Q}{1\ M\Omega}$

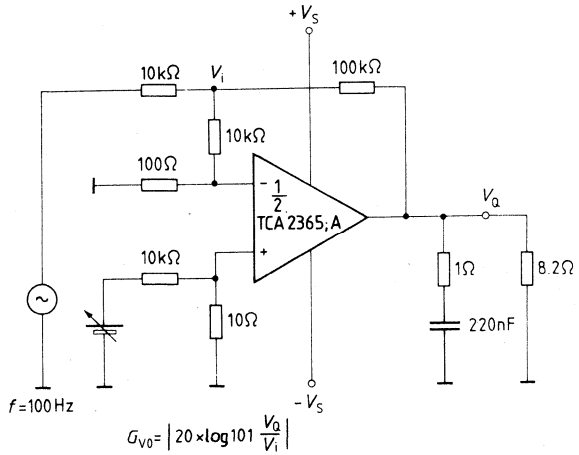
S1 closed – S2 closed: offset alignment

Figure 4
Output voltage, input resistance



S closed : to measure V_{Qpp}
S open / closed : to measure R_I

Figure 5
Open-loop voltage gain



$$G_{V0} = \left| 20 \times \log 101 \frac{V_Q}{V_i} \right|$$

Figure 6
Common mode voltage gain G_{VC}
Common mode rejection k_{CMR} (dB) = G_{V0} (dB) − G_{VC} (dB)

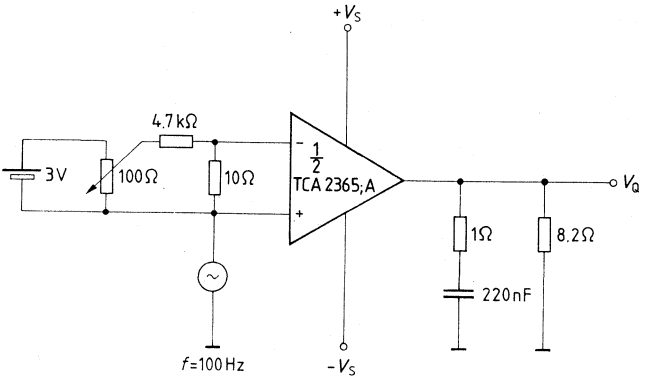
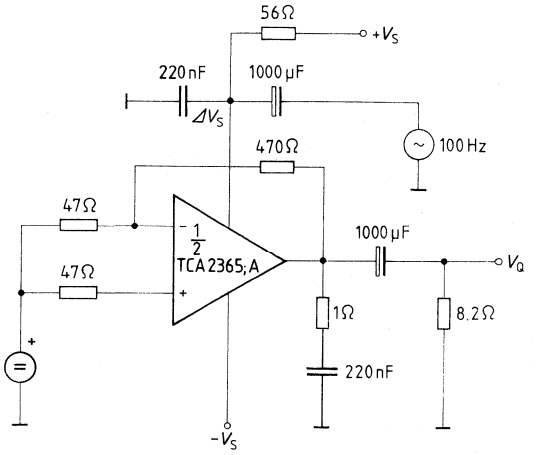


Figure 7
Supply voltage rejection



$$k_{SVR} = 20\log \frac{\Delta V_Q}{G_V \cdot \Delta V_S} \text{ [dB]}$$

Figure 8
Slew rate for non-inverting operation

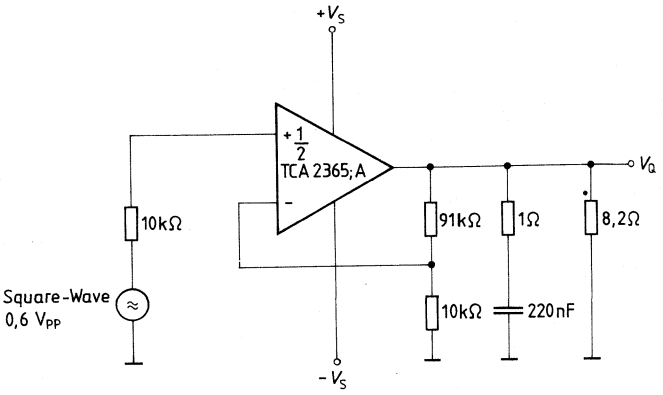
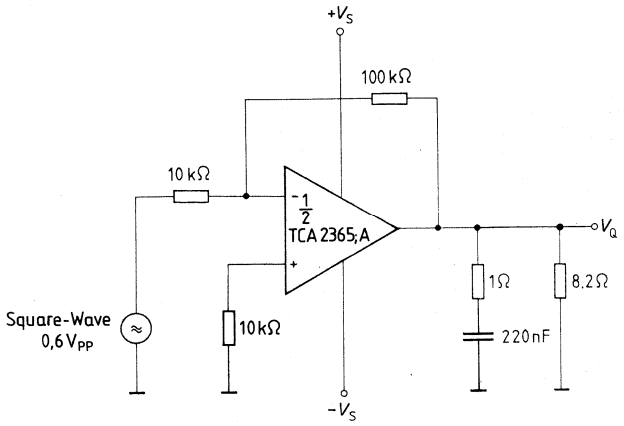
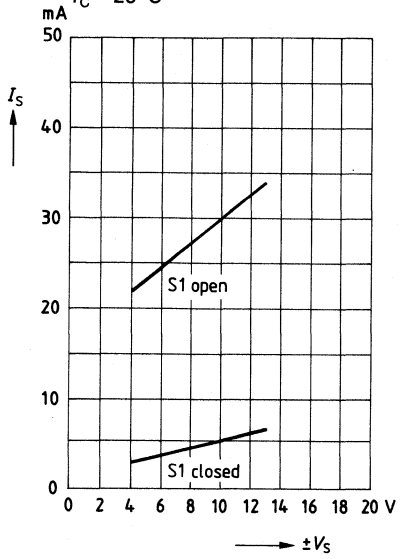


Figure 9
Slew rate for inverting operation

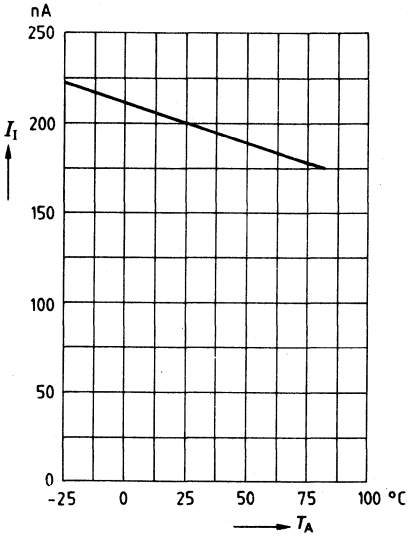


Supply current I_S and I_{SM} versus supply voltage

$T_C = 25\,°C$

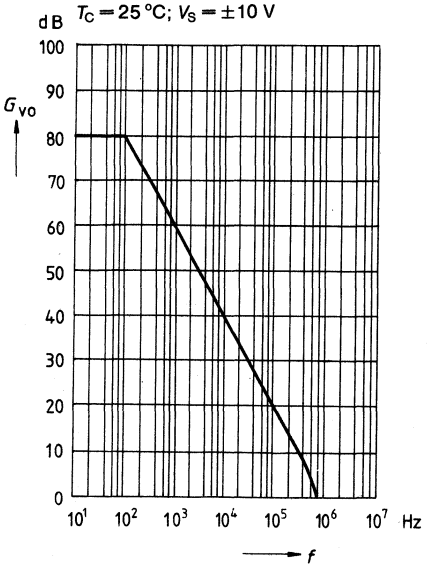


Input current versus ambient temperature

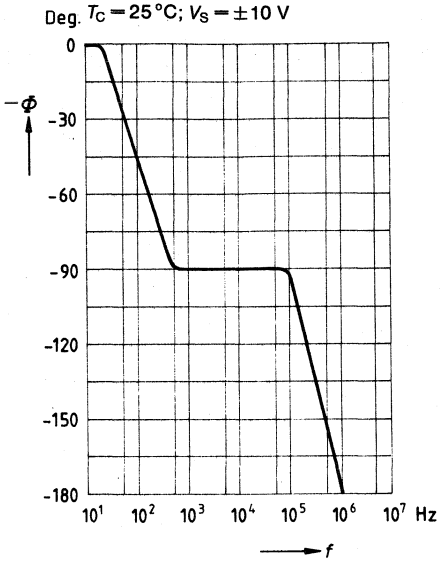


Open-loop voltage gain versus frequency

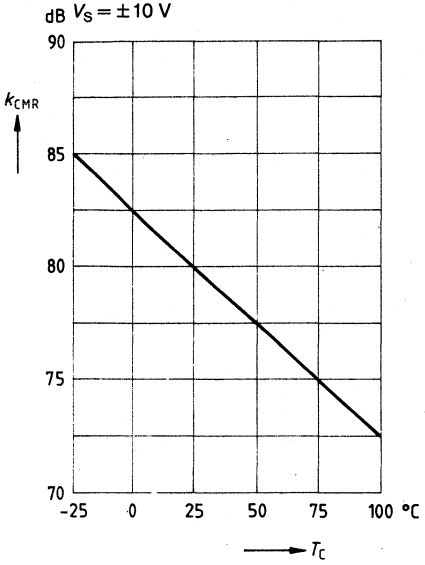
$T_C = 25\,°C$; $V_S = \pm 10$ V



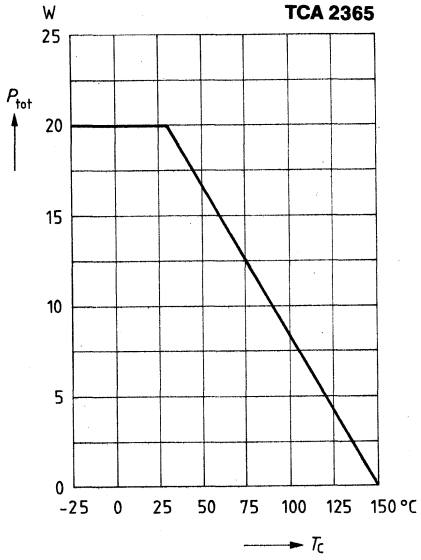
Phase response versus frequency



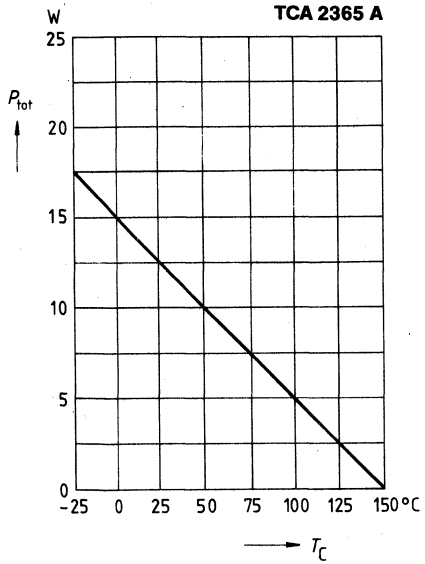
Common-mode rejection versus case temperature



Max. permissible power dissipation versus case temperature



Max. permissible power dissipation versus case temperature



Preliminary Data **Bipolar IC**

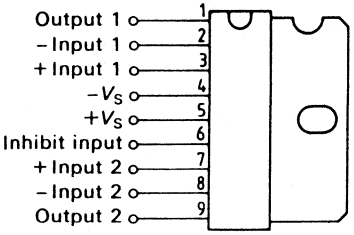
Type	Ordering Code	Package
TCA 2465	Q67000-A8109	P-SIP-9

The TCA 2465 is a dual power op amp in a P-SIP-9 package. The IC contains two identical op amps, each supplying a high output current of 2.5 A at supply voltages between ±3 V and ±20 V. Both amplifiers can be disconnected at $V_6 \geq 2$ V via an inhibit input. The same applies to an open pin 6. Integrated protective circuits protect the outputs against short-circuit to $+V_S$ and $-V_S$ and prevent thermal overloading of the IC.

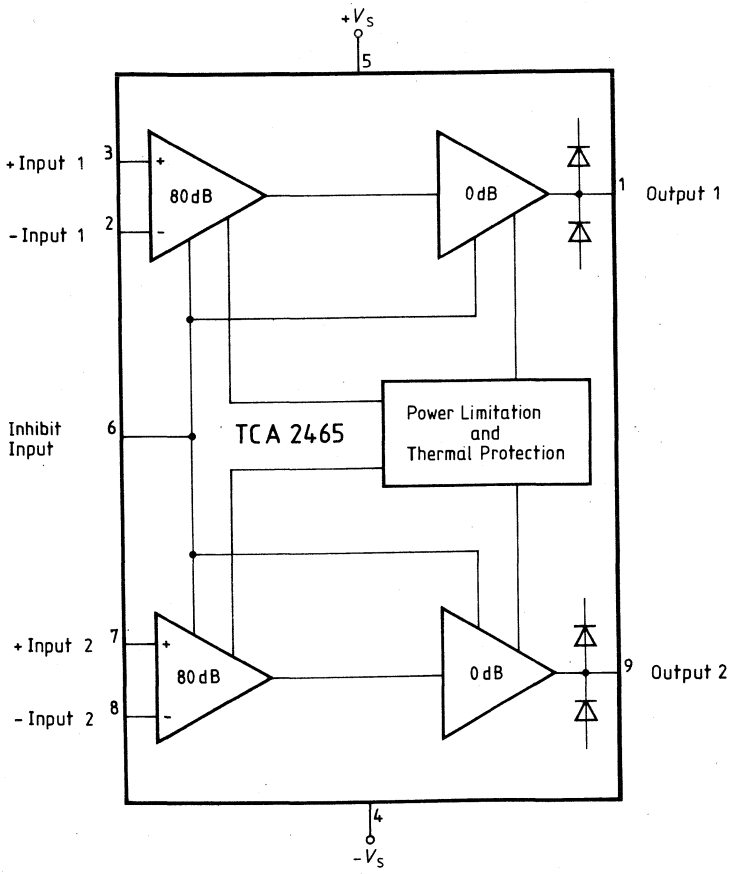
Features

- High output current of twice 2.5 A
- Large supply voltage range up to 42 V
- High slew rate of 2 V/µs
- Outputs fully protected (dc short-circuit proof)
- Thermal overload protection
- Inhibit input enables "tristate" outputs
- Integrated free-wheel diodes

Pin Configuration



Block Diagram



Maximum Ratings

$T_C = -40\,°C$ to $+85\,°C$

Description	Symbol	min	max	Unit	Notes
Supply voltage	V_S		± 21	V	
Differential input voltage	V_{ID}		$(-V_S) + (+V_S)$	V	$\Delta V_{2\text{-}3}$ or $\Delta V_{8\text{-}7}$
Output current	I_Q	-2.5	2.5	A	I_1 or I_9
Output current	I_Q	-1.5		A	$V_S \geq \pm 15$ V; $V_Q < -V_S$
Supply current	I_S	-5	5.5	A	I_S
Ground current	I_{GND}	-5.5	5	A	I_4
Input voltage	V_I	$-V_S$	$+V_S$	V	V_2, V_3, V_7, V_8
Inhibit input	V_6	$-V_S$	$+V_S$	V	
Junction temperature	T_j		150	°C	
Storage temperature range	T_{stg}	-50	150	°C	

Operating Range

Supply voltage	V_S	± 3	± 20	V	
Case temperature	T_C	-40	85	°C	$P_D = 12$ W
Voltage gain	$G_{V\,min}$	20		dB	
Thermal resistance					
system – air	$R_{th\,SA}$		60	K/W	
system – case	$R_{th\,SC}$		5	K/W	

Characteristics

$V_S = \pm 10$ V; $T_C = 25$ °C

Description	Symbol	Test circuit	min	typ	max	Unit
Open-loop supply current consumption S1 in position 1 and 2	I_S	1		30	50	mA
Input offset voltage	V_{IO}	2	−10		10	mV
Input offset current Input current	I_{IO} I_I	3 3	−100		100 1	nA µA
Output voltage R_L = 12 Ω; f = 1 kHz R_L = 4 Ω; f = 1 kHz R_L = 470 Ω; f = 40 kHz	 $V_{Q\,pp}$ $V_{Q\,pp}$ $V_{Q\,pp}$	 4 4 4	 ±8.5 ±8.0	 ±9.0 ±8.5 ±8.0		 V V V
Input resistance f = 1 kHz	I	4	1	5		MΩ
Open-loop voltage gain f = 100 Hz)	G_{V0}	5	70	80		dB
Common-mode input voltage range	V_{IC}	6	+7/−10	+7.5/−10.5		V
Common-mode rejection Supply voltage rejection	k_{CMR} k_{SVR}	6 7	70 −70	80 −80		dB dB
Temperature coefficient of V_{IO} −40 °C ≤ T_C ≤ +85 °C Temperature coefficient of I_{IO} −40 °C ≤ T_C ≤ +85 °C	α_{VIO} α_{IIO}	2 3		50 0.4		µV/K nA/K
Slew rate of V_Q for non-inverting operation Slew rate of V_Q for inverting operation	SR SR	8 9		2 2		V/µs V/µs
Noise voltage (DIN 45405, referred to input)	V_n	1		3		µV
Inhibit input (referred to $-V_S$) V_6 for IC turned off V_6 for IC turned on	 $V_{6\,OFF}$ $V_{6\,ON}$	 1 1	 2.0		 0.8	 V V
H input current, V_6 = 5 V[1]) L input current, V_6 = 0 V[1])	I_{6H} I_{6L}	1 1		0.1 0.5	0.5 3.0	µA µA
Turn-on dead time $\lvert I_{1;9} \rvert > A^2$) Turn-off dead time $\lvert I_{1;9} \rvert < 1\ A^2$) } referred to $V_{6\,OFF/ON}$	$t_{D\,ON}$ $t_{D\,OFF}$	1 1		10 10	20 20	µs µs
Short-circuit current (switch S3 closed) Short-circuit current (switch S4 closed)	I_{SC} I_{SC}	1 1		1 1		A A

[1]) referred to $-V_S$
[2]) Switch S2 closed

Test Circuits

Figure 1
Open-loop supply current consumption; noise voltage

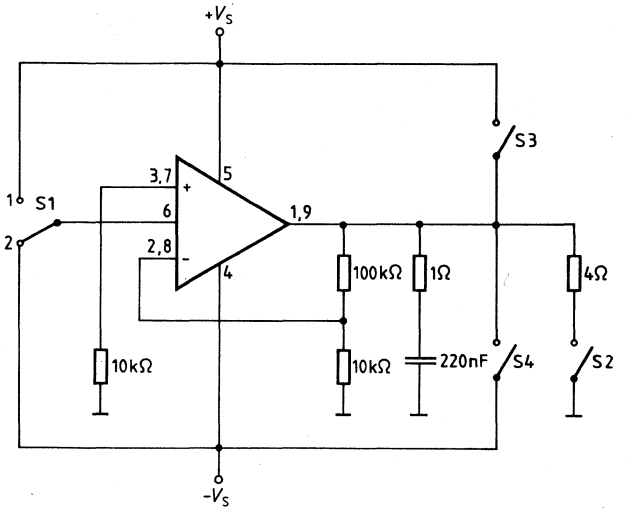


Figure 2
Input offset voltage; temperature coefficient of V_{IO}

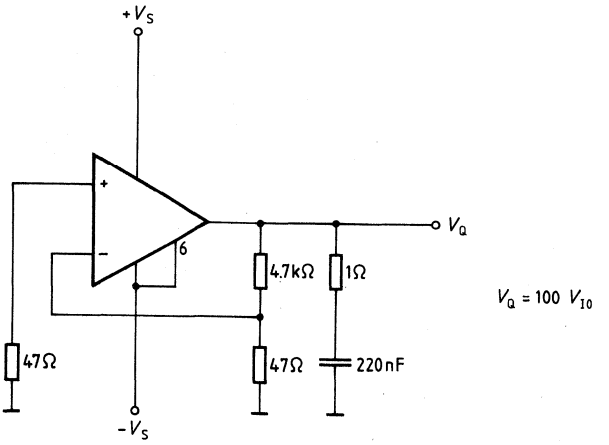
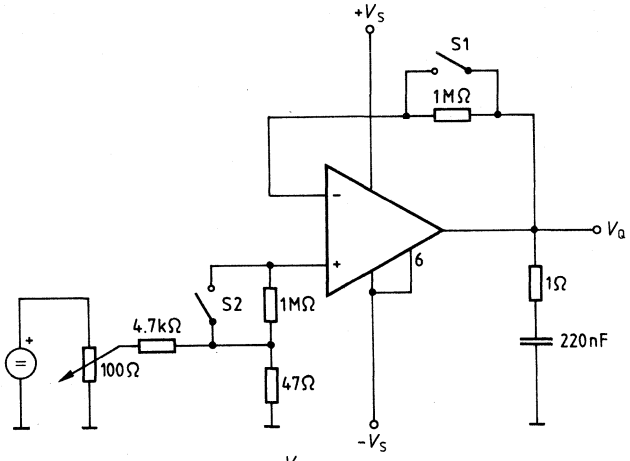


Figure 3
Input offset current; input current; temperature coefficient of I_{IO}



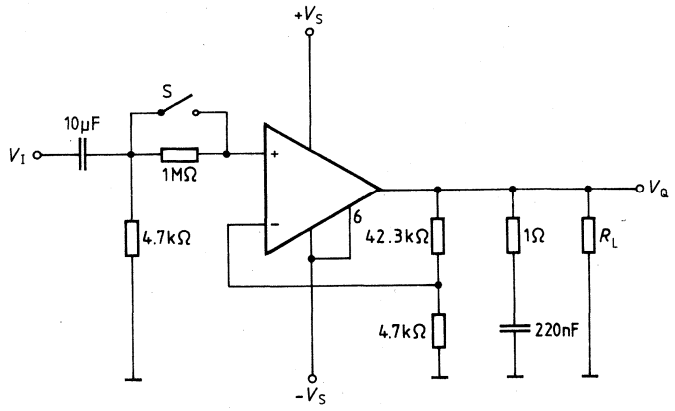
S1 open - S2 closed : $I_{I-} = \frac{V_Q}{1M\Omega}$

S2 open - S1 closed : $I_{I+} = \frac{V_Q}{1M\Omega}$

S1 open - S2 open : $I_{IO} = \frac{V_Q}{1M\Omega}$

S1 closed - S2 closed : offset adjustment

Figure 4
Output voltage; input resistance



S closed : to measure V_{Qpp}
S open / closed : to measure R_I

Figure 5
Open-loop voltage gain G_{V0}

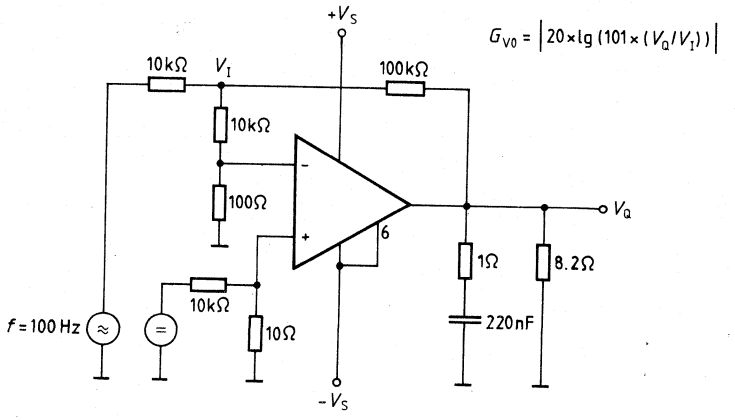


Figure 6
Open-loop voltage gain G_{VC}
common-mode rejection k_{CMR} (dB) = G_{V0} (dB) − G_{VC} (dB)

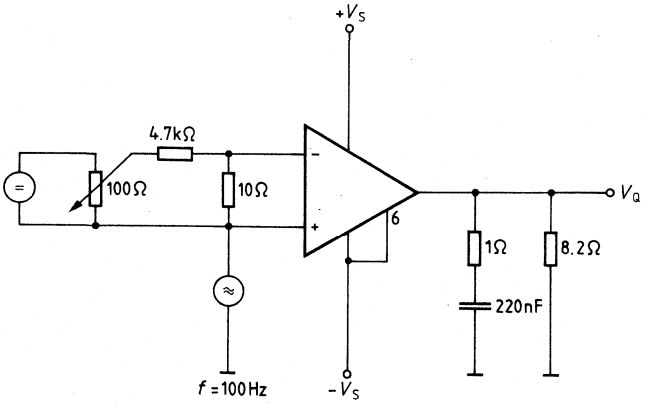


Figure 7
Supply voltage rejection k_{SVR}

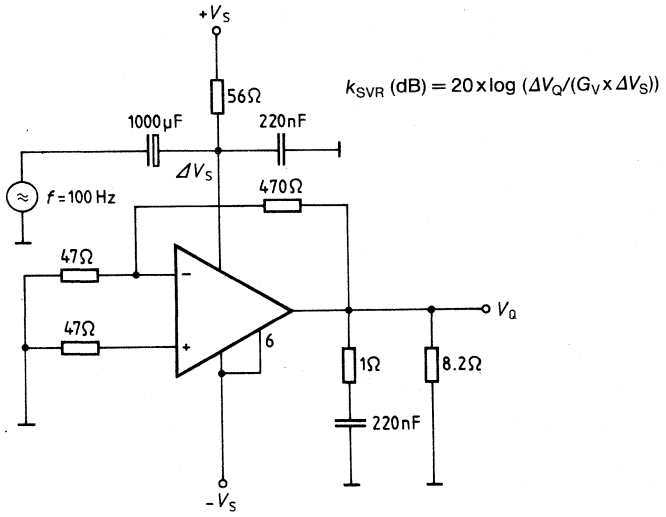


Figure 8
Slew rate for non-inverting operation

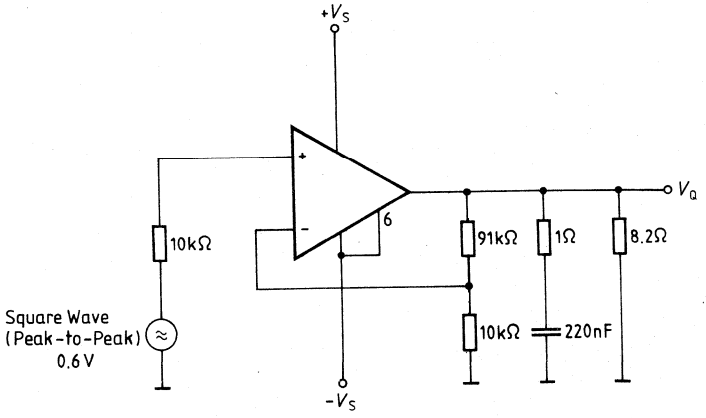
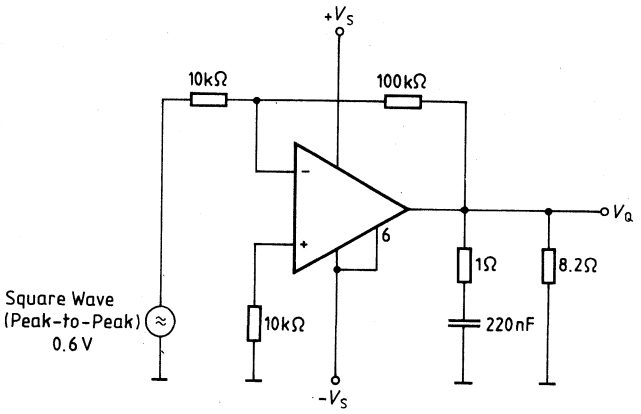


Figure 9
Slew rate for inverting operation



Application Circuits

Figure 10
Non-inverting operation; $G_V = 5$

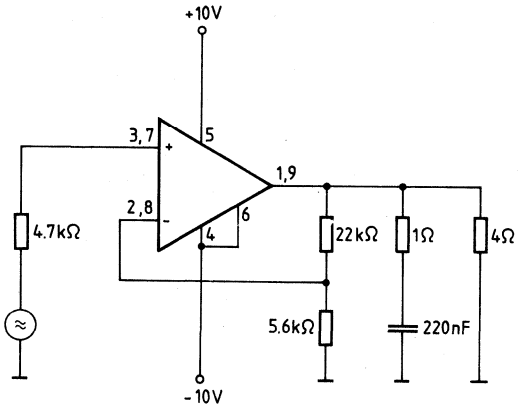
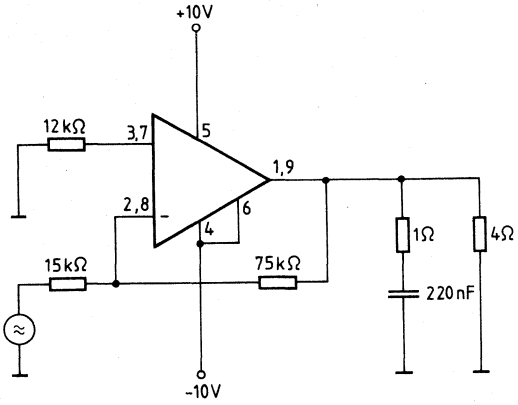
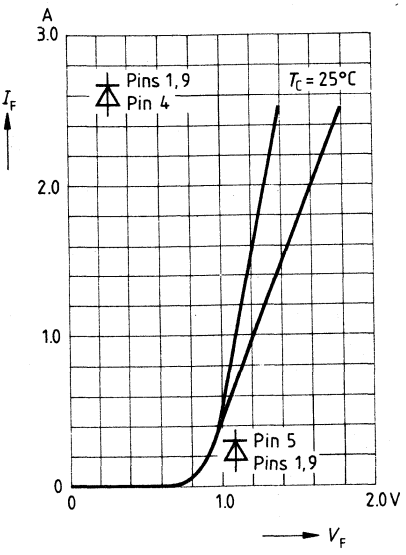


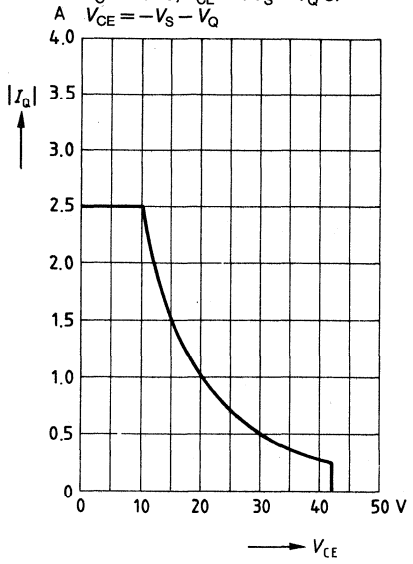
Figure 11
Inverting operation; $G_V = -5$



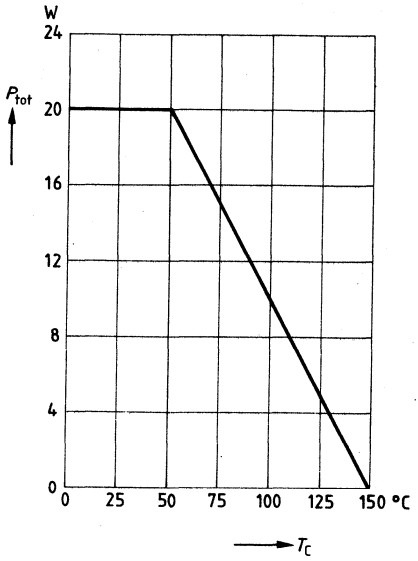
Forward current versus forward voltage



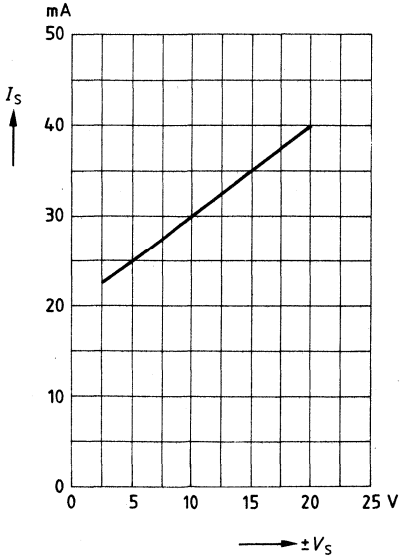
Safe operating area (SOA)
Peak output current versus collector-emitter voltage
$T_C = 25\,°C$, $V_{CE} = +V_S - V_Q$ or $V_{CE} = -V_S - V_Q$



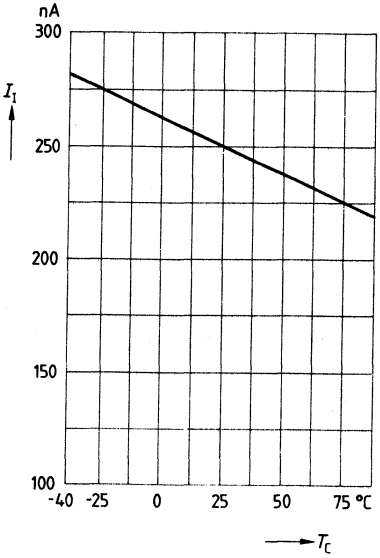
Max. permissible power dissipation versus case temperature



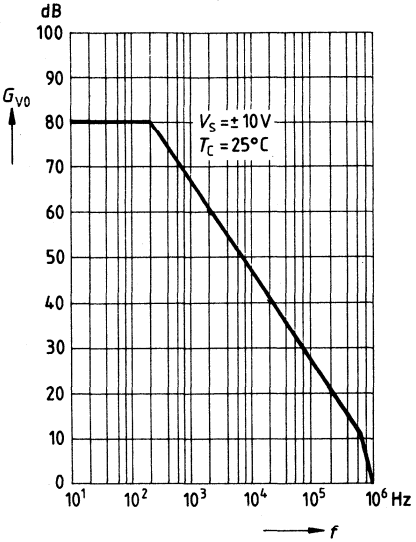
Supply current versus supply voltage
$T_C = 25\,°C$



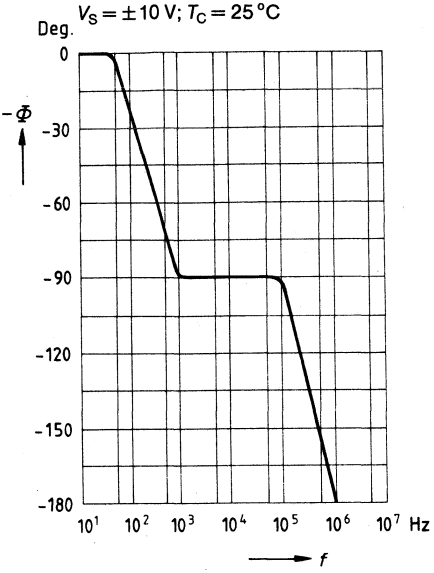
Input current versus case temperature
$V_S = \pm 10\,V$



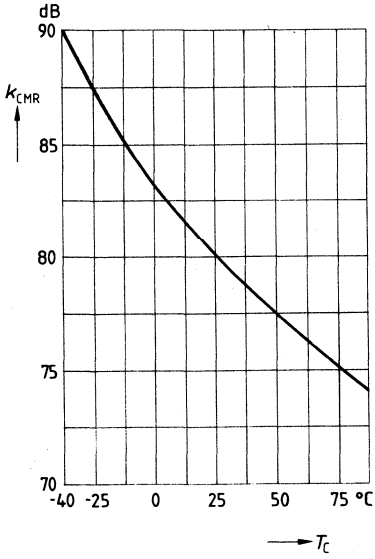
Open-loop voltage gain versus frequency



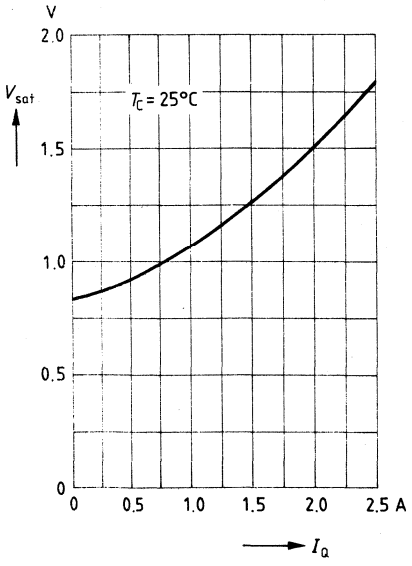
Phase response versus frequency
$V_S = \pm 10$ V; $T_C = 25$ °C



Common-mode rejection versus case temperature
$V_S = \pm 10$ V



Saturation voltage versus peak output current
$T_C = 25$ °C



Preliminary Data **Bipolar IC**

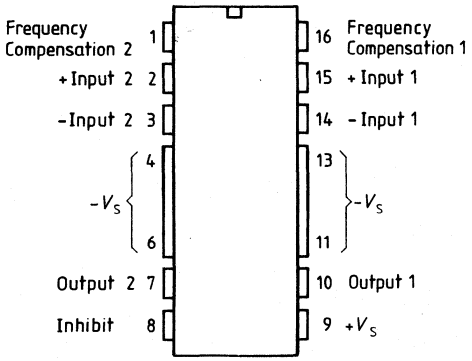
Type	Ordering Code	Package
TCA 2465 A	Q67000-A8110	P-DIP-16

The TCA 2465A is a dual power op amp in a P-DIP-16 package. The IC contains two identical op amps, each supplying a high output current of 2.5 A at supply voltages between ±3 V and ±20 V. Internal compensation permits negative feedback of the amplifiers up to a min. of 20 dB. If a voltage gain of 0 to 20 dB is required, the TCA 2465 A can be compensated with external capacitors from pin 7 to 1 or pin 10 to 16. Both amplifiers can be disconnected at $V_8 \geq 2$ V via an inhibit input. Integrated protective circuits protect the outputs against short-circuit to $+V_S$ and $-V_S$ and prevent thermal overloading of the IC.

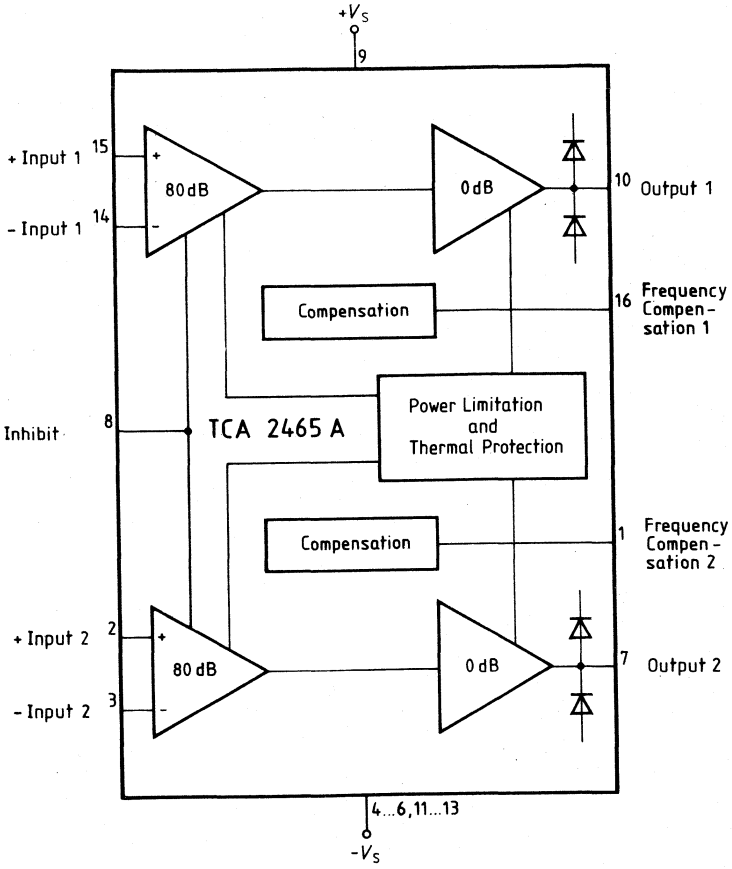
Features

- High output current of twice 2.5 A
- Large supply voltage range up to 42 V
- Outputs fully protected (dc short-circuit proof)
- Thermal overload protection
- Inhibit input enables "tristate" outputs
- Voltage gain up to 0 dB possible by external frequency compensation
- Integrated free-wheel diodes

Pin Configuration
(top view)



Block Diagram



Maximum Ratings

$T_C = -40\,°C$ to $+85\,°C$

Description	Symbol	min	max	Unit	Notes
Supply voltage	V_S		± 21	V	
Differential input voltage	V_{ID}		$(-V_S) + (V_S)$	V	$\Delta V_{2\text{-}3}$ or $\Delta V_{15\text{-}14}$
Output current	I_Q	−2.5	2.5	A	I_7 or I_{10}
Output current	I_Q	−1.5		A	$V_S \geq \pm 15$ V; $V_Q < -V_S$
Supply current	I_S	−5	5.5	A	I_9
Ground current	I_{GND}	−5.5	5	A	I_4
Input voltage	V_I	$-V_S$	$+V_S$	V	V_2, V_3, V_{14}, V_{15}
Inhibit input	V_8	$-V_S$	$+V_S$	V	
Junction temperature	T_j		150	°C	
Storage temperature range	T_{stg}	−50	150	°C	

Operating Range

Supply voltage	V_S	±3	±20	V	
Case temperature	T_C	−40	85	°C	$P_D = 5$W
Thermal resistance					
system – air	$R_{th\ SA}$		60	K/W	
system – case	$R_{th\ SC}$		12	K/W	

Characteristics

$V_S = \pm 10$ V, $T_C = 25$ °C

Description	Symbol	Test circuit	min	typ	max	Unit
Open-loop supply current consumption S1 in position 1 and 2	I_S	1		30	50	mA
Input offset voltage	V_{IO}	2	−10		10	mV
Input offset current Input current	I_{IO} I_I	3 3	−100	 0.25	100 1	nA µA
Output voltage R_L = 12 Ω; f = 1 kHz R_L = 4 Ω; f = 1 kHz R_L = 470 Ω; f = 40 kHz	 $V_{Q\ pp}$ $V_{Q\ pp}$ $V_{Q\ pp}$	 4 4 4	 ±8.5 ±8.0	 ±9.0 ±8.5 ±8.0	 V	 V V
Input resistance f = 1 kHz	R_I	4	1	5		MΩ
Open-loop voltage gain f = 100 Hz	G_{V0}	5	70	80		dB
Common-mode input voltage range	V_{IC}	6	+7/−10	+7.5/−10.5		V
Common-mode rejection Supply voltage rejection	k_{CMR} k_{SVR}	6 7	70 −70	80 −80		dB dB
Temperature coefficient of V_{IO} −40 °C ≤ T_C ≤ +85 °C Temperature coefficient of I_{IO} −40 °C ≤ T_C ≤ +85 °C	α_{VIO} α_{IIO}	2 3		50 0.4		µV/K nA/K
Slew rate of V_Q for non-inverting operation Slew rate of V_Q for inverting operation	SR SR	8 9		0.5 0.5		V/µs V/µs
Noise voltage (DIN 45405, referred to input)	V_n	1		3		µV
Inhibit input (referred to $-V_S$) V_8 for IC turned off V_8 for IC turned on	 $V_{8\ OFF}$ $V_{8\ ON}$	 1 1	 2.0	 	 0.8	 V V
H input current, V_8 = 5 V[1]) L input current, V_8 = 0 V[1])	I_{8H} I_{8L}	1 1		0.1 0.5	0.5 3.0	µA µA
Turn-on dead time $\lvert I_{7,10} \rvert > 1$ A[2]) Turn-off dead time $\lvert I_{7,10} \rvert < 1$ A[2]) } referred to $V_{8\ OFF/ON}$	$t_{D\ ON}$ $t_{D\ OFF}$	1 1		10 10	20 20	µs µs
Short-circuit current (S3 closed) Short-circuit current (S4 closed)	I_{SC} I_{SC}	1 1		1 1		A A

[1]) referred to $-V_S$
[2]) Switch S2 closed

Test Circuits

Figure 1
Open-loop supply current consumption; noise voltage

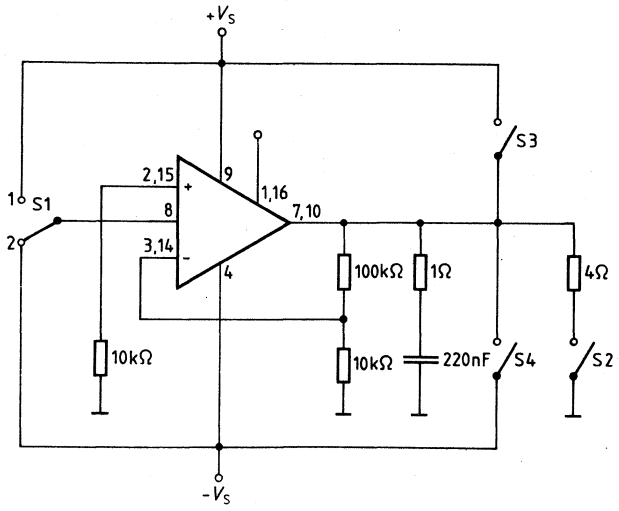
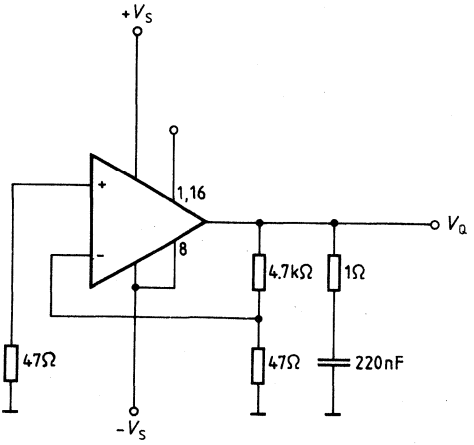
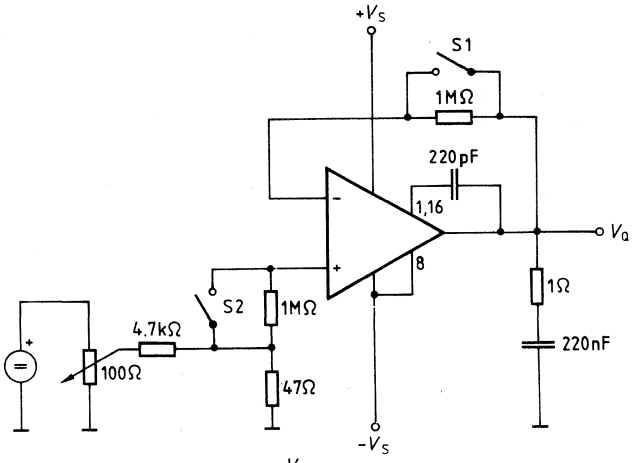


Figure 2
Input offset voltage; temperature coefficient of V_{IO}



$V_Q = 100\ V_{IO}$

Figure 3
Input offset current; input current; temperature coefficient of I_{IO}



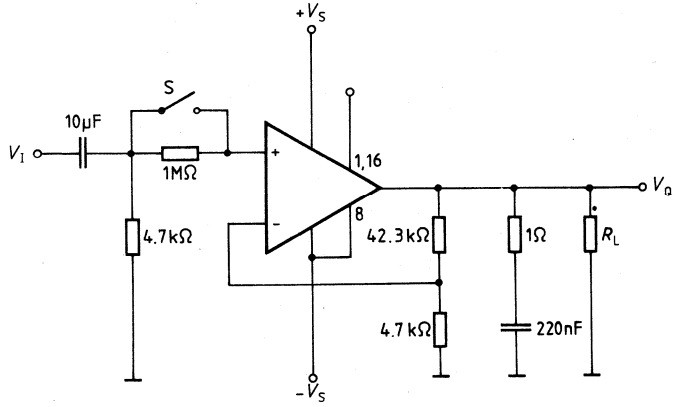
S1 open – S2 closed: $I_{I-} = \frac{V_Q}{1M\Omega}$

S2 open – S1 closed: $I_{I+} = \frac{V_Q}{1M\Omega}$

S1 open – S2 open $I_{IO} = \frac{V_Q}{1M\Omega}$

S1 closed – S2 closed: offset adjustment

Figure 4
Output voltage; input resistance



S closed: to measure V_{Qpp}
S open/closed: to measure R_I

Figure 5
Open-loop voltage gain G_{V0}

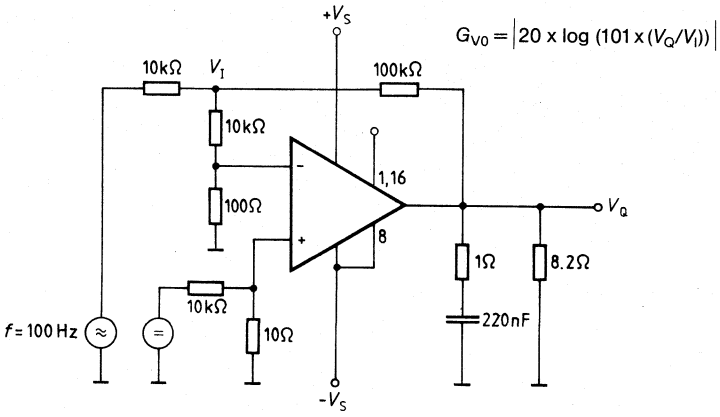


Figure 6
Open-loop voltage gain G_{VC}
Common-mode rejection k_{CMR} (dB) − G_{V0} (dB) − G_{VC} (dB)

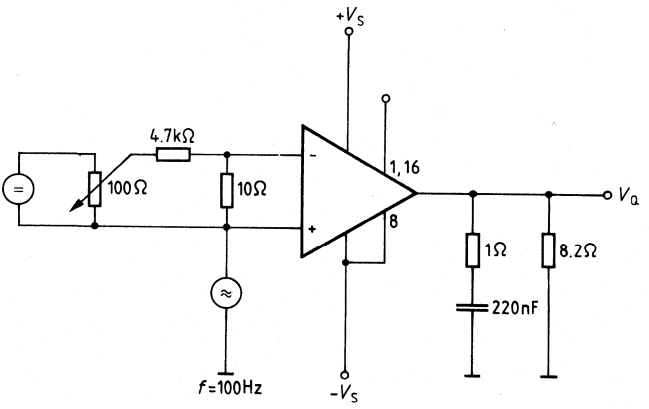


Figure 7
Supply voltage rejection k_{SVR}

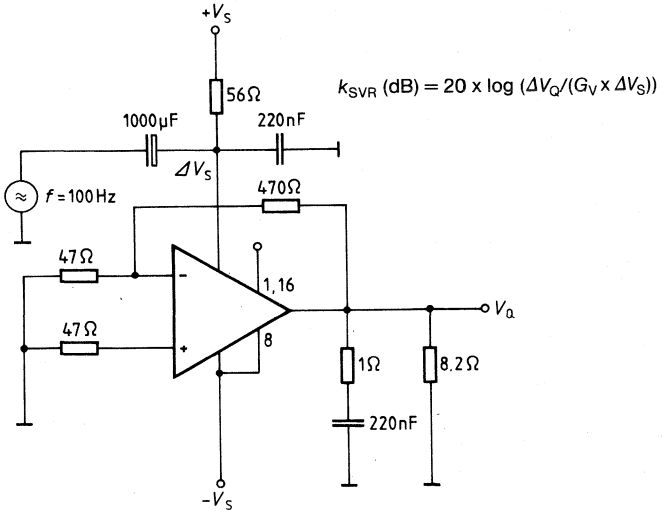


Figure 8
Slew rate for non-inverting operation

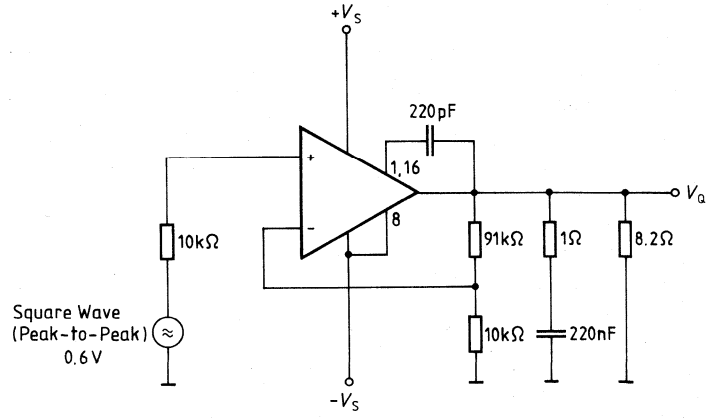
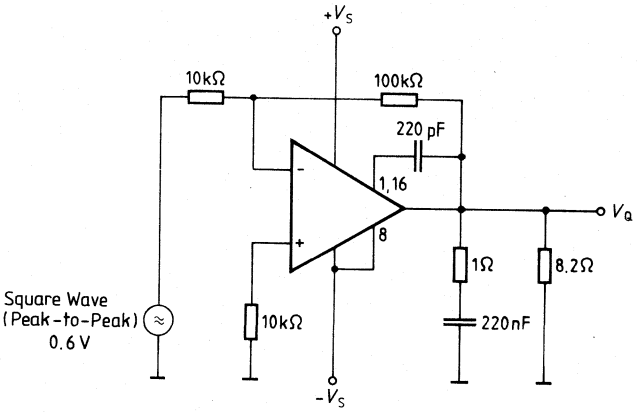
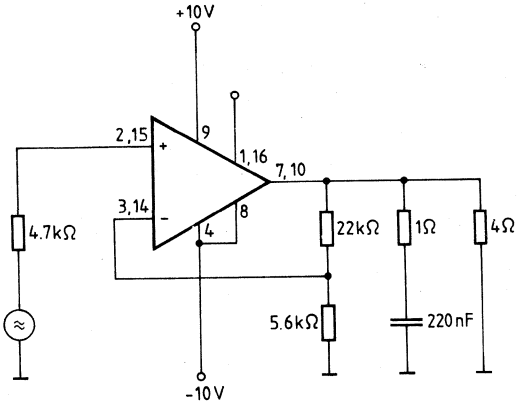


Figure 9
Slew rate for inverting operation



Application Circuits

Figure 10
Non-inverting operation
a) Amplifier; $G_V = 5$



b) Voltage follower

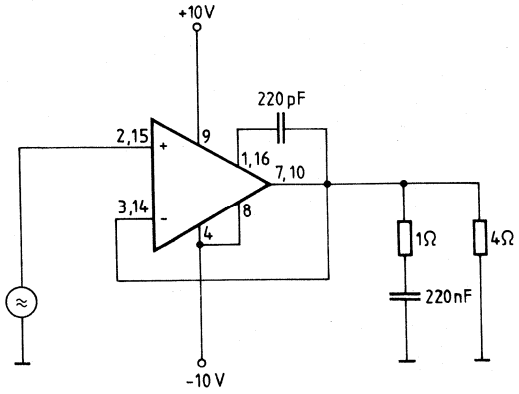
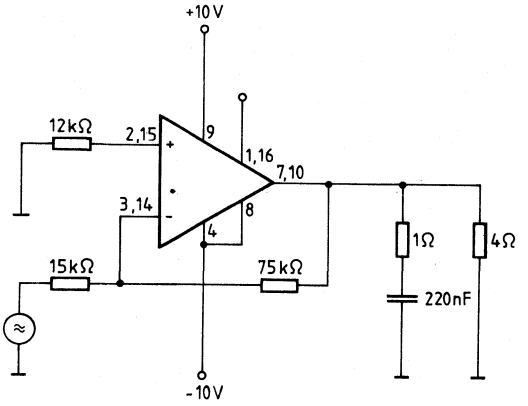
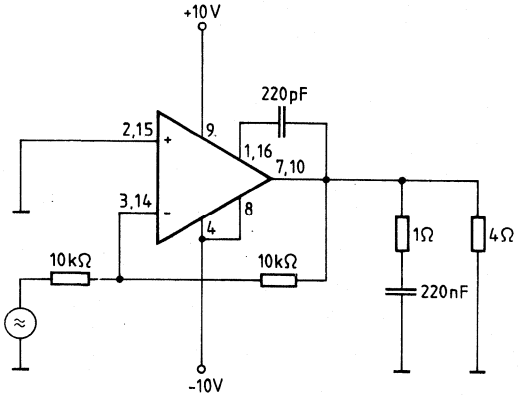


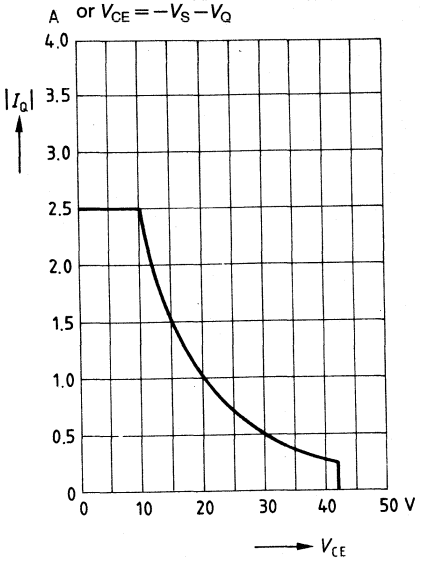
Figure 11
Inverting operation
a) Amplifier; $G_V = -5$



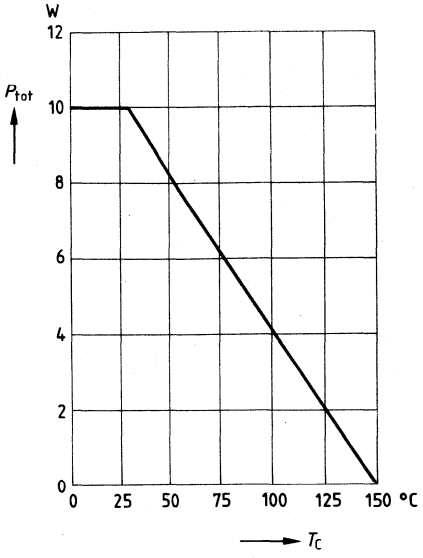
b) Inverter



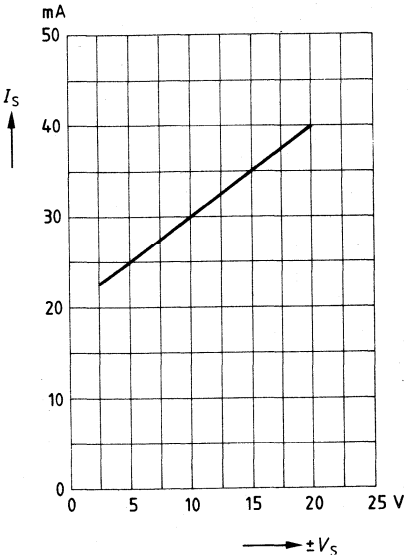
Safe operating area (SOA)
Peak output current versus collector-emitter voltage
$T_C = 25\,°C$, $V_{CE} = +V_S - V_Q$ or $V_{CE} = -V_S - V_Q$



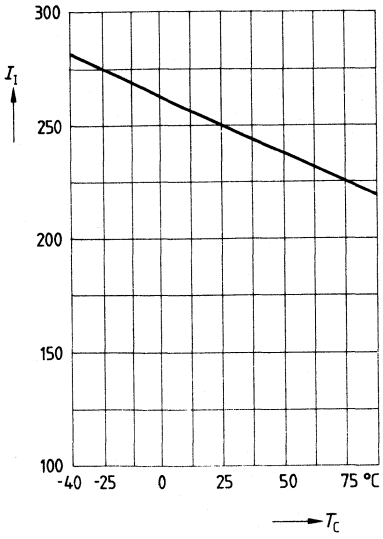
Max. permissible power dissipation versus case temperature



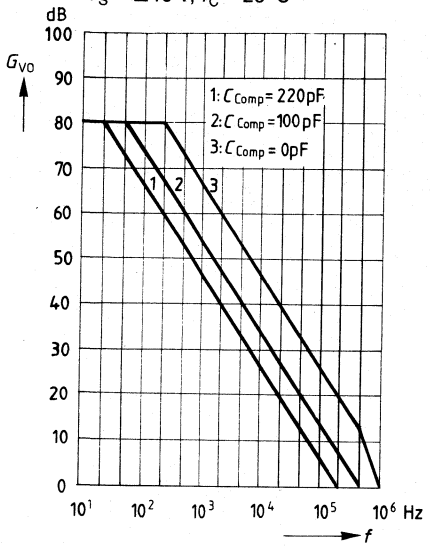
Supply current versus supply voltage
$T_C = 25\,°C$



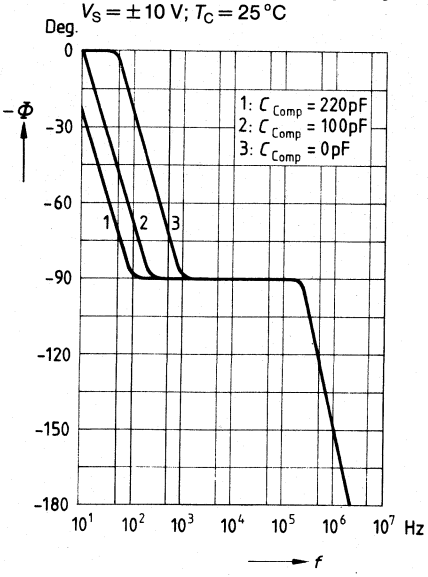
Input current versus case temperature
$V_S = \pm 10\,V$



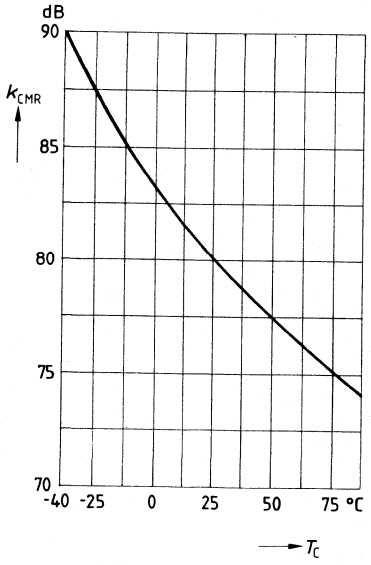
Open-loop voltage gain versus frequency
$V_S = \pm 10$ V, $T_C = 25$ °C



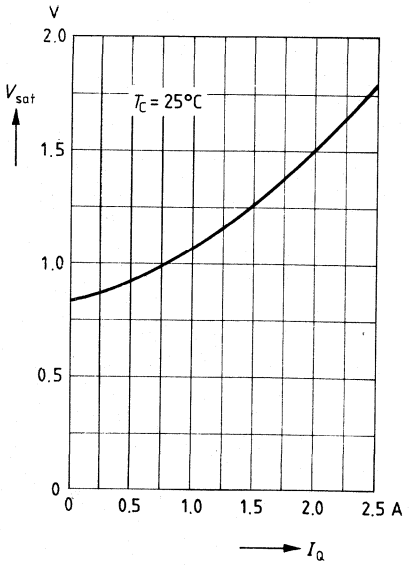
Phase response versus frequency
$V_S = \pm 10$ V; $T_C = 25$ °C



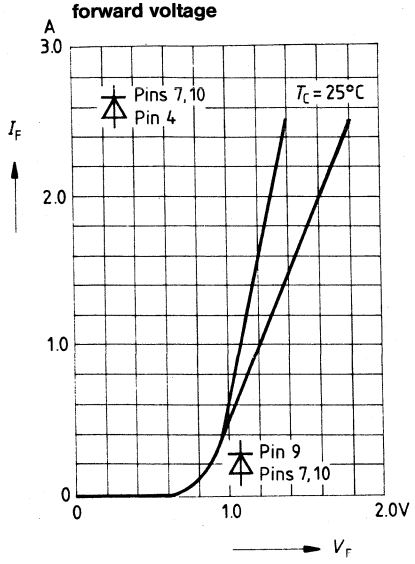
Common-mode rejection versus case temperature
$V_S = \pm 10$ V



Saturation voltage versus peak output current
$T_C = 25$ °C



Forward current versus forward voltage



Bipolar IC

Type	Ordering Code	Package
TLE 4201 A1	Q67000-A8080	P-DIP-18-L9
TLE 4201 S1	Q67000-A2285	P-SIP-9

The TLE 4201 IC is a dual comparator that is particularly suitable as a driver for reversible dc motors and may also be used as a versatile power driver.

The push-pull power-output stages work in a switch mode and can be combined into a full bridge configuration.

The driving of the comparators may be analog in the form of a window discriminator, or it can be accomplished very simply with digital logic.

Typical applications are follow-up controls, servo drives, servo motors, drive mechanisms, etc.

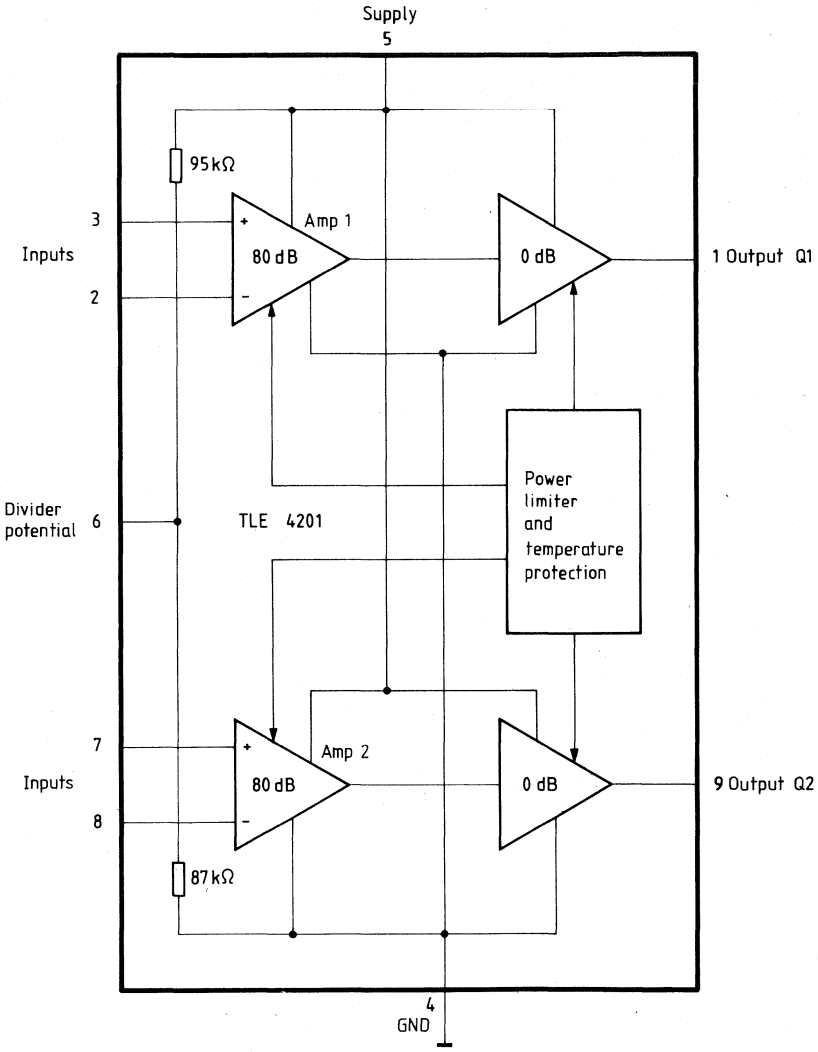
Features

- Max. output current 2.5 A
- Open-loop gain 80 dB typ.
- PNP input stages
- Large common-mode input-voltage range
- Wide control range
- Low saturation voltages
- SOA circuit
- Temperature protection

The TLE 4201 IC comes in two different packages: with the P-SIP-9 package it is possible to remove the heat by way of a cooling fin to a suitable heat sink, whereas with the P-DIP-18-L9 package the pins 10 through 18 are thermally linked to the chip and provide for heat dissipation by way of the circuit board.

Block Diagram

Figure 1



Pin Description

TLE 4201 A1 Pin	TLE 4201 S1 Pin	Function
1	1	Output of 1st amplifier
2 3	2 3	Inverting input of 1st amplifier Non-inverting input of 1st amplifier
4	4	Ground
5	5	Supply voltage
6	6	Divider potential
7 8	7 8	Non-inverting input of 2nd amplifier Inverting input of 2nd amplifier
9	9	Output of 2nd amplifier
10 to 18		Ground; to be connected to pin 4

Circuit Description

The IC contains two amplifiers featuring a typical open-loop voltage gain of 80 dB at 500 Hz. The input stages are PNP differential amplifiers. This results in a common-mode input voltage range from 0 V to almost the value of V_S, and in a maximum input differential voltage of I V_S I. To obtain low saturation voltages, the sink transistor (lower transistor) of the push-pull AB output stage is internally bootstrapped. An SOA protective circuit protects the IC against motor short circuits and ground short circuits. An internal overtemperature protection protects the IC against overheating in case of failure due to insufficient cooling or overload.

For logic control, a divider potential of approx. $V_S/2$ is available at pin 6 (see application circuit 2). This makes the IC particularly suitable as power driver for digital circuits.

Application

Figure 2 shows a window discriminator operation with the control voltage V_I.

The window within which the motor is to stop is set by R_2.

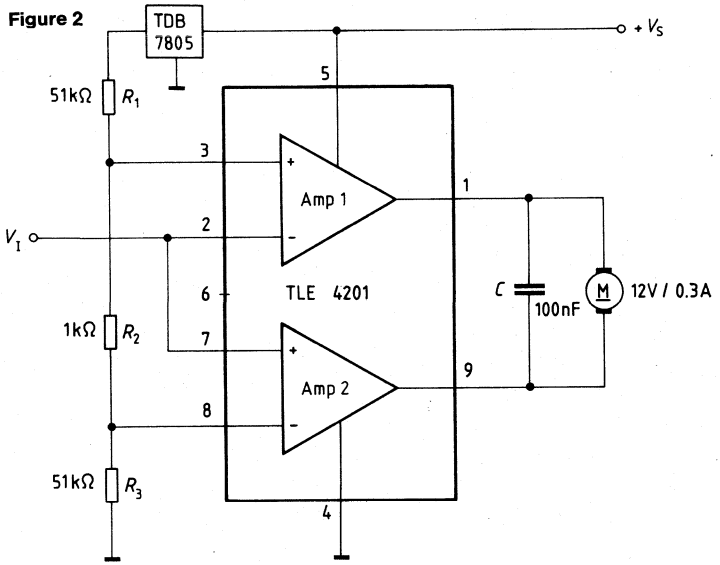
Figure 3 shows driving by logic inputs A and B. The motor is controlled according to the following truth table.

A	B	Output
L	L	Motor stopped (slowed down)
L	H	Motor turns right
H	L	Motor turns left
H	H	Motor stopped (slowed down)

Application Circuits

Operated as Window Discriminator

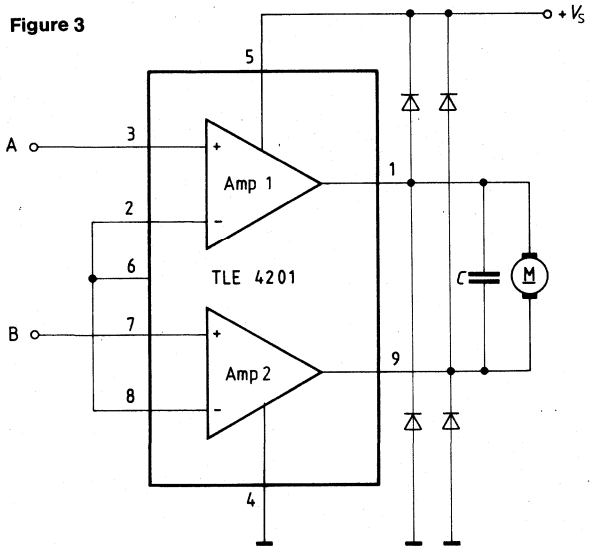
Figure 2



Digital Control

for input signals applies: H ≥ 0.6 V_S
L ≤ 0.3 V_S

Figure 3



Maximum Ratings

$T_C = -35\,°C$ to $+85\,°C$

Description	Symbol	min	max	Unit
Supply voltage	V_S		25	V
Supply voltage ($t \leq 50$ ms)	V_S		36	V
Output current	I_Q		2.5	A
Voltage of pins 2, 3, 6, 7, 8	V	−0.3	V_S	V
Voltage of pins 1, 9	V	−0.3		V
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance				
TLE 4201 S1 system – air	$R_{th\ JA}$		65	K/W
system – case	$R_{th\ JC}$		8	K/W
TLE 4201 A1 system – air[1])	$R_{th\ JA}$		60	K/W
system – PC board[1])	$R_{th\ JA1}$		44[1])	K/W

Operating Range

Supply voltage	V_S	3.5	17	V
Case temperature	T_C	−35	85	°C
Voltage gain (at negative feedback with external components)	G_V	25		dB

Characteristics

$V_S = 13$ V, $T_C = 25\,°C$

Description	Symbol	Test conditions		min	typ	max	Unit
Supply current	I_S	Figure 4: S = 1			20	30	mA
Open-loop voltage gain	G_{V0}	$f = 500$ Hz			80		dB
Input resistance	R_I	$f = 1$ kHz		1	5		MΩ
Saturation voltages		Figure 5:	S1				
Source operation	$V_{Q\ 10}$	$I_Q = 0.3$ A	1		1.0	1.1	V
		$I_Q = 1.0$ A	1		1.2	1.6	V
Sink operation	$V_{Q\ 20}$	$I_Q = -0.3$ A	2		0.35	0.5	V
		$I_Q = -1.0$ A	2		0.7	1.0	V
Rise time of V_Q	t_r	Figure 4 and 6			1.5		µs
Fall time of V_Q	t_f	Figure 4 and 6			1.5		µs
Turn-on delay time	t_{ON}	Figure 4 and 6			3.0		µs
Turn-off delay time	t_{OFF}	Figure 4 and 6			1.5		µs
Input current (pins 2, 3, 7, 8)	I_I	Figure 5 $V_{2,3,7,8} = 0$			1.5	3.0	µA
Input offset voltage	V_{I0}	Figure 7		−5		5	mV

[1]) see figure 8

Test and Measurement Circuits

Figure 4

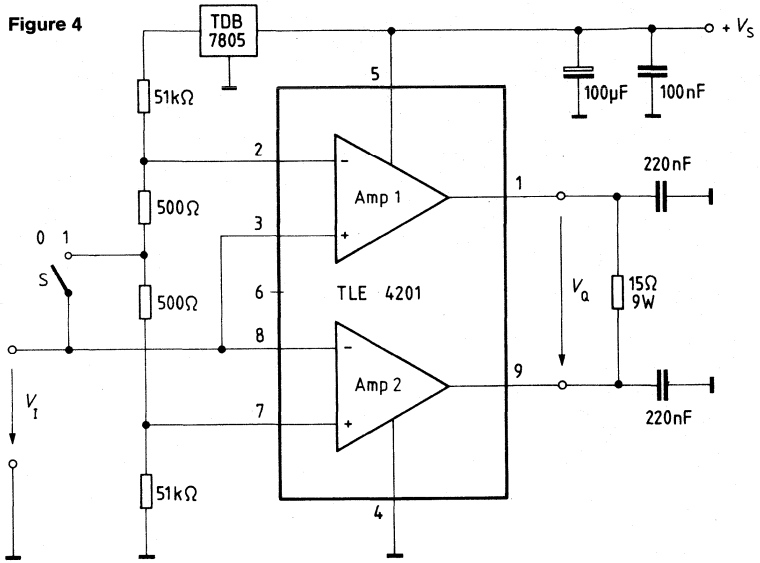


Figure 5

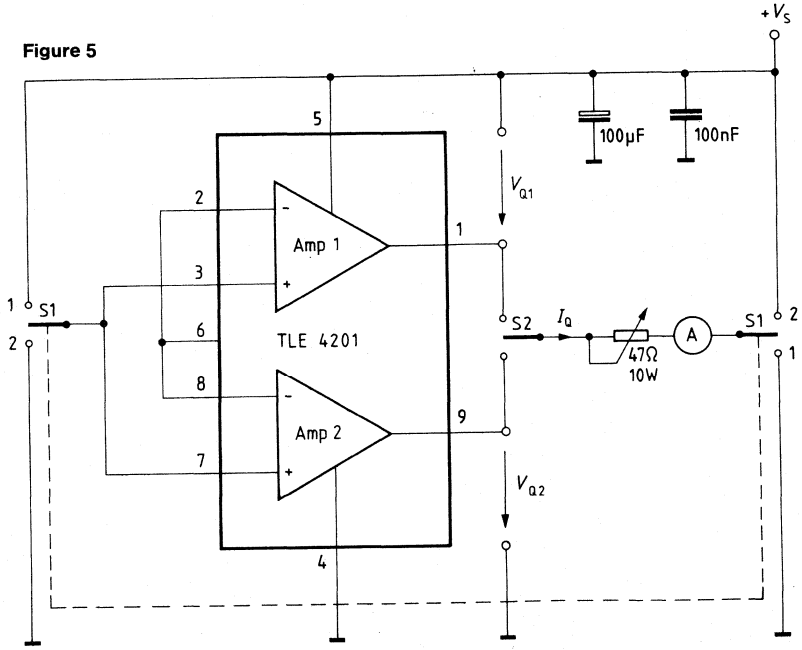


Figure 6
Pulse Diagram

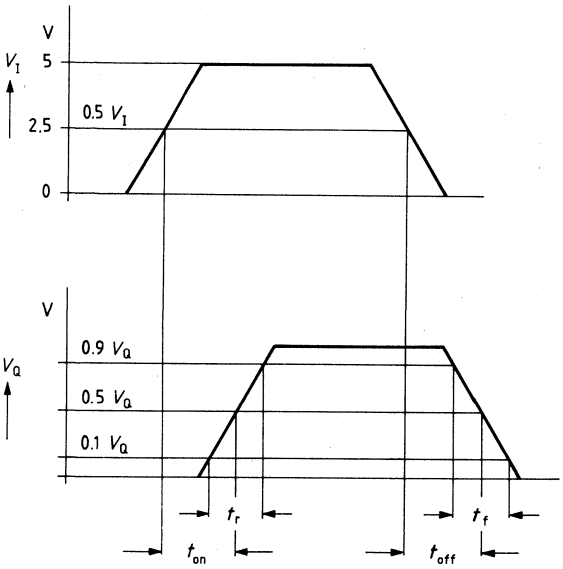
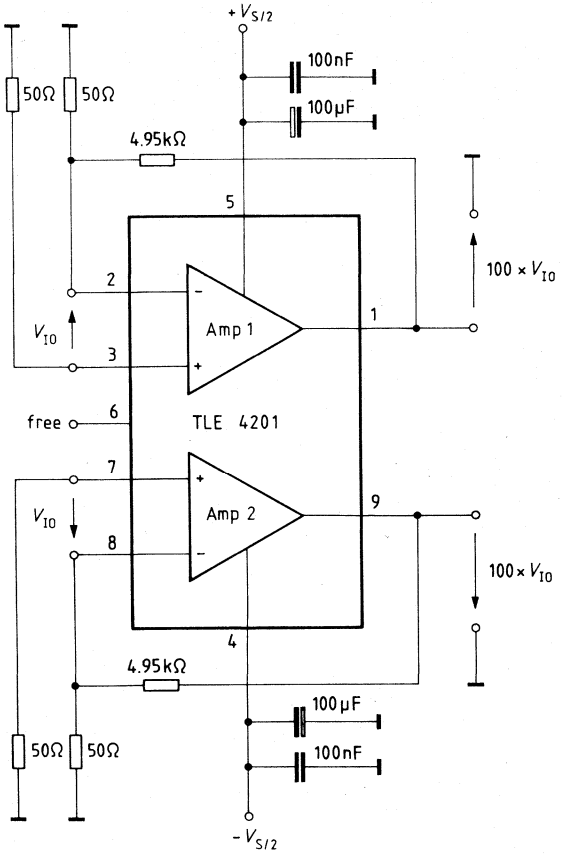


Figure 7
Test and Measurement Circuit

Input offset voltages

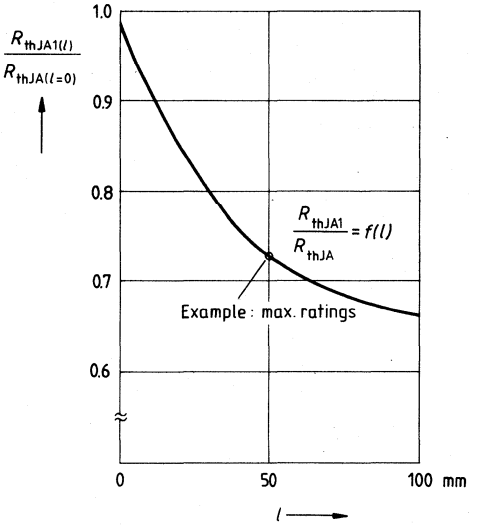


Thermal resistance of TLE 4201 A1

Thermal resistance, junction-air, $R_{th\ JA\ 1}$ (standard) versus side length l of a square copper-clad cooling surface (35 µm copper plate)

$R_{th\ JA}$ $(l = 0) = 60$ K/W
$T_A \leq 70$ °C
$P_V = 1$ W
substrate vertical
circuit vertical
still air

Figure 8



Bipolar IC

Type	Ordering Code	Package
TLE 4202	Q67000-A8007	P-T66-7-H

The TLE 4202 IC is a dual comparator that is particularly suitable as a driver for reversible dc motors and may also be used as a versatile power driver.

The two power comparators can switch magnets, motors or other loads either by being separated from each other or by being combined to a full-bridge circuit. The IC is designed for applications in motor vehicles. It can be applied at package temperatures between −40° and +130°C.

The comparators can be driven analogically in form of a window discriminator or simply by digital logic.

Typical applications are follow-up controls, servo drives, servo motors, drive mechanism, etc.

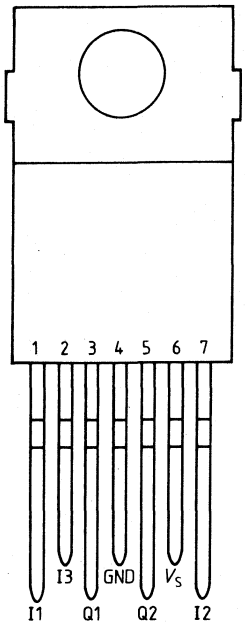
Features

- Max. output current 3.0 A
- Open-loop gain 80 dB typ.
- PNP input stages
- Large common-mode input-voltage range
- Wide control range
- Low saturation voltages
- SOA circuit
- Temperature protection
- Short-circuit proof to ground
- Suitable for applications in automotive engineering

Circuit Description

The IC contains two amplifiers featuring a typical open-loop voltage gain of 80 dB at 500 Hz. The input stages are PNP differential amplifiers. This results in a common-mode input voltage range from 0 V to almost the value of V_S, and in a maximum input differential voltage of I V_S I. To obtain low residual voltages at the sink transistor, the drive circuit of the sink transistor is connected to the supply voltage. An SOA circuit protects the IC against ground short-circuits.

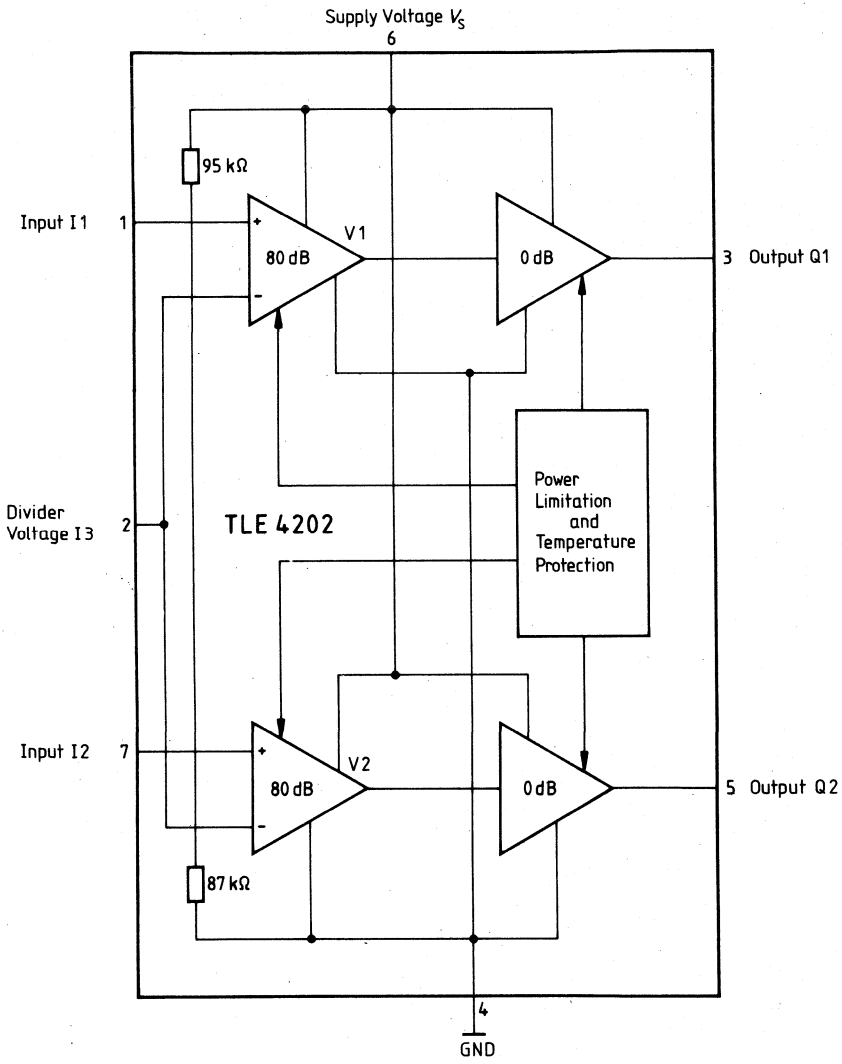
Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	I1	**Input** Non-inverting input 1, to be connected to pin 2 and pin 3 according to general rules
2	I3	**Inverting input** Inverting input of the two comparators, to be connected according to general rules
3	Q1	**Output Q1** Push-pull B output dc-short-circuit proof to ground
4	GND	**Ground**
5	Q2	**Output Q2** see pin 3
6	V_S	**Supply voltage V_S** Has to be blocked to ground with a ceramic capacity or of at least 100 nF directly at the pins of the ICs
7	I2	**Input** Non-inverting input I2, see pin 1

Block Diagram



Maximum Ratings

$T_C = -40\,°C$ to $+130\,°C$

Description	Symbol	min	max	Unit
Supply voltage Supply voltage ($t \leq 50$ ms)	V_S V_S		25 36	V V
Output current $T_C \leq 85\,°C$	I_Q	−3.0	3.0	A
Voltage at pins 1, 2, I3 Voltage at the pins Q1, Q2	$V_{1,2,7}$ $V_{3,5}$	−0.3 −0.7	V_S $V_S + 0.7$	V V
Junction temperature Storage temperature	T_j T_{stg}	 −55	150 125	°C °C

Operating Range

Supply voltage	V_S	3.5	17	V
Package temperature during operation $R_L \geq 11\,\Omega$, $V_S = 7 \ldots 16$ V $R_L \geq 18\,\Omega$, $V_S = 16$ V	T_C	 −40	 130	 °C °C
Voltage gain (at negative feedback with external connection)	G_V	30		dB
Thermal resistance system – case	$R_{th\,SC}$		4.8	K/W

Outputs Q1 and Q2 short-circuit proof to ground

R_L: Resistance between output 1 and output 2

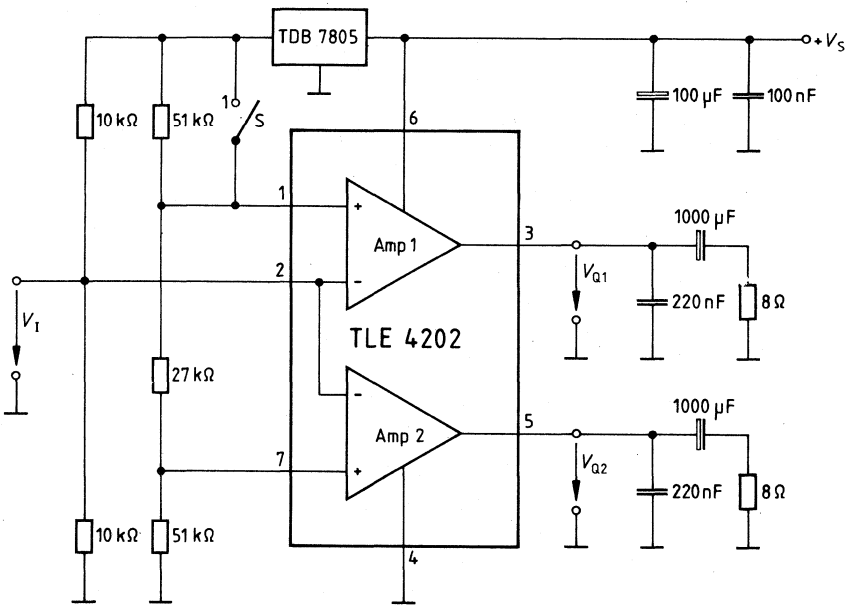
Characteristics

$V_S = 13$ V, $T_C = 25$ °C

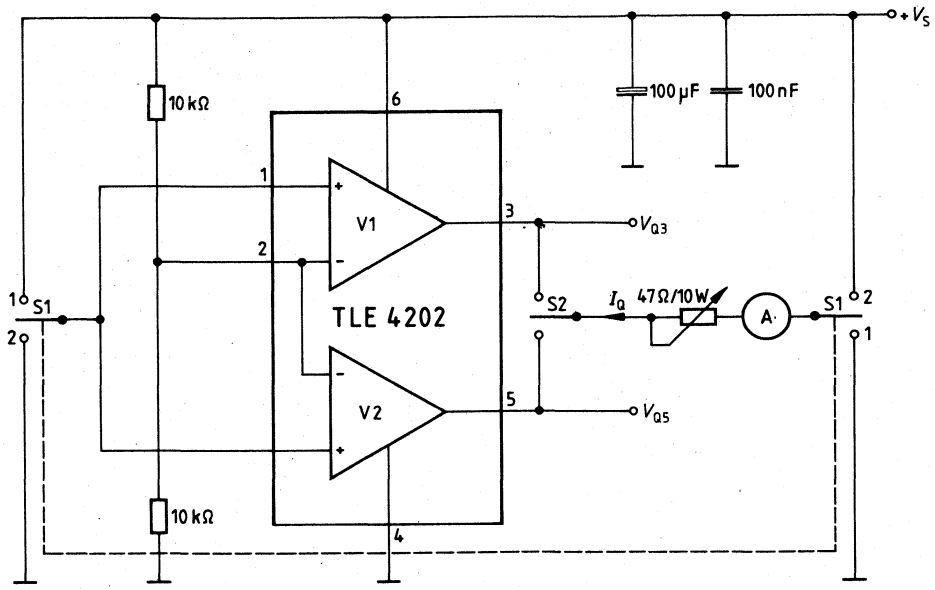
Description	Symbol	Measuring conditions	Measuring circuit	min	typ	max	Unit
General characteristics							
Quiescent current	I_q	$S = 1$	1		15	25	mA
Open-loop voltage gain	G_{VO}	$f = 500$ Hz[1]	1	50	80		dB
Input characteristics							
Input current (pins I1, I2)	$I_{I\,1,7}$	$V_{I\,1,12} = 0$	2		1.5	3.0	µA
Input resistance	$R_{I\,1,7}$	$f = 1$ kHz	1	1	5		MΩ
Input offset voltage	V_{I0}		3	−20		20	mV
Output characteristics							
Source operation	V_{Sato}	$I_Q = -0.3$ A S1 = 1	2		1.0	1.1	V
		$I_Q = -1.0$ A S1 = 1	2		1.2	1.6	V
		$I_Q = -1.5$ A S1 = 1[1]	2		1.3	2.0	V
Sink operation	V_{Satu}	$I_Q = +0.3$ A S1 = 2	2		0.35	0.5	V
		$I_Q = +1.0$ A S1 = 2	2		0.7	1.0	V
		$I_Q = +1.5$ A S1 = 2[1]	2		0.8	1.5	V
Short-circuit current	$I_{Q\,max}$	Source operation[1]	2		1.25	1.60	A
Slew-rate (falling edge)	SR		1	6			V/µs
Slew-rate (rising edge)	SR		1	6			V/µs
Switching times							
Rise time of V_Q	t_r		1		1.5		µs
Falling time of V_Q	t_f		1		1.5		µs
Turn-on delay	t_{ON}		1		3.0		µs
Turn-off delay	t_{OFF}		1		1.5		µs

[1] $-40\,°C \le T_C \le 110\,°C$
$7\,V \le V_S \le 16\,V$

Measuring Circuit 1

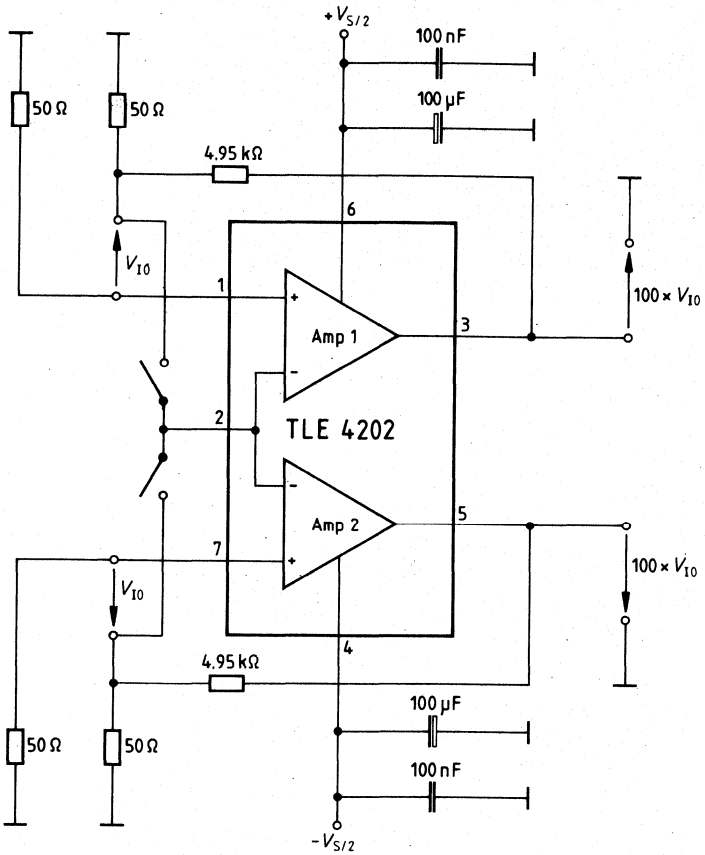


Measuring Circuit 2

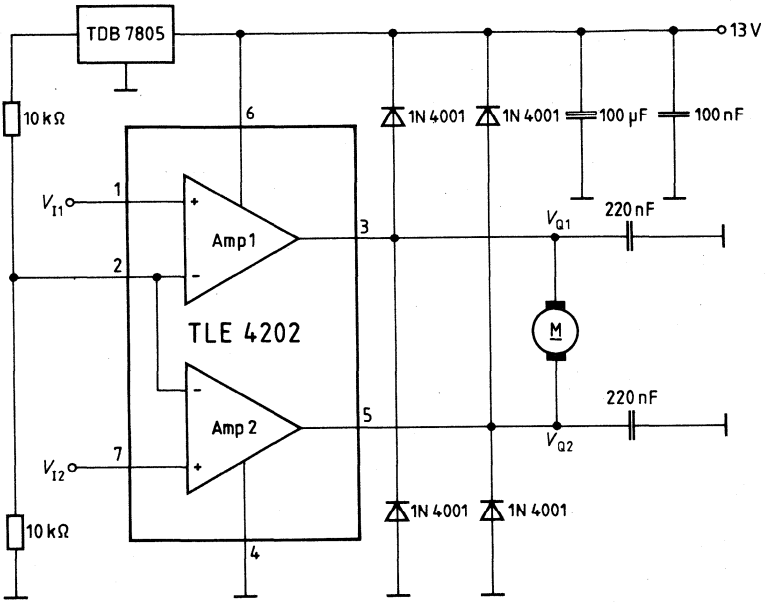


$V_{Sato} = V_S - V_{Q3/5}$
$V_{Satu} = V_{Q3/5}$
$I_{SC} = -I_Q$

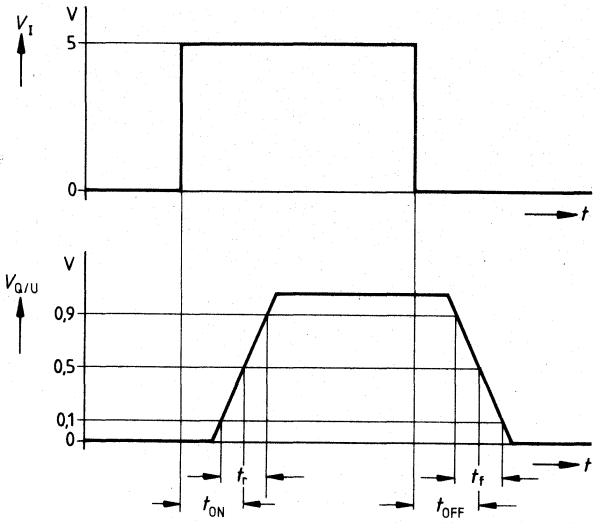
Measuring Circuit 3



Application Circuit



Diagram



Preliminary Data **Bipolar IC**

Type	Ordering Code	Package
TLE 4202 B	Q67000-A8225	P-T66-7-H

The two power comparators can switch magnets, motors or other loads either by being separated from each other or by being combined to a full-bridge circuit. The IC is designed for application in motor vehicles. It can be applied at package temperatures between −40 °C and +130 °C.

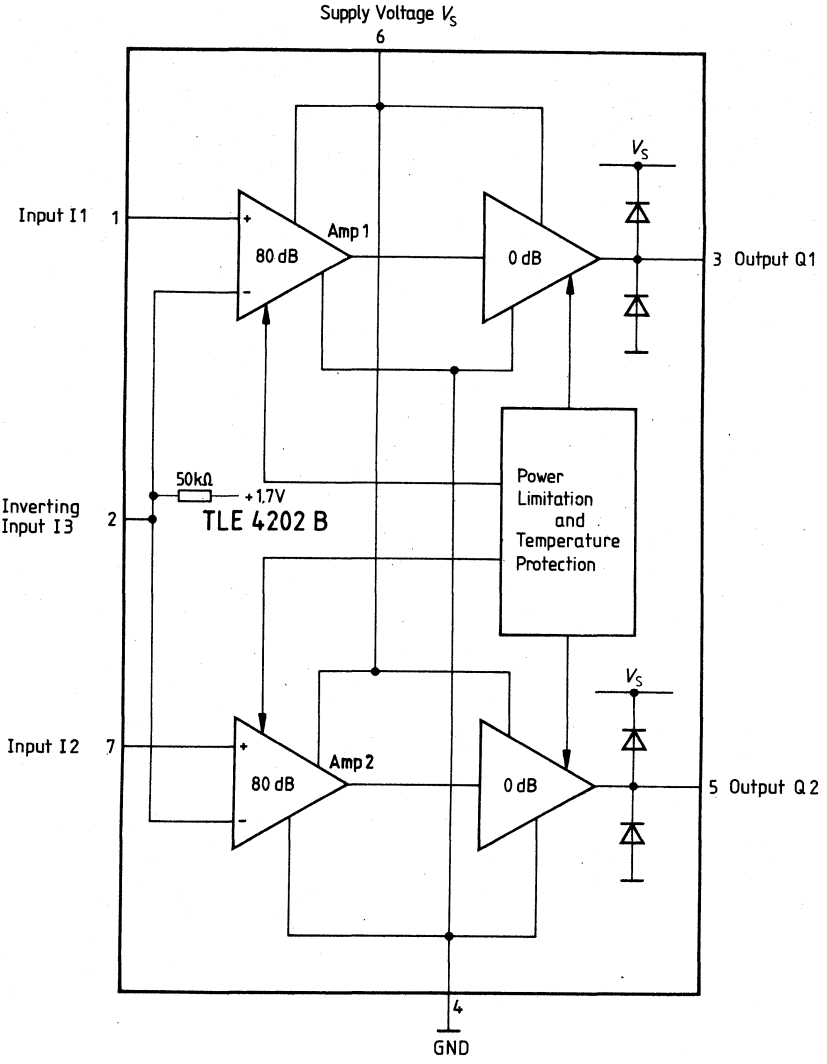
The IC contains two amplifiers featuring a typical open-loop voltage gain of 80 dB at 500 Hz.

The input stages are PNP differential amplifiers thus resulting in a common-mode input voltage range from 0 V to approx. the value of V_S and in a maximum input differential voltage of V_S. To obtain low saturation voltages at the sink circuit, the drive circuit of the sink transistor is connected to the supply voltage. An SOA protective circuit protects the IC against ground short-circuits. At chip temperatures above approx. 160 °C the source transistors are turned off.

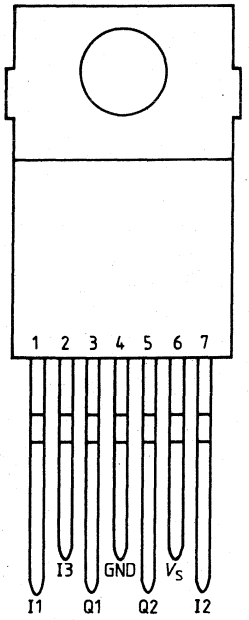
Features

- Drives motors up to 2 A
- Integrated free-wheel diodes 2.5 A
- Short-circuit proof to ground
- Overtemperature protection
- Low saturation voltages through bootstrap
- Wide temperature range
- Suitable for applications in automotive engineering

Block Diagram



Pin Configuration
(top view)



Pins

Pin	Symbol	Function
1	I1	**Input 1** Non-inverting input 1, to be connected to pin 2 and pin 3 according to general rules
2	I3	**Inverting input 3** Inverting inputs of the two comparators; internally connected to reference voltage across 50 kΩ (typ. 1.7 V)
3	Q1	**Output Q1** Push-pull output B dc-short-circuit proof to ground. Integrated free-wheel diodes to ground and to supply voltage
4	GND	**Ground**
5	Q2	**Output Q2,** see pin 3
6	V_S	**Supply voltage** Has to be blocked to ground with a ceramic capacitor of at least 100 nF directly at the pins of the ICs
7	I2	**Input 2** Non-inverting input 2; see pin 1

Maximum Ratings

$T_C = -40\,°C$ to $+130\,°C$

Description	Symbol	min	max	Unit
Supply voltage	V_S		40	V
Output current of sink transistors $T_C \leq 85\,°C$	I_Q		2.5	A
Output current of source transistors internally limited	I_Q			
Diode peak currents				
to $+V_S$	I_{F+}		2.5	A
to ground	I_{F-}		2.5	A
Voltage at pins I1, I2, I3	$V_{1,2,7}$	−0.3	V_S	V
Voltage at pins Q1, Q2[1])	$V_{3,5}$			V
Junctione temperature	T_j		150	°C
Storage temperature	T_{stg}	−55	125	°C

Operating Range

Description	Symbol	min	max	Unit
Supply voltage	V_S	3.5	17	V
Package temperature during operation	T_C			
$R_L \geq 6\,\Omega$, $V_S = 7 \ldots 16$ V		−40		°C
$R_L \geq 9\,\Omega$, $V_S = 16$ V			130	°C
Voltage amplification (at negative feedback with external connection)	V_V	30		dB
Thermal resistance system – case	$R_{th\,SC}$		4.8	K/W

Outputs Q1 and Q2 short-circuit proof to ground

R_L: Resistance between output 1 and output 2

[1]) The output voltages are kept within a permissible range by free-wheel diodes

Characteristics

$V_S = 13$ V, $T_C = 25$ °C

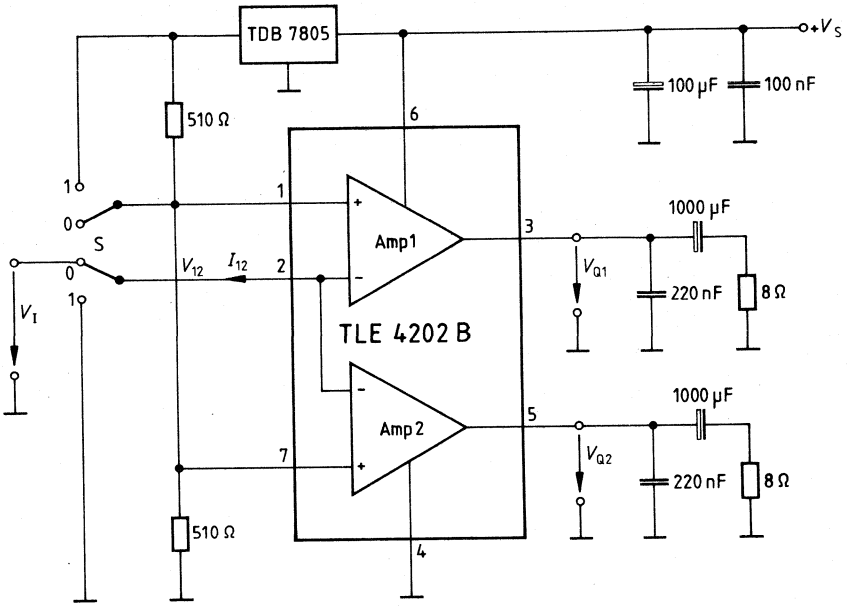
Description	Symbol	Mesuring conditions	Measuring circuit	min	typ	max	Unit
General data							
Quiescent current	I_S	$S = 1$	1		15	25	mA
Open-loop gain	G_{VO}	$f = 500$ Hz $V_S \leq 7$ V ≤ 16 V $T_C = -40$ °C to +110 °C	1	50	80		dB
Input characteristics							
Input current (pins I1, I2)	$I_{I1,7}$	$V_{I1,12} = 0$	2		1.0	3.0	µA
Input current	I_{I2}	$V_{I2} = 0$; $V_{I1,7} = V_S$	1		35	70	µA
	$-I_{I2}$	$V_{I2} \leq V_S$; $V_{I1,7} = 0$ V			230	300	µA
Input resistance	$R_{I1,7}$	$f = 1$ kHz	1	1	5		MΩ
Input reference voltage	V_{I2}	$I_{I2} = 0$; $V_{I1,7} = 0$ V	1	1.4	1.7	2.0	V
Input offset voltage	V_{I0}		3	−20		20	mV
Output characteristics							
Saturation voltages							
Source operation	V_{Sato}	$I_Q = -0.3$ A S1 = 1	2		0.9	1.0	V
measured to V_S	V_{Sato}	$I_Q = -1.0$ A S1 = 1	2		1.2	1.6	V
	V_{Sato}	$I_Q = -2$ A S1 = 1	2		1.5	2.1	V
Sink operation	V_{Satu}	$I_Q = +0.3$ A S1 = 2	2		0.25	0.4	V
		$I_Q = +1.0$ A S1 = 2	2		0.5	0.75	V
	V_{Satu}	$I_Q = +2$ A S1 = 2	2		1.0	1.3	V
Short-circuit current	I_{SC}	$V_Q = 0$ V	2		1.25	1.60	A
Diode forward voltage							
to $+V_S$	V_{F+}	$I_F = I_Q = +1$ A	2		1.0	1.3	V
to ground	V_{F-}	$I_F = I_Q = -1$ A	2		0.9	1.2	V
Slew rate falling edge	SR		1		6		V/µs
Slew rate rising edge	SR		1		6		V/µs
Switching times							
Rise time of V_Q	t_r		1		1.5		µs
Fall time of V_Q	t_f		1		1.5		µs
Switch-on delay	t_{ON}		1		3.0		µs
Switch-off delay	t_{OFF}		1		1.5		µs

Characteristics

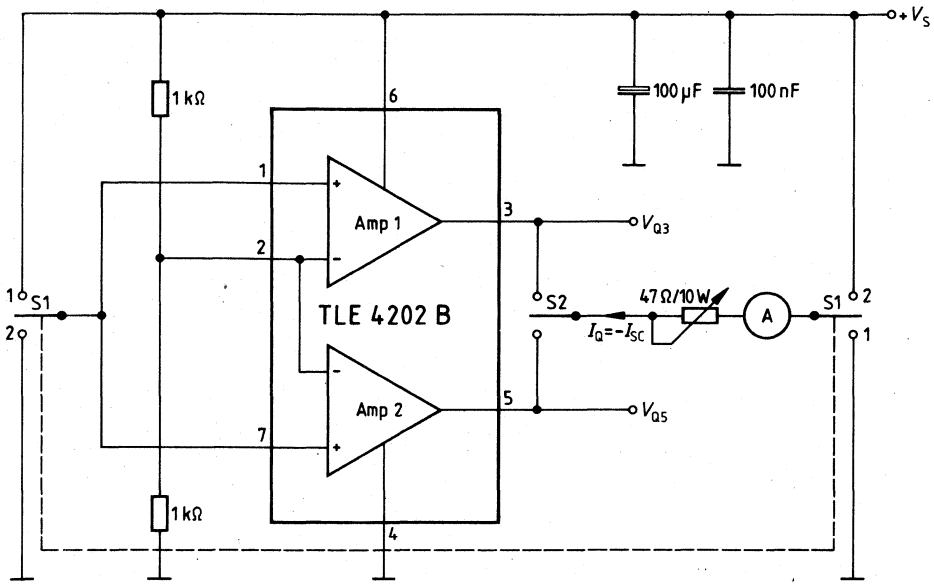
$V_S \leq 7$ V to ≤ 17 V; $T_C = -40$ °C to +110 °C

Description	Symbol	Measuring conditions	Measuring circuit	min	typ	max	Unit
Quiescent current	I_S	S = 1	1		15	30	mA
Saturation voltage							
Source operation measured to V_S	V_{Sato}	$I_Q = -0.3$ A; S = 1	2		0.9	1.2	V
	V_{Sato}	$I_Q = -1$ A; S = 1	2		1.2	1.8	V
	V_{Sato}	$I_Q = -2$ A; S = 1	2		1.5	2.4	V
Sink operation	V_{Satu}	$I_Q = 0.3$ A; S1 = 2	2		0.25	0.60	V
	V_{Satu}	$I_Q = 1$ A; S1 = 2	2		0.5	1.1	V
	V_{Satu}	$I_Q = 2$ A; S1 = 2	2		1.2	2.0	V
Short-circuit current	$-I_{SC}$	$V_Q = 0$ V T_C=+25 °C to+110 °C				3.5	V

Measuring Circuit 1



Measuring Circuit 2

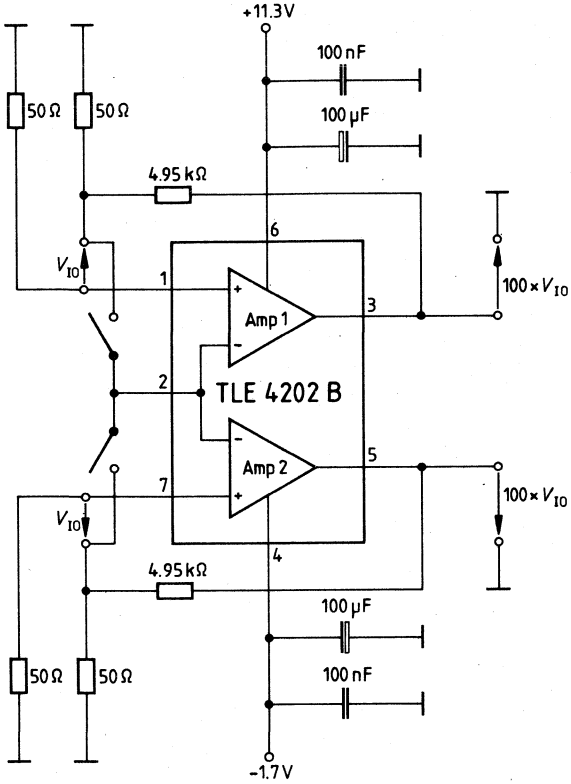


$V_{Satc} = V_S - V_{Q3/5}$

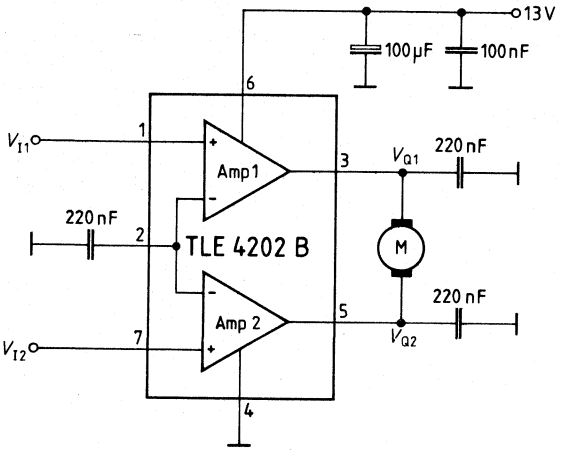
$V_{Satu} = V_{Q3/5}$

$I_{SC} = -I_Q$

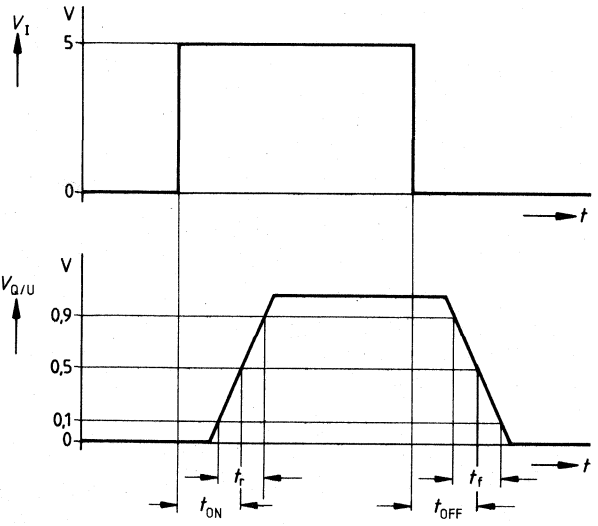
Measuring Circuit 3



Application Circuit



Diagram



Preliminary Data **Bipolar IC**

Type	Ordering Code	Package
TLE 4204	Q67000-A8182	P-T66-7-H

Integrated 3 A full-bridge dc motor driver with temperature protection, fully protected output stages and integrated free-wheel diodes. The package temperature range is −40 °C to +125 °C. The IC is also especially suitable for application in motor vehicles.

Features

- Max. output current 4 A
- Outputs short-circuit proof to $\pm V_S$
- Thermal overload protection
- Integrated free-wheel diodes to $\pm V_S$
- Max. supply voltage 45 V
- Suitable for motor vehicles

Application Description

In industrial electronics full-bridge dc motor drivers are mostly applied for bidirectional motor drives. Both of the differential control inputs act on the outputs as follows:

State	Differential input voltage 1	Differential input voltage 2	Output 1	Output 2
1	<0	<0	V_{QL}	V_{QL}
2	<0	>0	V_{QL}	V_{QH}
3	>0	<0	V_{QH}	V_{QL}
4	>0	>0	V_{QH}	V_{QH}

V_{QL} means: Lower power unit conducts; upper power unit is blocked
V_{QH} means: Upper power unit conducts; lower power unit is blocked

Examples:
State 1: Motor is slowed down
State 2: Motor turns right
State 3: Motor turns left
State 4: Motor is slowed down

Circuit Description

Input Circuit

The input stages are designed as differential inputs with an open-loop gain of typ. 80 dB and a common-mode input voltage range to 0 V.

Output Stages

The output stages consist of two push-pull C stages. Using the protective circuits for limiting the power dissipation makes the outputs short-circuit proof to ground and to supply voltage throughout the entire operating range. Positive and negative voltage peaks which occur during switching of inductive loads, are limited by integrated diodes.

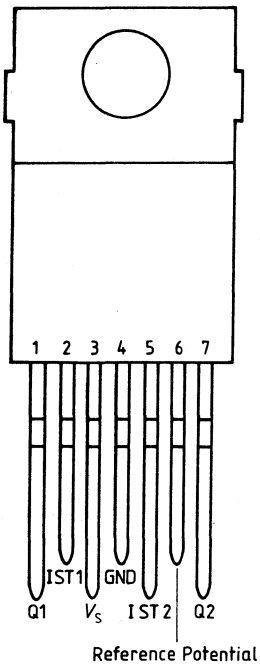
Monitoring and Protecting Functions

The IC is protected against thermal overload by a temperature protecting unit.

The power units are controlled by a protection circuit. At low voltages (up to 8 V) only the current is limited in order to protect the bond leads. At higher voltages the protection circuit controls the power dissipation in the power unit.

Pin Configuration

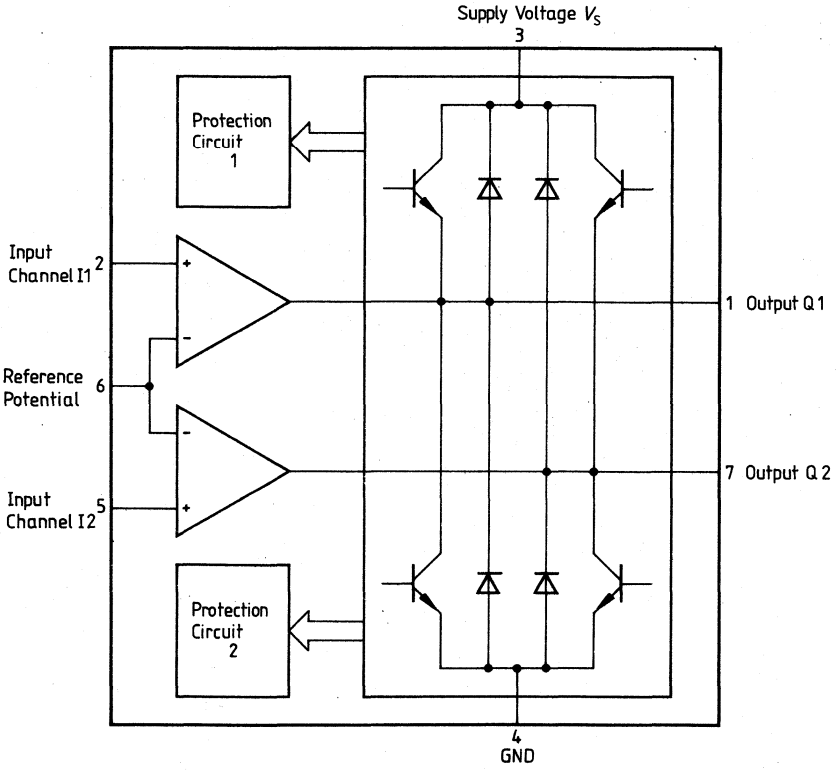
(top view)



Pin Description

Pin	Symbol	Function
1	Q1	**Output for channel 1** Short-circuit proof push-pull C output channel 1 for rated currents up to 3 A. Free-wheel diodes to $+V_S$ and to ground are integrated.
2	IST1	**Control input for channel 1** Differential input referred to pin 6; of non-inverting effect on output channel 1. The common-mode range is specified from V_S −2.5 V to ground.
3	V_S	**Supply voltage** Block against ground (pin 4) with a ceramic capacitor of 220 nF min. close to pin 3. For longer connections a low-inductance circuit-proof supporting electrolytic capacitor of at least 10 µF between pin 3 and 4 is to be supplied. The connection is to be designed for the maximum short-circuit current (2 x 4 A).
4	GND	**Ground** Design the connection for the maximum short-circuit current (2 x 4 A).
5	IST2	**Control input channel 2** Differential input referred to pin 6; of non-inverting effect on output 2. The common-mode range is specified from V_S −2.5 V to ground.
6	Reference potential	**Input reference potential for channel 1 and 2** The user can individually determine the switching threshold with this input. The common-mode range is specified from V_S −2.5 V to ground.
7	Q2	**Output for channel 2** Short-circuit proof push-pull C output channel 2 for rated currents up to 3 A. Free-wheel diodes to $+V_S$ and to ground are integrated.

Block Diagram



Maximum Ratings

$T_A = -40\,°C$ to $+125\,°C$

Description	Symbol	min	max	Unit
Voltages				
Supply voltage	V_S	−0.3	45	V
Input voltages Pin 2, 5 and 6	V_I	−0.3	$+V_S$	V
Currents				
Supply current $T_C \leq 85\,°C$	I_S	−3	8	A
Output current $T_C \leq 85\,°C$	$I_{Q\,1,2}$	−4	4	A
Ground current $T_C \leq 85\,°C$	I_{GND}	−8	8	A
Diode peak currents				
to $+V_S$	I_{F+}		1.5	A
to ground	I_{F-}		4	A
Temperatures				
Junction temperature	T_j		150	°C
Storage temperature range	T_{stg}	−50	150	°C
Operating Range				
Supply voltage	V_S	8	24	V
Case temperature $T_j \leq 150\,°C$	T_C	−40	125	°C
Thermal resistance				
system – case	$R_{th\,SC}$		4	K/W
system – ambient	$R_{th\,SA}$		65	K/W

Characteristics

$T_C = 25\,°C$; $V_S = 12\,V$

Description	Symbol	Measuring conditions	min	typ	max	Unit
General ratings						
Quiescent current	I_1	$V_{2,5} = 12\,V$; $V_6 = 0\,V$		15	30	mA
Control inputs						
Input offset voltage	V_{I0}		−10		10	mV
Input offset current	I_{I0}		−100		100	nA
Input current	$-I_{I,2,5}$	$V_{2,5} = 0\,V$ $V_6 = 12\,V$		1	2	µA
Input current	$-I_{I6}$	$V_{2,5} = 12\,V$ $V_6 = 0\,V$		2	4	µA
Common-mode input voltage ranges						
to $+V_S$	V_{IC+}	Difference to $+V_S$		2.5	3	V
to ground	V_{IC-}	to ground		−0.5	0	V
Output stages						
Saturation voltages						
to $+V_S$	V_{QSato}	$V_{I6} < V_{I2,5}$; $I_Q = -1\,A$ [1]		1.0	1.3	V
to $+V_S$	V_{QSato}	$V_{I6} < V_{I2,5}$; $I_Q = -3\,A$ [1]		2.0	2.5	V
to ground	V_{QSatu}	$V_{I6} > V_{I2,5}$; $I_Q = 1\,A$		1.0	1.3	V
to ground	V_{QSatu}	$V_{I6} > V_{I2,5}$; $I_Q = 3\,A$		2.0	2.5	V
Forward voltages						
to $+V_S$	V_{Fo}	$V_{I6} < V_{I2,5}$; $I_Q = 1\,A$ [1]		1.2	1.4	V
to ground	V_{Fu}	$V_{I6} > V_{I2,5}$; $I_Q = -1\,A$		−1	−1.2	V
to ground	V_{Fu}	$V_{I6} > V_{I2,5}$; $I_Q = -3\,A$		−1.4	−1.6	V
Short-circuit currents						
at short-circuit		S 1P, 2P closed				
to $+V_S$	$I_{QP1,7}$					
$V_6 > V_{12,5}$						
	$I_{QP1,7}$	$V_S = 12\,V$		2.5	3.5	A
	$I_{QP1,7}$	$V_S = 24\,V$		1.0		
at short-circuit		S 1M, 2M closed				
to ground	$-I_{QM1,7}$					
$V_6 < V_{12,5}$						
	$-I_{QM1,7}$	$V_S = 12\,V$	1	2.5	3.5	A
	$-I_{QM1,7}$	$V_S = 24\,V$	1	1.5		A
Switching times						
Turn-on time	$t_{D\,ON}$	see figure 2		2	4	µs
Turn-off time	$t_{D\,OFF}$	see figure 2		3	6	µs

[1]) measured to $+V_S$

Figure 1
Test Circuit

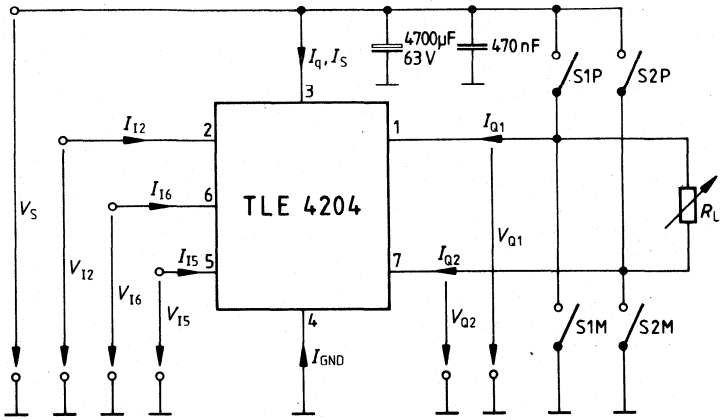
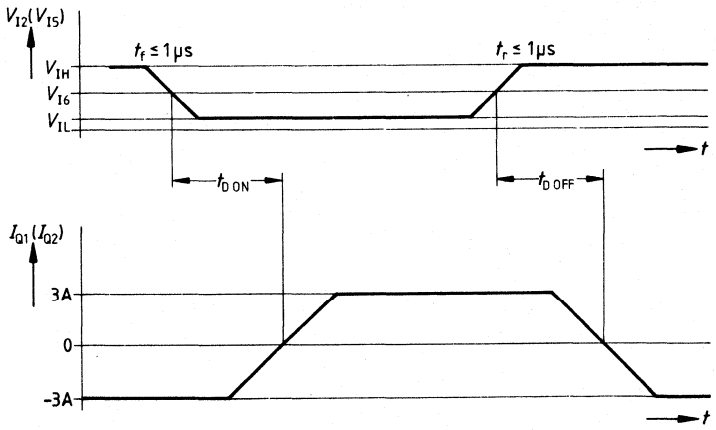
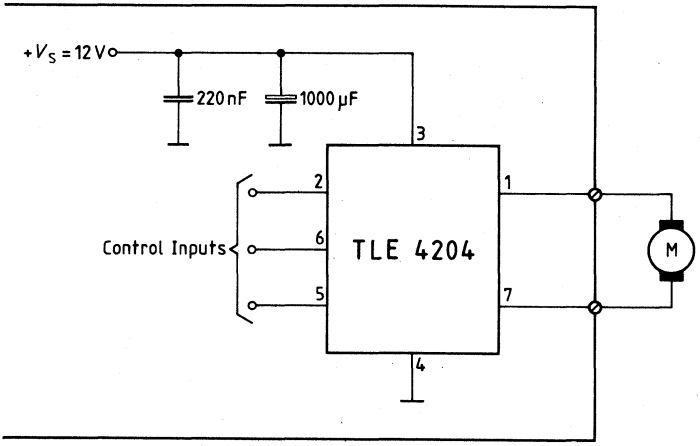


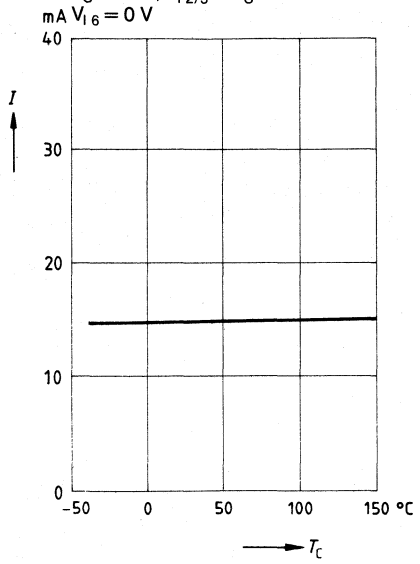
Figure 2



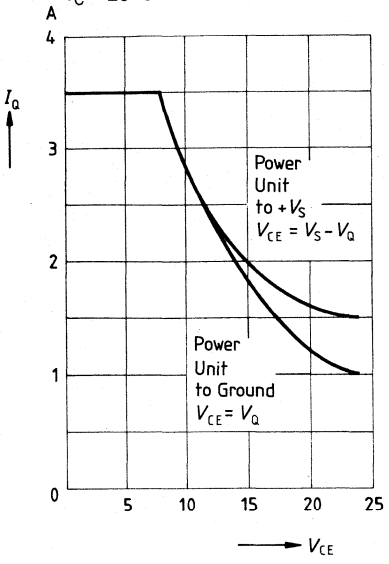
Application Circuit



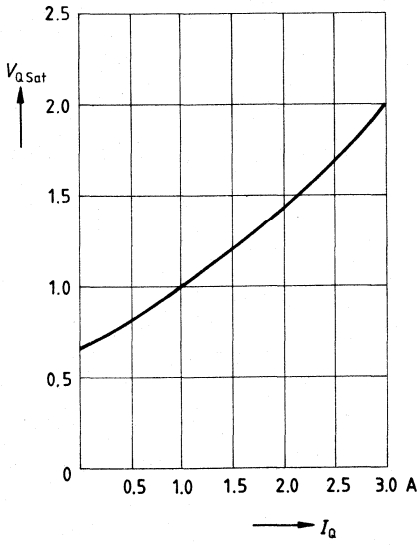
Quiescent current I_q versus case temperature T_C
$V_S = 12$ V; $V_{I\,2/5} = V_S$



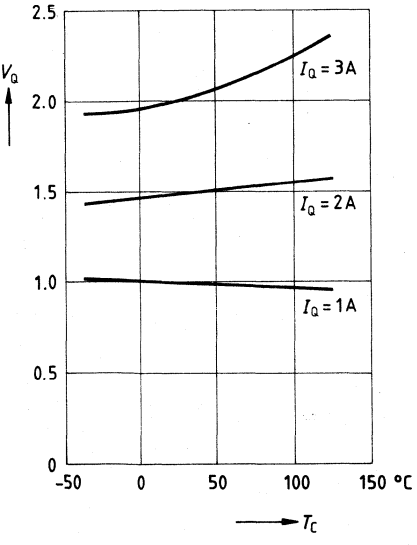
Short-circuit current I_Q versus voltage V_{CE} of power unit
$T_C = 25$ °C



Saturation voltage V_{QSat} versus output current I_Q
$V_S = 12$ V; $T_C = 25$ °C



Saturation voltage V_{QSat} versus case temperature T_C
$V_S = 12$ V; $P_D \leq 6$ W



Preliminary Data **Bipolar IC**

Type	Ordering Code	Package
TCA 1561 B	Q67000-A8209	P-SIP-9
TCA 1560 B	Q67000-A8208	P-DIP-18-L9

The TCA 1561 B is a bipolar monolithic IC designed to control the motor current in one phase of a bipolar stepper motor. It can also be used to drive direct-current motors as well as all inductive loads operated by constant current.

The IC has TTL-compatible logic inputs and contains a full-bridge driver with integrated, high-speed free-wheel diodes and chopper-operated dynamic motor current limiting. The nominal current is infinitely variable with a control voltage. Using minimum external components and a single supply voltage, two TCA 1561 B ICs form a complete and directly MC-drivable system for two-phase bipolar stepper motors with output currents up to 2.5 A per phase.

The functionally identical TCA 1560 B in P-DIP-18-L9 package is designed for output currents up to 1.25 A.

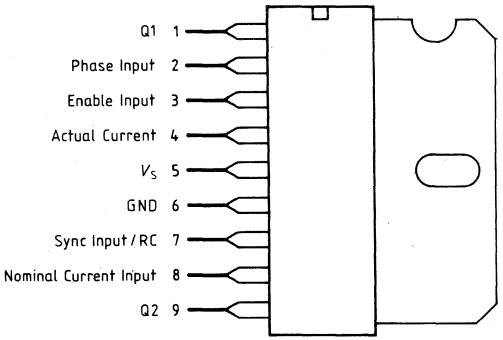
Features

- 2.5 A peak current
- High-speed integrated free-wheel diodes
- Simple drive
- Thermal overload protection with hysteresis

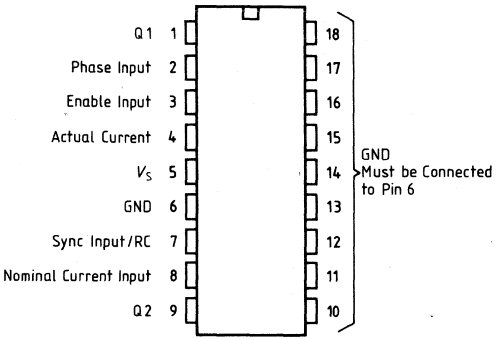
TCA 1561 B

Pin Configurations
(top view)

TCA 1561 B



TCA 1560 B



Pin Descriptions

TCA 1561 B

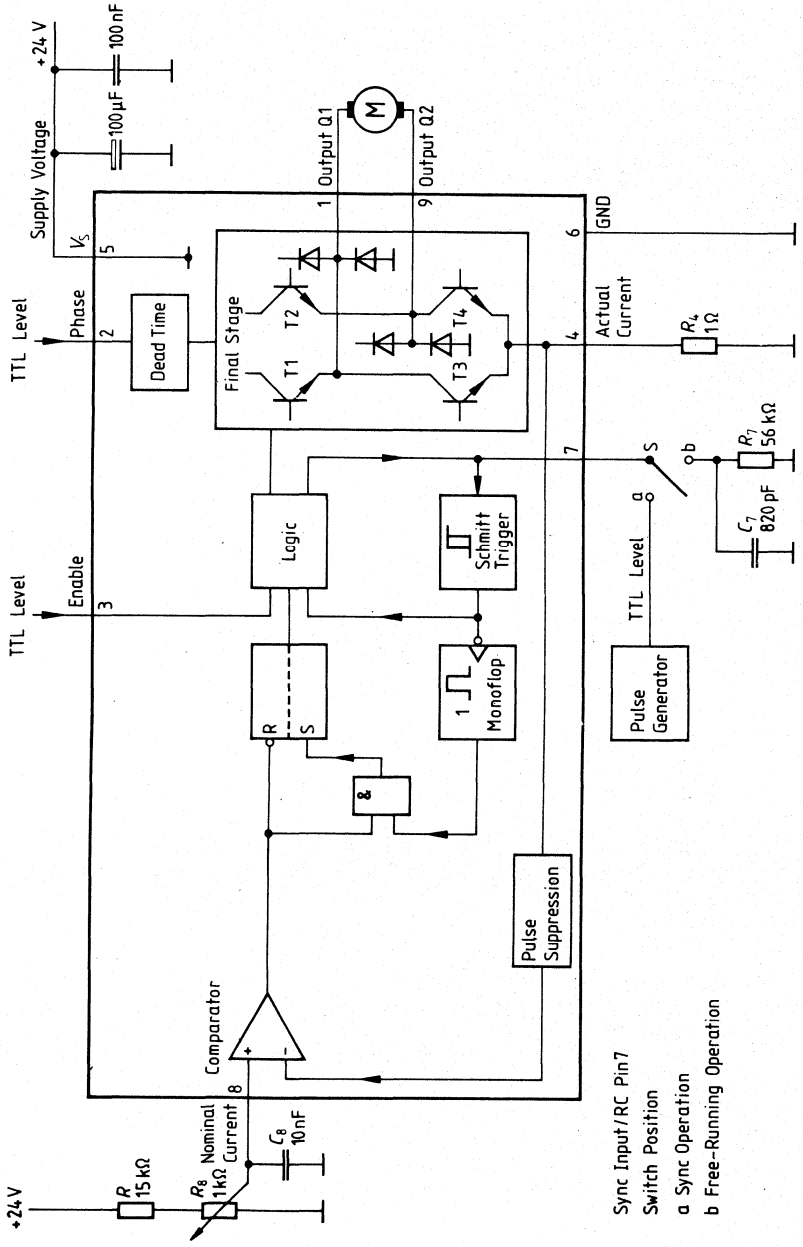
Pin	Symbol	Function
1	Q1	Output Q1
2 3		Phase input Enable input
4		Actual current
5	V_S	Supply voltage
6	0_S	GND
7 8	RC	Sync input/RC Nominal current input
9	Q2	Output Q2

The cooling fin is connected internally to pin 6 (ground).

TCA 1560 B

Pin	Symbol	Function
1	Q1	Output Q1
2 3		Phase Input Enable input
4		Actual current
5	V_S	Supply voltage
6	0_S	GND
7 8	RC	Sync input/RC Nominal current input
9	Q2	Output Q2
10-18		Ground (must be connected to pin 6)

Block Diagram



Circuit Description

Outputs

Outputs Q1, Q2 (pins 1, 9) are fed by push-pull output stages. The two integrated free-wheel diodes, referred to ground or supply voltage respectively, protect the IC against flyback voltages from an inductive load.

Enable

Outputs Q1 and Q2 are turned off when voltage $V_{I3} \leq 0.8$ V is applied to pin 3. The supply current then decreases maximally to 1 mA. The same occurs if pin 3 is open. The sink transistors are turned on when $V_{I3} \geq 2$ V.

Phase

The voltage at pin 2 determines the phase position of the output current. Output Q1 acts as sink for $V_{I2} \leq 0.8$ V and as source for $V_{I2} \geq 2$ V.

Similarly output Q2 acts as

sink when $V_{I2} \geq 2$ V and
source when $V_{I2} \leq 0.8$ V

The sink transistors are current-chopped. An internal circuit avoids undesired cross-over currents at phase change.

Nominal Current Input

The peak current in the motor winding is determined by the voltage at pin 8. A comparator compares this with the voltage drop at the actual current sensor at pin 4. If the nominal current is exceeded, the output sink transistors are turned off by a logic circuit.

Sync Input/RC

Outputs are turned on by a signal at pin 7. Two operation modes are possible: Synchronizing by a fed-in TTL signal or free running with the external RC combination.

Free-Running Operation

When the supply voltage is applied, capacitor C_7 at pin 7 charges to a limiting voltage, typically 2.4 V. With increasing current in the motor winding, the voltage rises at the actual current sensor R_4 (pin 4). After exceeding the predetermined value at the nominal current input (pin 8) the comparator, in conjunction with pulse suppression, resets an RS flipflop. The logic turns off sink transistors T3 and T4. C_7 ceases charging and the parallel resistance R_7 then discharges C_7. The sink transistors remain turned off until the lower threshold voltage of the Schmitt trigger is reached. This off period is thus controlled by the time constant $t_s = R_7 \times C_7$. After the lower trigger threshold has been passed, the monoflop is triggered by the falling edge of the Schmitt trigger output and, provided the voltage at the actual current sensor (pin 4) is lower than the nominal value at pin 8, the RS flipflop is reset. The logic circuit then turns on the sink transistors T3 or T4 and rechatges capacitor C_7. If the voltage at pin 4 rises above the comparator value at pin 8, the sink transistors T3 and T4 are turned off again. Turn-on cannot be repeated until capacitor C_7 has discharged to the lower trigger threshold, the discharge time being a function of R_7 and C_7.

Synchronous Operation

If a TTL level sync signal is fed to pin 7, the negative edge sets the RS flipflop, via the Schmitt trigger/monoflop combination, provided that the voltage at pin 4 is below the nominal value at pin 8. As in the free-running operation mode, the relevant output transistors become conducting. Similarly they are cut off by resetting the RS flipflop once the voltage at pin 4 is higher than the nominal value at pin 8.

Pulse Suppression

In all cases the pulse suppression circuit eliminates positive pulses, typically of 0.5 µs duration, at pin 4. These can result from cross-over currents in chopper operation through the integrated free-wheel diodes. As a result, the voltage at pin 4 rises well above the nominal value, and without pulse suppression this would lead to dynamic current limiting. The duration of these basically unavoidable cross-over currents is of the same order of magnitude as the reverse-recovery time of the free-wheel diodes.

Temperature Safeguard

If the temperature of the IC rises to approx. 150 °C, the final stages are turned off. At approx. 130 °C they are turned on again.

Logic Table

Enable		L	L	H	H
Phase		L	H	L	H
Output	Q1	/	/	L	H
Output	Q2	/	/	H	L
Transistor	T1	X	X	X	·
Transistor	T2	X	X	·	X
Transistor	T3	X	X	··	X
Transistor	T4	X	X	X	··

at:
$V_4 > 10$ mV
$R_4 > 0\ \Omega$

L = Low voltage level, input open
H = High voltage level
X = Transistor turned off
· = Transistor conducting
·· = Transistor conducting with current limiting turned on
/ = Output high-impedance

Maximum Ratings

$T_C = -25\,°C$ to $+85\,°C$

Description	Symbol	min	max	Unit
Supply voltage, pin 5	V_S	−0.3	45	V
Supply current, pin 5	I_S	0	2.5	A
Peak current in output transistors, pin 1, 9	I_Q	−2.5	2.5	A
Diode currents				
Diode to $+V_S$	I_{FH}		2.5	A
Diode to ground	I_{FL}		2.5	A
Input voltage, pins 2, 3, 7, 8	V_I	−0.3	6	V
Output current, pin 4	I_4	−2.5		A
Voltage, pin 4	V_4	−0.3	5	V
Ground current, pin 6	I_6		2.5	A
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−40	125	°C
Thermal resistance				
system – ambient	$R_{th\ SA}$		70	K/W
system – case	$R_{th\ SC}$		8	K/W

Operating Range

Supply voltage, pin 5	V_S	8	40	V
Package temperature	T_C	−25	85	°C
Input voltage, pins 2, 3, 7	V_I		5	V
Output current	I_Q	−2	2	A

Characteristics

$V_S = 24$ V; $T_C = 25$ °C

Description	Symbol	Test conditions	min	typ	max	Unit
Supply current, pin 5	I_S	$V_{I3} = V_{IH}$		18	30	mA
Supply current, pin 5	I_S	$V_{I3} = V_{IL}$		0.5	1	mA
Output, pins 1, 9						
Output voltage: source	V_{QH}	$\mid I_Q \mid = 1$ A		1.7	1.9	V
Output voltage: source	V_{QH}	$\mid I_Q \mid = 1.5$ A		1.9	2,1	V
Output voltage: sink	V_{QL}	$\mid I_Q \mid = 1$ A		1.2	1.4	V
Output voltage: sink	V_{QL}	$\mid I_Q \mid = 1.5$ A		1.5	1.7	V
Reverse current	$\mid I_{QS} \mid$				300	µA
Phase dead time	t_T	Figure 1	0.1	0.3	1.0	µs
Forward voltage of diodes to $+V_S$	V_{FH}	$I_{FH} = 1$ A		1.0	1.2	V
	V_{FH}	$I_{FH} = 1.5$ A		1.1	1.3	V
Forward voltage of diodes to ground	V_{FL}	$I_{FL} = 1$ A		1.1	1.3	V
	V_{FL}	$I_{FL} = 1.5$ A		1.3	1.5	V
Inputs: enable, pin 3 and phase, pin 2						
H input voltage	V_{IH}		2			V
L input voltage	V_{IL}				0.8	V
H input current	I_{IH}	$V_{IH} = 5$ V		50	100	µA
L input current	$-I_{IL}$	$V_{IL} = 0$ V			100	µA
Rise and fall time	t_r, t_f				2	µs
Nominal current, pin 8						
Control range	V_{I8}		0		2	V
Input current	$-I_{I8}$	$V_{I8} = 0$ V			5	µA
Input offset voltage	$V_{I\,(8-4)}$	Figure 5		0		mV
Actual current, pin 4						
Control range	V_{I4}	Figure 5	0		2	V
Turn-off delay	t_D	Figure 3		2	3	µs
Sync input/RC, pin 7						
Sync frequency	f	Duty cycle: 0.5	1		100	kHz
Duty cycle	D	$f = 40$ kHz	0.1		0.9	
Rise and fall time	t_r, t_f				2	µs
Output current, pin 7	$-I_{Q7}$		1.2	1.6	2.0	mA
Trigger threshold, pin 7	V_{L7}	Figure 2		0.6	0.8	V
Charging limit C_7	V_{G7}		2.2	2.4		V
Off period	t_{OFF}	Figure 4		64		µs
Dynamic input resistance pin 7	R_{I7}	$V_7 = 1.5$ V		1		kΩ

Maximum Ratings

$T_C = 25\,°C$ bis $+85\,°C$

Description	Symbol	min	max	Unit
Supply voltage, pin 5	V_S	−0.3	45	V
Supply current, pin 5	I_S	0	1.25	A
Peak current in output transistors, pins 1, 9	I_Q	−1.25	1.25	A
Diode currents, pins 1,9				
Diode against $+V_S$	I_{FH}		1.25	A
Diode against ground	I_{FL}		1.25	A
Input voltage, pins 2, 3, 7, 8	V_I	−0.3	6	V
Output current, pin 4	I_4	−1.25		A
Voltage, pin 4	V_4	−0.3	5	V
Ground current, pin 6	I_6		1.25	A
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−40	125	°C
Thermal resistance system – ambient	$R_{th\ SA}$		70	K/W
system – case (measured at pin 14)	$R_{th\ SC}$		15	K/W

Operating Range

Supply voltage, pin 5	V_S	8	40	V
Package temperature measured at pin 14	T_C	−25	85	°C
Input voltage, pins 2, 3, 7	V_I		5	V
Output current, pins 1, 9	I_Q	−1	1	A

Characteristics

$V_S = 24$ V; $T_C = 25$ °C

Description	Symbol	Test conditions	min	typ	max	Unit
Supply current, pin 5	I_S	$V_{I3} = V_{IH}$		18	30	mA
Supply current, pin 5	I_S	$V_{I3} = V_{IL}$		0.5	1	mA
Output, pins 1, 9						
Output voltage: source	V_{QH}	$\mid I_Q \mid = 0.5$ A		1.6	1.8	V
Output voltage: source	V_{QH}	$\mid I_Q \mid = 0.75$ A		1.65	1.90	V
Output voltage: sink	V_{QL}	$\mid I_Q \mid = 0.5$ A		1.0	1.2	V
Output voltage: sink	V_{QL}	$\mid I_Q \mid = 0.75$ A		1.1	1.4	V
Reverse current	$\mid I_{QS} \mid$				300	µA
Phase dead time	t_T	Figure 1	0.1	0.3	1.0	µs
Forward voltage of diodes to $+V_S$	V_{FH}	$I_{FH} = 0.5$ A		0.9	1.1	V
	V_{FH}	$I_{FH} = 0.75$ A		0.95	1.15	V
Forward voltage of diodes to ground	V_{FL}	$I_{FL} = 0.5$ A		0.95	1.15	V
	V_{FL}	$I_{FL} = 0.75$ A		1.0	1.2	V
Inputs: enable, pin 3 and phase, pin 2						
H input voltage	V_{IH}		2			V
L input voltage	V_{IL}				0.8	V
H input current	I_{IH}	$V_{IH} = 5$ V		50	100	µA
L input current	$-I_{IL}$	$V_{IL} = 0$ V			100	µA
Rise and fall time	t_r, t_f				2	µs
Nominal current, pin 8						
Control range	V_{I8}		0		2	V
Input current	$-I_{I8}$	$V_{I8} = 0$ V			5	µA
Input offset voltage	$V_{I\,(8\text{-}4)}$	Figure 5		0		mV
Actual current, pin 4						
Regulating range	V_{I4}	Figure 5	0		2	V
Turn-off delay	t_D	Figure 3		2	3	µs
Sync input/RC, pin 7						
Sync frequency	f	Duty cycle: 0.5	1		100	kHz
Duty cycle	D	$f = 40$ kHz	0.1		0.9	
Rise and fall time	t_r, t_f				2	µs
Output current, pin 7	$-I_{Q7}$		1.2	1.6	2.0	mA
Trigger threshold, pin 7	V_{L7}	Figure 2		0.6	0.8	V
Charging limit C_7	V_{G7}		2.2	2.4		V
Off period	t_{OFF}	Figure 4		64		µs
Dynamic input resistance pin 7	R_{I7}	$V_7 = 1.5$ V		1		kΩ

Internal Wiring of Pins

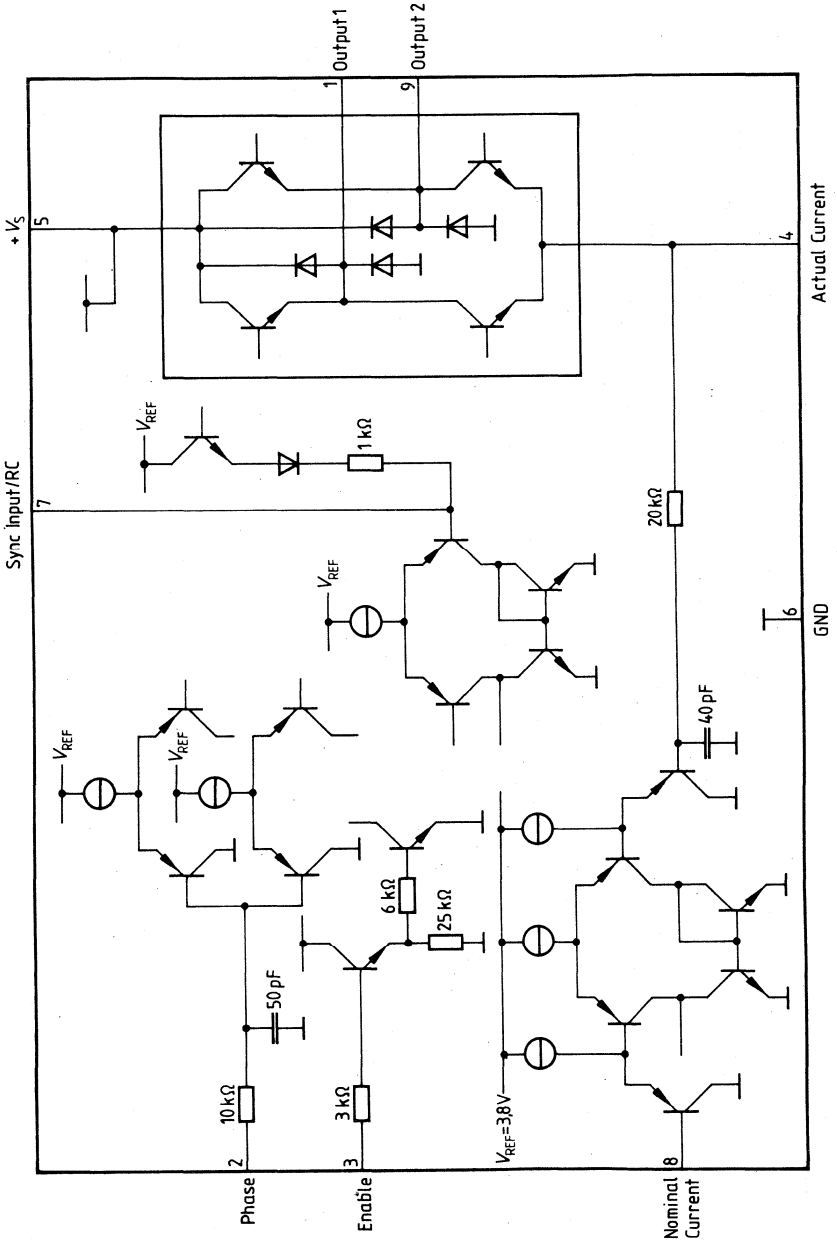


Figure 1
Phase Dead Time

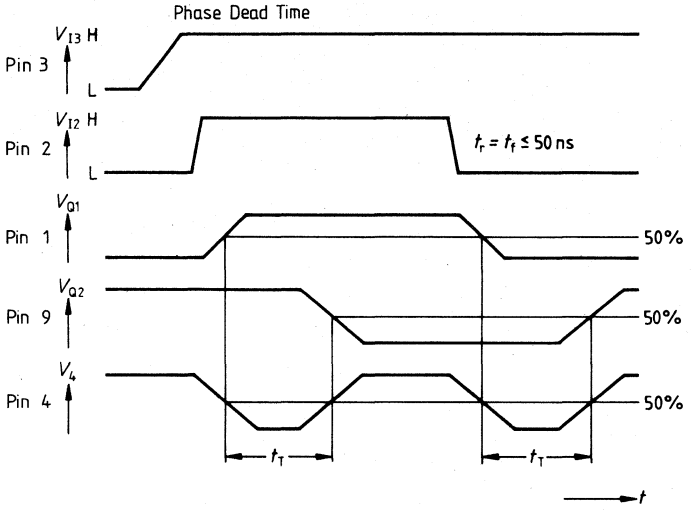


Figure 2
Trigger Threshold

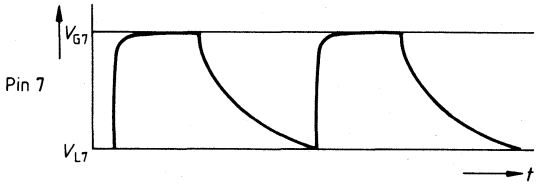


Figure 3
Turn-OFF Delay

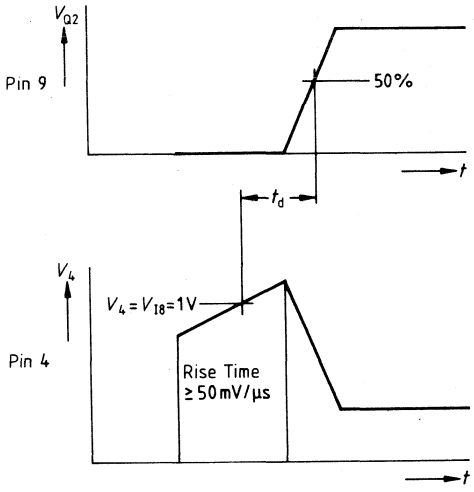


Figure 4
OFF Period versus Capacitance

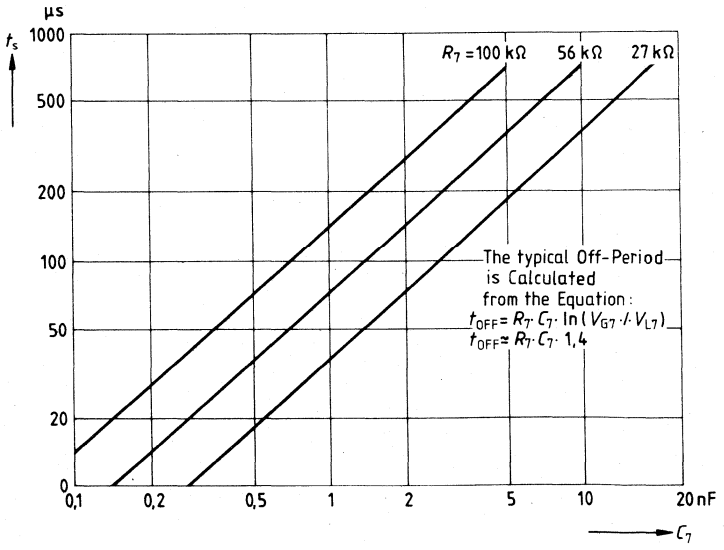
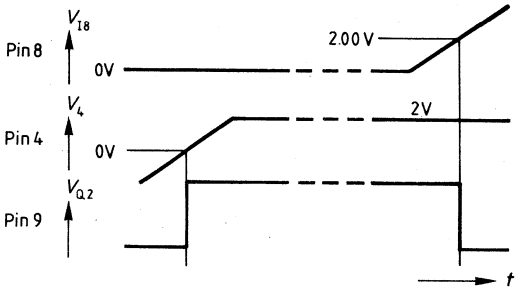
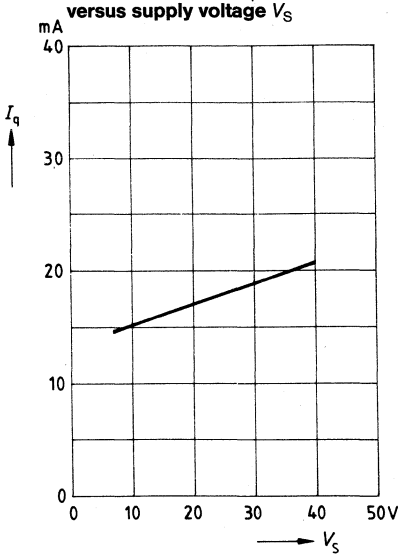


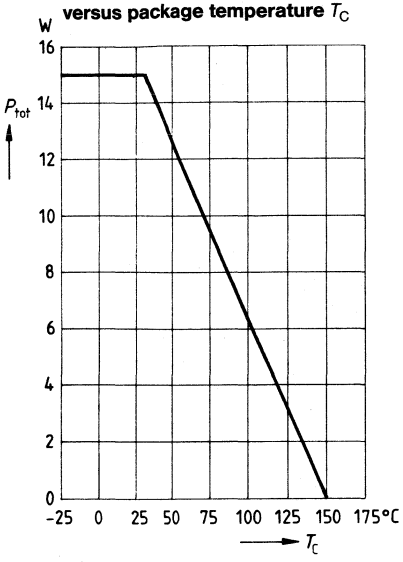
Figure 5
Control Range, Input Offset Voltage



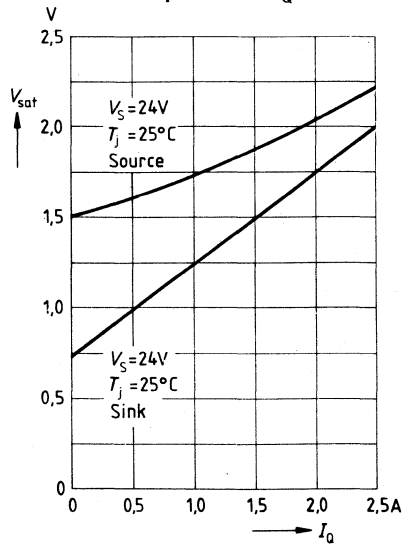
Quiescent current I_q versus supply voltage V_S



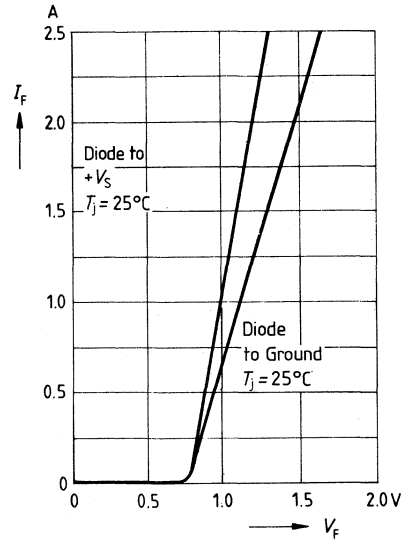
Permissible power dissipation P_{tot} versus package temperature T_C



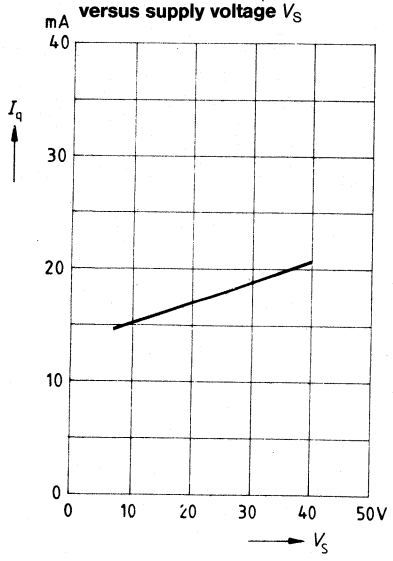
Output saturation voltages V_{sat} versus output current I_Q



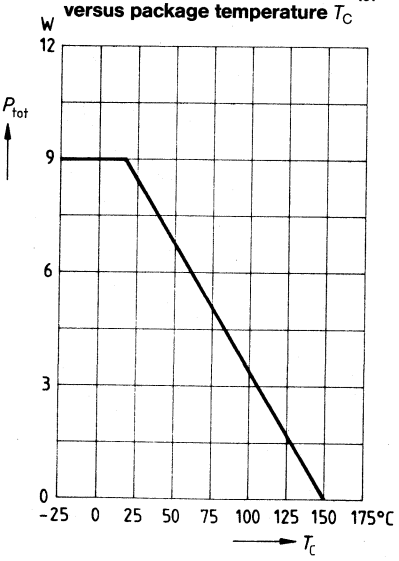
Forward current I_F of free-wheel diodes versus forward voltages V_F



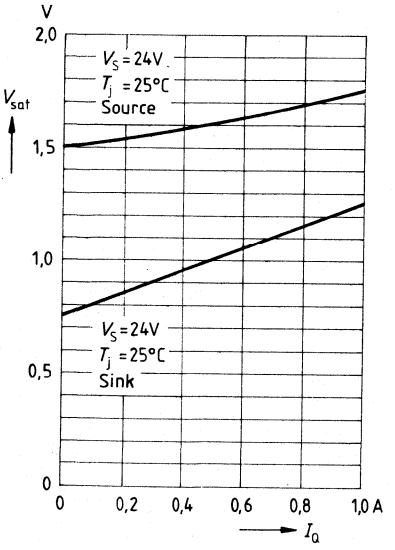
Quiescent current I_q versus supply voltage V_S



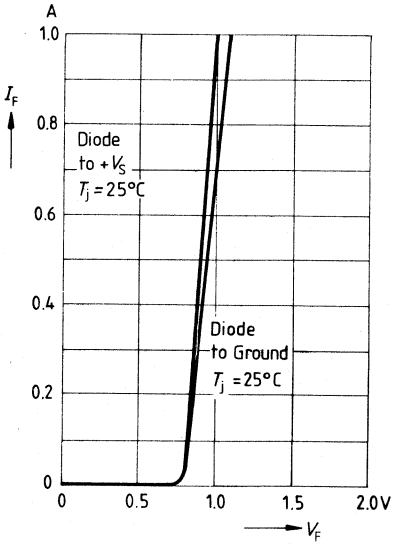
Permissible power dissipation P_{tot} versus package temperature T_C



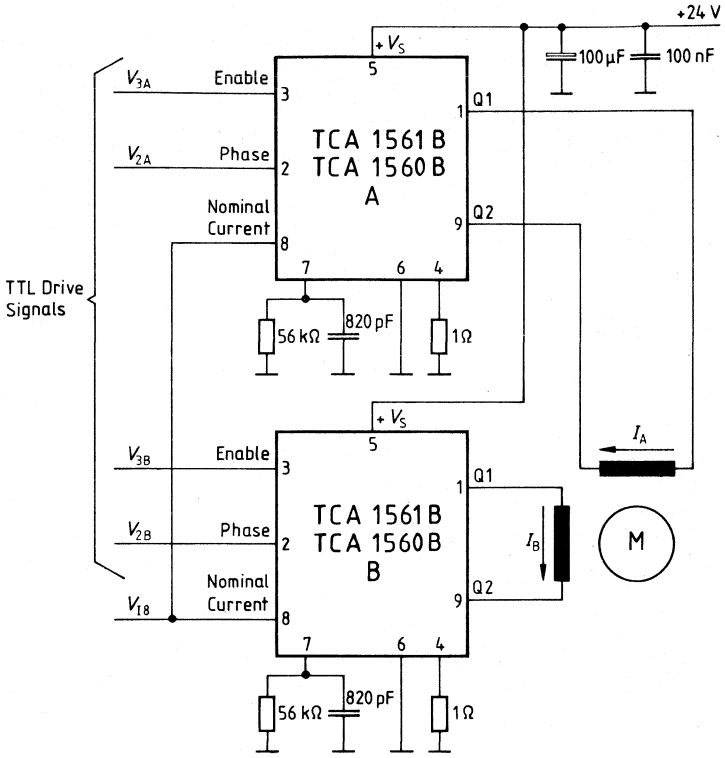
Output saturation voltages V_{sat} versus output current I_Q



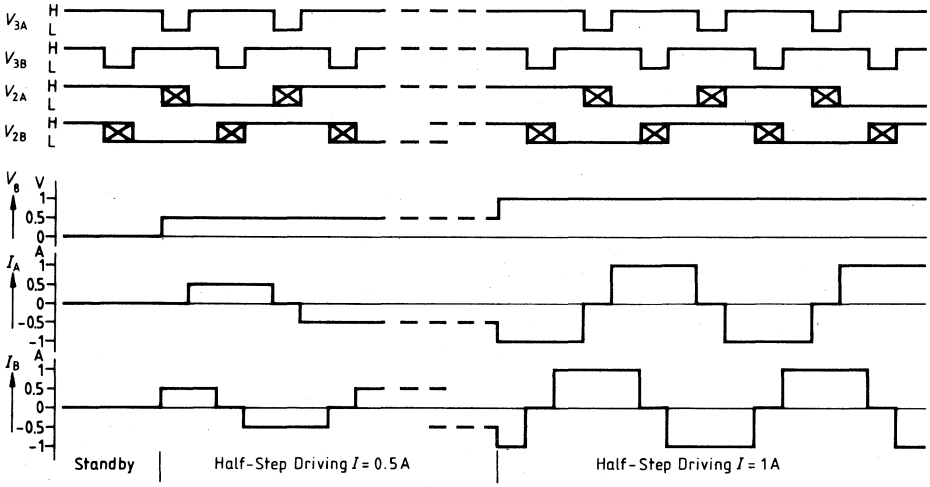
Forward current I_F of free-wheel diodes versus forward voltages V_F



Application Circuit



Pulse Diagram for Application Circuit



Calculation of Power Dissipation

The total power dissipation P_{tot} comprises

Saturation losses P_{sat}	(transistor saturation voltage and diode forward voltages)
Quiescent current losses P_q	(quiescent current multiplied by supply voltage)
Switching losses P_s	(turn-on/turn-off operation)

The following equations give the power dissipation for chopper operation without phase reversal. This can be regarded as "worst case", as, in addition to the switching losses, full-load current flows for the entire time.

$$P_{tot} = P_{sat} + P_q + P_s$$

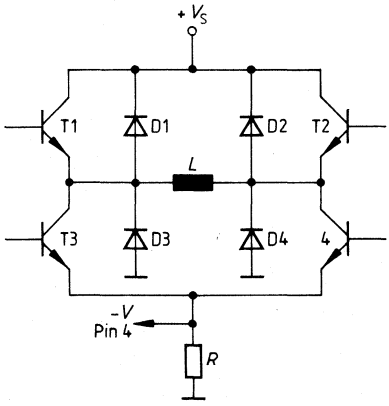
with

$$P_{sat} \simeq I_R \{ V_{satu} \cdot D + V_{Fo} (1 - D) + V_{sato} \}$$

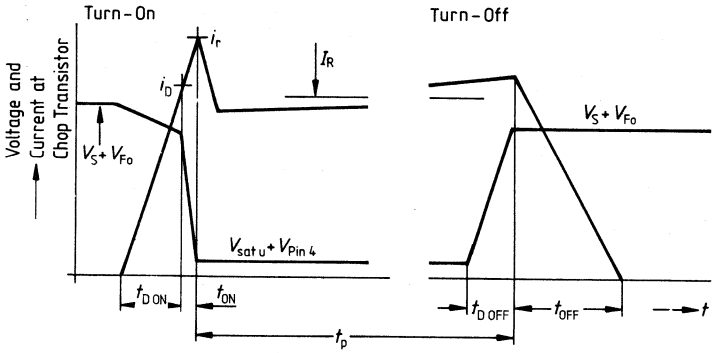
$$P_q = I_q \cdot V_S$$

$$P_s \simeq \frac{V_S}{T} \left\{ \frac{i_D \cdot t_{D\,ON}}{2} + \frac{(i_D + i_r)\, t_{ON}}{4} + \frac{I_R}{2} \left(t_{D\,OFF} + t_{OFF} \right) \right\}$$

I_R = Rated current (mean value)
I_q = Quiescent current
i_D = Reverse current during turn-on delay time
i_r = Peak reverse current
t_p = Conducting time of chop transistor
t_{ON} = Turn-on time
t_{OFF} = Turn-off time
$t_{D\,ON}$ = Turn-on delay time
$t_{D\,OFF}$ = Turn-off delay time
T = Cycle duration
D = Duty cycle t_p/T
V_{satu} = Saturation voltage of sink transistor (T3, 4)
V_{sato} = Saturation voltage of source transistor (T1, 2)
V_{Fo} = Forward voltage of free-wheel diode (D1, 2)
V_S = Supply voltage



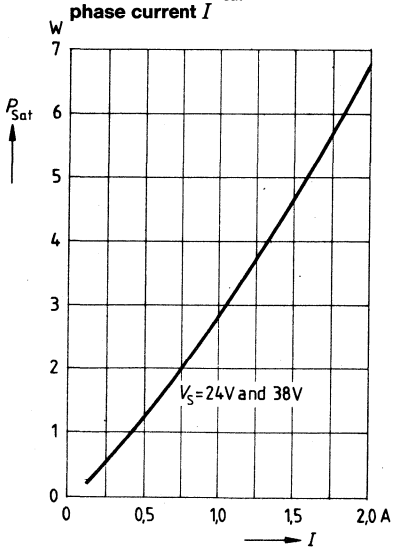
Calculation of Power Dissipation



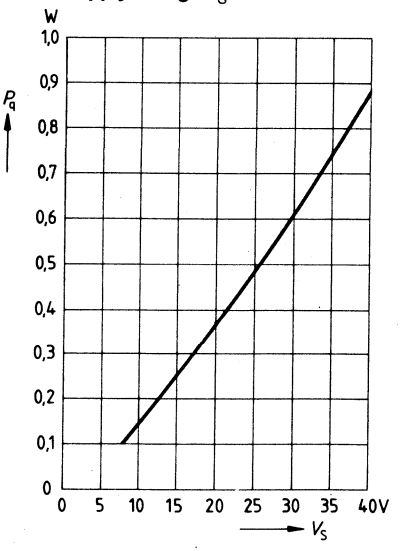
Characteristics for determining the typical power dissipation during chopper operation without phase reversal.

Parameters: $L_{load} = 10$ mH, $C_7 = 820$ pF; $R_7 = 33$ kΩ; $T_C = 25$ °C

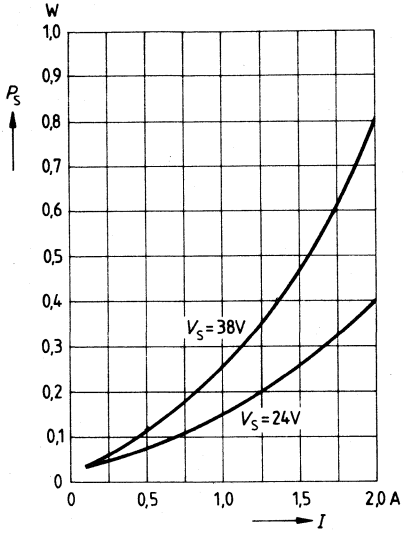
Saturation loss P_{sat} versus phase current I



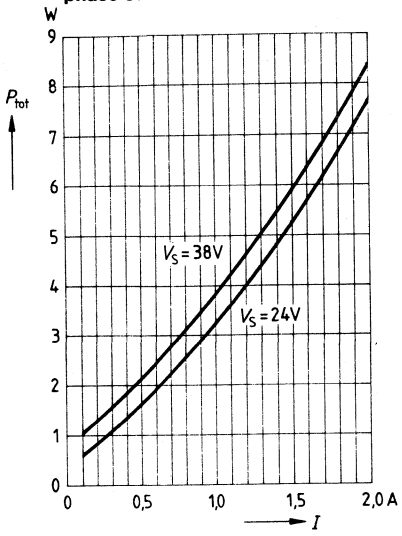
Quiescent current loss P_q versus supply voltage V_S



Switching loss P_S versus phase current I



Total power dissipation P_{tot} versus phase current I



Preliminary Data **MOS IC**

Type	Ordering Code	Package
SLE 4520	Q671000-H8271	P-DIP-28

Features

- Digital sine synthesis for controlling the speed of rotation and the torque of three-phase motors.
- 2-chip solution (e.g. SAB 8051 with SLE 4520) for easy configuration of a powerful frequency converter.
- Motor frequencies from 0 to 3000 Hz selectable at a switching frequency up to 23.4 kHz.
- Adaptation to different output stages through programmable dead time.
- Functional and performance features determined by dedicated software.

Application Notes

The new pulse-width modulator (PWM) converts an 8-bit data word into a rectangular signal of corresponding width.

Three independently operating channels consisting of a latch, loadable counter and zero detector are used for this purpose. Together with a microcontroller (e.g. SAB 8051) and suitable software, pulses are generated to drive ac converters and inverters (three-phase) with an almost unlimited range of waveforms (sinusoidal, triangular) and phase relationships. An oscillator with clock output, a programmable prescaler to adapt the switching frequency to the requirements of the output stage, an interlocking stage with status flipflop and the ability to program dead times are features that recommend the SLE 4520 for use in frequency converters to drive three-phase induction motors.

Speed control of three-phase motors is easily done when such motors are supplied with a three-phase voltage the V/f ratio of which is kept almost constant with variable frequency. For the generation of this three-phase voltage a frequency converter is required, which rectifies and filters the ac supply voltage and, subsequently, reconverts it into an ac voltage of another frequency the aid of a drive circuit and three power half-bridges. In order to avoid high losses the output stages operate in a switched mode and are driven by rectangular pulses which increase or decrease in width, depending on the waveform of the sinusoidal function. To produce such pulse with a repetition frequency (switching frequency) up to and above the audible range, a drive block consisting of the SAB 8051 microcontroller and the SLE 4520 PWM as a minimum configuration has proved to be best suited to the job.

Functional Description

The following description deals with the combination of the SAB 8051 microcontroller and the SLE 4520 PWM and a program developed by Siemens. Other hardware combinations are possible as well.

An on-chip oscillator directly feeds the programmable prescaler and has a buffered output for the connected microcontroller. The interface to the microcontroller has a width of 8 bits.

Data from the SAB 8051 microcontroller to the SLE 4520 PWM are transferred via the data bus P0 using the control signals $\overline{ALE}$ and $\overline{WR}$. In the PWM component three 8-bit registers for the three phases and two 4-bit registers for dead time and divider ratio respectively as well as an address decoder latch to buffer the relevant addresses are connected to the internal data bus of the SLE 4520 **(see block diagram)**.

Addresses are as follows:

Address	Register
00	8-bit register for phase 1
01	8-bit register for phase 2
02	8-bit register for phase 3
03	dead time control register
04	divider control register

The last two registers have to be written only once when being initialized. In the case of a controller output the above-mentioned 3-bit address is latched and decoded with the falling edge of the ALE clock. With the rising edge of the $\overline{WR}$ signal data are loaded from the bus into the registers of the pulse-width modulator.

The required divider ratio for the production of low switching frequencies at a simultaneously high operating frequency of the microcontroller is set by the divider control register. The divider control register is best loaded with an adequate value in the starting routine.

Allocation of value and divider ratio is shown in table 1:

Value	Divider ratio Counter	Divider ratio Delay clock
0	1 : 4	1 : 4
1	1 : 6	1 : 6
2	1 : 8	1 : 4
3	1 : 12	1 : 6
4	1 : 16	1 : 4
5	1 : 24	1 : 6
6	1 : 32	1 : 4
7	1 : 48	1 : 6

Table 1: Allocation of value in the divider register to the divider ratio by which the SLE 4520 operating frequency is selected.

After the ratio has been determined, the length of the switching frequency cycle should be selected in such a way that the maximum pulse width is just reached. This means that with a PWM counter clock of, e.g. 1 MHz (oscillator frequency of 12 MHz, divider ratio 1:12) and a table value of 127 (7 bits) the counter reaches zero after 128 µs (switching frequency cycle 128 µs).

Table 2 gives a number of useful allocations of counter frequency and switching frequency for the SAB 8051 (12 MHz clock).

Divider ratio	Counter frequency	Operating time Timer 0	Switching frequency	Resolution
1:6	2 MHz	64 µs	15.6 kHz	7 bit
1:6	2 MHz	128 µs	7.8 kHz	8 bit
1:12	1 MHz	128 µs	7.8 kHz	7 bit
1:12	1 MHz	256 µs	3.9 kHz	8 bit
1:24	500 kHz	256 µs	3.9 kHz	7 bit
1:24	500 kHz	2 x 256 µs	1.95 kHz	8 bit
1:48	250 kHz	2 x 256 µs	1.95 kHz	7 bit
1:48	250 kHz	4 x 256 µs	975 Hz	8 bit

Table 2: Allocation of counter frequency and switching frequency of SAB 8051

Converting a data word into a pulse width

Pulse generation in the three processing channels is done by a presettable 8-bit down-counter and a zero detector (NOR gate) which is connected to the eight counter outputs. With the transfer pulse from the microcontroller (width 1 instruction cycle), whose repetition rate determines the length of the switching frequency, the presettable counter is loaded with the contents of the appropriate register and 0 appears at the zero detector's output (provided the register does not contain 00H).

This 0 digit enables the counter and starts it running down. When zero is reached the pulse ends and the counter is stopped until the next transfer pulse arrives. The crystal frequency multiplied by the divider ratio serves as clock frequency for the PWM counter.

Functional Description

Dead-time control register and dead-time setting in order to avoid overlapping switching operations

The dead time between the drive pulses for the two transistors of a half-bridge must consider the storage times of the bipolar driver and the power transistors, otherwise dangerous overlapping switching operations might occur. In the pulse-width modulator the dead time is obtained by linking the pulse-width modulated signal source with a delay signal. The delay is obtained by passing the source signal through a 15-bit shift register with 15 outputs.

The shift pulse is either $f_{CRYSTAL}/6$ or $f_{CRYSTAL}/4$, depending on the values in the divider control register.

By writing a value between 0 and 0FH into the appropriate control register 16 dead times are presettable (incl. zero dead time)

The dead time depends on the crystal frequency and the preset divider ratio. Programmable dead times for a 12-MHz crystal frequency are shown in **table 3.**

Word in dead time memory	Divider ratio 1:4 dead time (µs)	Divider ratio 1:6 dead time (µs)
0	0	0
1	0.33	0.5
2	0.66	1
3	1.0	1.5
4	1.33	2
5	1.66	2.5
6	2.0	3
7	2.33	3.5
8	2.66	4
9	3.0	4.5
10	3.33	5
11	3.66	5.5
12	4.0	6
13	4.33	6.5
14	4.66	7
15	5.0	7.5

Table 3: Dead times presettable in the dead time control register using divider ratios of 1:4 and 1:6

Functional Description

The interface to the power circuit is provided by outputs PH1/1 to PH3/2

Without dead time PH1/2 is inverted to PH1/1, PH2/2 to PH2/1 and PH3/2 to PH3/1. The active switching state is Low.

With a programmed dead time the negative edges of the output signal are shifted to the right by the dead time.

The outputs are capable of directly driving TTL devices or optocouplers for voltage isolation of drive block and power circuit with a current up to 20 mA.

Static or dynamic interlocking of outputs is possible

Within the duration of the inhibit signal (pin 19) all six outputs can be set to high level. In case the outputs are connected to optocouplers the light emitting diodes are currentless and all six individual transistors of the power circuit are blocked. This option is particularly necessary when switching on the drive block, as proper pulses at the pulse-width modulator output are only available after the oscillator output has been built up and the initilization routine has been executed.

As the SAB 8051 sets the port outputs to high when switched on, only one port pin of the microcontroller has to be connected to inhibit. At the end of the initialization routine this port pin is set to low.

Another way of inhibiting the outputs (hold function) is to apply a high pulse to the Set input (pin 22) of the status flipflop. This inhibit state is indicated by the "Status" output (pin 20) and can be used to indicate or inform the microcontroller (active high; used, for example, in the event of power failure, short circuit, overtemperature etc.).

The status flipflop is cleared by a high pulse at the "Clear Status" input (pin 21).

Features

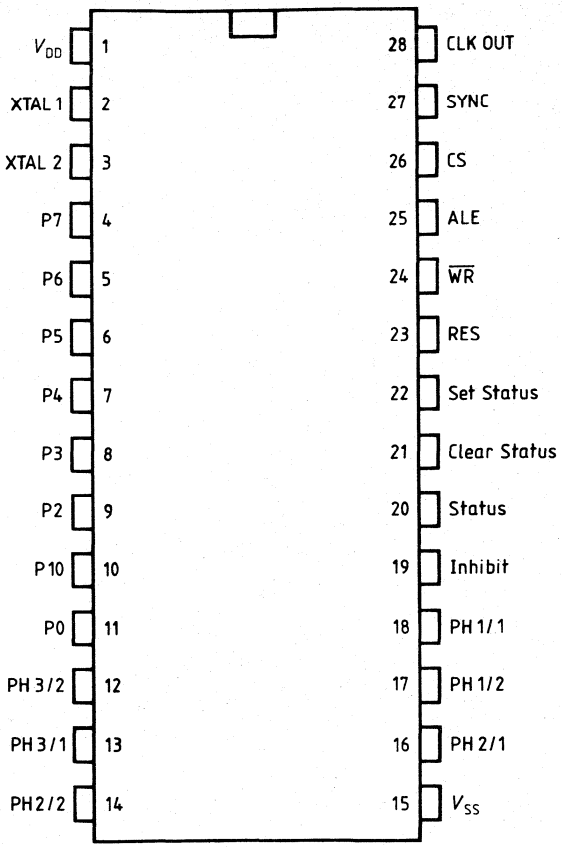
- Generation of three pairs of pulse-width modulated rectangular pulses (phase angle between one phase and the next is, for example, 120°) to drive six individual transistors of an inverter power block.
- Programmable dead time to reliably drive both power switches of a half-bridge from

  0 to 15 x $\frac{6}{f_{crystal}}$ or 15 x $\frac{4}{f_{crystal}}$ in 15 steps.

  It is the negative edge which is in each case delayed because the output signal is active low.
- Programmable divider in the pulse-width modulator to obtain low switching frequencies (for output stages with thyristors, GTOs, and bipolar transistors) and to simultaneously operate the microcontroller at higher crystal frequencies.
- Direct drive of an optocoupler interface to isolate control and load circuits (I_{sink} = 20 mA maximum).
- All six outputs of the SLE 4520 are set to high level either dynamically by an inhibit signal (INHIBIT) or statically by an R-S flipflop (SET STATUS). Thus blocking of all six individual transistors of the power circuit is possible.
- DC braking by selecting different, fixed duty cycles in the three output pairs.
- Direction of rotation is software-reversed by changing between two phases.
- Sine-wave frequency range about 0 to > 2600 Hz.
- Switching frequency range < 1 to > 20 kHz.
- 8-bit resolution of the desired sine-wave function with a switching frequency of $\frac{f_{crystal}}{6 \times 2^8}$

  or 7 bits with a switching frequency of $\frac{f_{crystal}}{6 \times 2^7}$ ($f_{crystal}$ = 12 MHz and resolution = 7 bits result in a 15.6 kHz switching frequency).
- Smallest increment of the pulse-width is 333 ns with $f_{crystal}$ = 12 MHz and divider ratio 1:4.
- Changing the switching frequency cycle in 1-µs steps allows the transition from one sine-wave frequency stage to the next quasi continuously (virtually analog).
- Evaluating the bit pattern at one port of the microcontroller enables many (256) different speed-control programs to be selected.
- Low current consumption of the pulse-width modulator due to ACMOS technology.

Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	V_{DD}	+5 V pin
2	XTAL1	Crystal pin
3	XTAL2	Crystal pin
4	P7	Data bus pins (inputs)
5	P6	
6	P5	
7	P4	
8	P3	
9	P2	
10	P10	
11	P0	
12	PH 3/2	Output phase 3 inverted
13	PH3/1	Output phase 3 normal (active low)
14	PH2/2	Output phase 2 inverted
15	V_{SS}	Ground
16	PH2/1	Output phase 2 normal (active low)
17	PH1/2	Output phase 1 inverted
18	PH1/1	Output phase 1 normal (active low)
19	INHIBIT	Inhibit (active high) sets all phase outputs to high
20	STATUS	Output of status flipflop
21	CLEAR STATUS	Resets status flipflop
22	SET STATUS	Sets status flipflop
23	RES	Chip reset
24	$\overline{WR}$	Input for $\overline{WR}$ pulse from microcontroller
25	ALE	Input for ALE clock from microcontroller
26	CS	Chip select
27	SYNC	Input for trigger pulse from microcontroller
28	CLK OUT	Output crystal frequency for microcontroller

Maximum Ratings

Description	Symbol	min	typ	max	Unit
Supply voltage	V_{DD}	−0.3		6	V
Input voltage	V_I	−0.3		V_{DD}+0.3	V
Storage temperature	T_{stg}	−50		125	°C
Total power dissipation	P_{tot}			500	mW
Power dissipation per output	P_Q			50	mW

Operating Range

Supply voltage	V_{CC}	4.5	5	5.5	V
Supply current (outputs not connected)	I_{DD}			15	mA
Operating frequency	f_{CLK}			12	MHz
Ambient temperature	T_A	−40		85	°C

DC Characteristics

$T_A = 25\,°C$

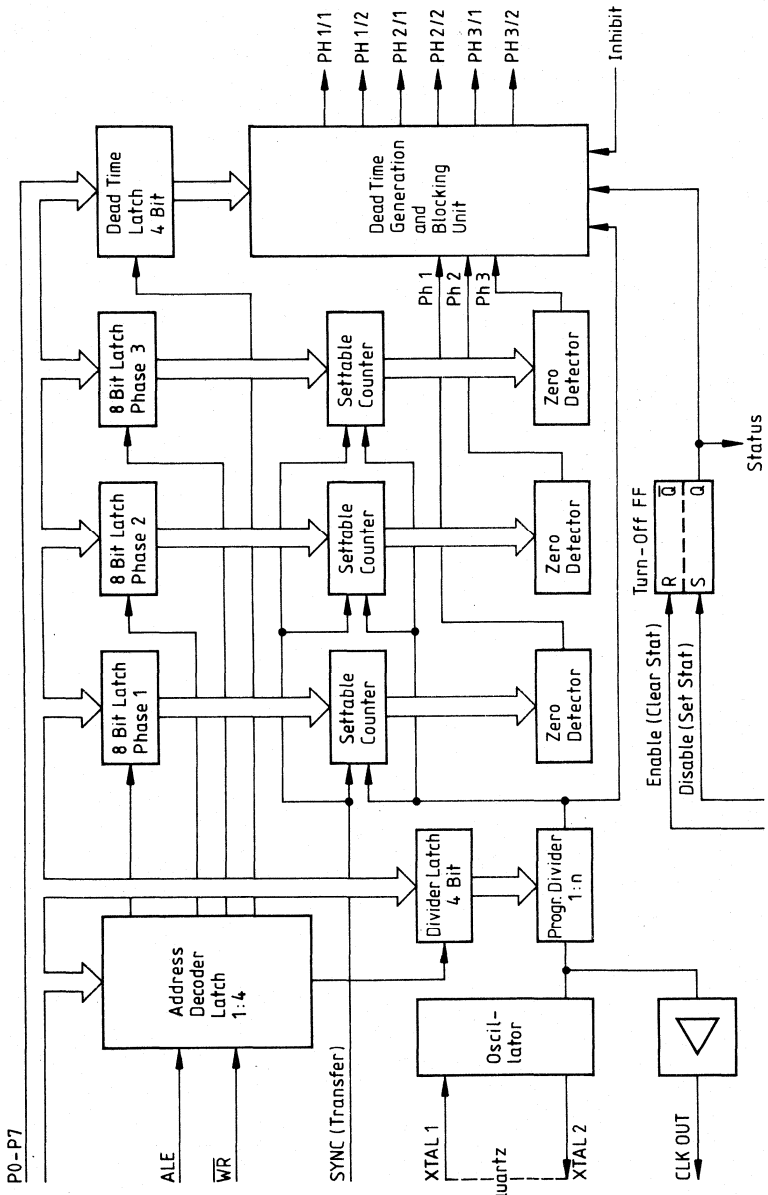
Description	Symbol	Measuring conditions	min	typ	max	Unit
All input signals except XTAL2						
H input voltage	V_{IH}		2.2		V_{DD}	V
L input voltage	V_{IL}		0		0.8	V
Input capacitance	C_I				10	pF
Input current	I_{IL}				1	µA
Input signal XTAL2 for external clock						
H input voltage	V_{IH}		4.0			V
L input voltage	V_{IL}		0		0.3	V
Input capacitance	C_I				10	pF
Input current	I_{IL}				1	µA
Output signals STATUS, CLK OUT						
H output voltage	V_{QH}	$I_Q = 0.5$ mA	$V_{DD}-0.8$			V
L output voltage	V_{QL}	$I_Q = 1.6$ mA			0.4	V
Output Signals PH1/1, PH1/2, PH2/1, PH2/2, PH3/1, PH3/2						
L output voltage	V_{QL}	$I_Q = 20$ mA			1	V
H output voltage	V_{QH}	$I_Q = 1$ mA	$V_{DD}-0.8$ V			V

AC Characteristics

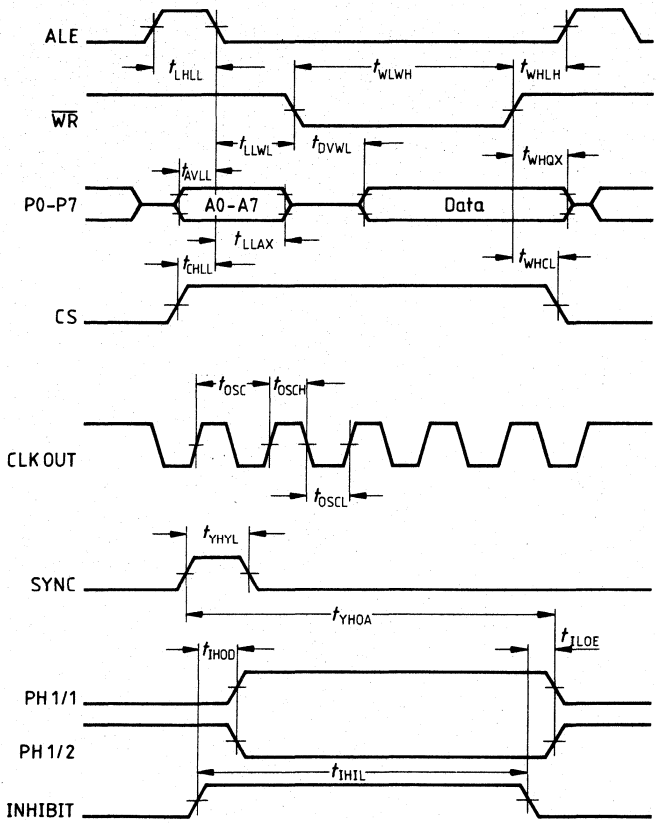
Symbol	Parameter	min	max	Unit
t_{LHLL}	ALE pulse width	100		ns
t_{AVLL}	Address setup to ALE	30		ns
t_{LLAX}	Address hold after ALE	30		ns
t_{WLWH}	WRN pulse width	200		ns
t_{WHLH}	WRN high to ALE high	50		ns
t_{DVWL}	Data setup after WRN low	20		ns
t_{LLWL}	ALE low to WRN low	100		ns
t_{WHQX}	Data hold after WRN[1])	30		ns
t_{OSC}	Oscillator period	83		ns
t_{OSCH}	High time	35		ns
t_{OSCL}	Low time	35		ns
t_{YHYL}	SYNC pulse width	200		ns
t_{ILOE}	INHIBIT low to output enable		100	ns
t_{YHOA}	Delay between SYNC high to output active	4 t_{OSC}	97 t_{OSC} + 20	ns
t_{CHLL}	Chip select setup to ALE low	20		ns
t_{WHCL}	Chip select hold after WRN high	30		ns
t_{RHRL}	Reset pulse width	12 t_{OSC}		ns
t_{SHSL}	Set Status pulse width	200		ns
t_{CHCL}	Clear Status pulse width	200		ns
t_{IHOD}	INHIBIT high to output disable		100	ns
t_{SHOD}	Set Status high to output disable		100	ns
t_{CHOD}	Clear Status high to output enable		100	ns
t_{SHTH}	Set Status pulse length	100		ns
t_{CHTL}	Clear Status pulse length	100		ns
t_{IHIL}	Inhibit pulse length	100		ns

[1]) If t_{WLWH} is less than 2 t_{OSC} + 20 ns, then t_{WHQX} is 50 ns

Block Diagram



Pulse Diagrams



Type	Ordering Code	Package
TCA 955	Q67000-A983	P-DIP-16
TCA 955 K	Q67000-A983-K	MIKROPACK 16 pins (SMD)

The TCA 955 is suited for the speed control of dc motors. The principle corresponds to a clocked control. Outstanding features are its high control accuracy, its large supply voltage range, and the possible current saving. Additionally, the IC features a battery voltage indicator.

Typical Applications

Speed control in

- Tape recorders
- Cassette recorders
- Record players
- Movie Cameras
- Control system drivers

Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage Supply voltage (pin 11 and pin 15 connected)	V_S V_S	16 6	V V
Output current pin 16 Output current pin 12 (LED output)	I_Q $I_{Q\ LED}$	200 15	mA mA
Power dissipation, LED output	$P_{Q\ LED}$	150	mW
Junction temperature Storage temperature range	T_j T_{stg}	125 −55 to 125	°C °C
Thermal resistance system – air	$R_{th\ SA}$	85	K/W

Operating Range

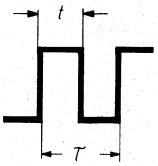
With internal short-circuit stabilization (pin 11 and pin 15 connected)	V_S	2 to 6	V
With internal stabilization (V_S to pin 15)	V_S	4.8 to 16.0	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = 2.2$ V to 16.0 V; $T_A = 25$ °C

Description	Symbol	min	typ	max	Unit
Controller					
Current consumption $V_S = 4.8$ V $V_S = 16$ V	I_S I_S		8.3 15.5	12.0 24.0	mA mA
Stabilized voltage $V_S = 4.8$ to 16 V	V_{stab}	2.75	3.00	3.30	V
Input threshold (pin 3) to ground Hysteresis of input threshold Offset voltage (pin 3 to pin 2)	 V_I ΔV_I V_{offset}	 0.46 x V_{11}	 0.485 x V_{11} 0.015 x V_{11} 11	 0.51 x V_{11} 0.03 x V_{11} 20	 V V mV
Input current (pin 3)	I_I			1	µA
Output transistor saturation voltage $I_Q =$ 50 mA $I_Q = 100$ mA	 $V_{Q\,sat}$ $V_{Q\,sat}$		 0.84 0.92	 1.00 1.25	 V V
Output transistor cutoff current	$I_{Q\,H}$			30	µA
Duty cycle – control range[1])	D	0		1	
Rated rpm[2])	n	$\frac{12.55}{p \cdot R_1 \cdot C_2}$	$\frac{14.85}{p \cdot R_1 \cdot C_2}$	$\frac{17.64}{p \cdot R_1 \cdot C_2}$	rpm
Error in rpm with duty cycle control[3]) from 0 to 1				$\frac{0.224}{N \cdot p \cdot C_3}$	%
Switching Oscillator					
Frequency	f		$\frac{1}{0.4 \cdot R_2 \cdot C_4}$		Hz
Average voltage pin 10 Voltage pin 11 peak to peak $V_{Q\,OSC}$	$V_{Q\,OSC}$		0.48 x V_{11} 0.18 x V_{11}		V V

[1]) Duty cycle



$D = \frac{t}{T}$

[2]) p = number of pole pairs of the tachometer generator.
[2]) in applications without switching oscillator.

Description	Symbol	min	typ	max	Unit
Battery Voltage Indicator					
Threshold voltage	$V_{I\,ON}$ $V_{I\,OFF}$	1.0		1.5	V V
Hysteresis	V_{hy}		220		mV
Input current	I_I			0.2	µA
Saturation voltage LED output[1])	$V_{Q\,LED}$			0.5 + 500 x I_{LED}	V

Formulae

Rate rpm $n = \dfrac{14.85}{p \cdot R_1 \cdot C_2}$ [rpm]

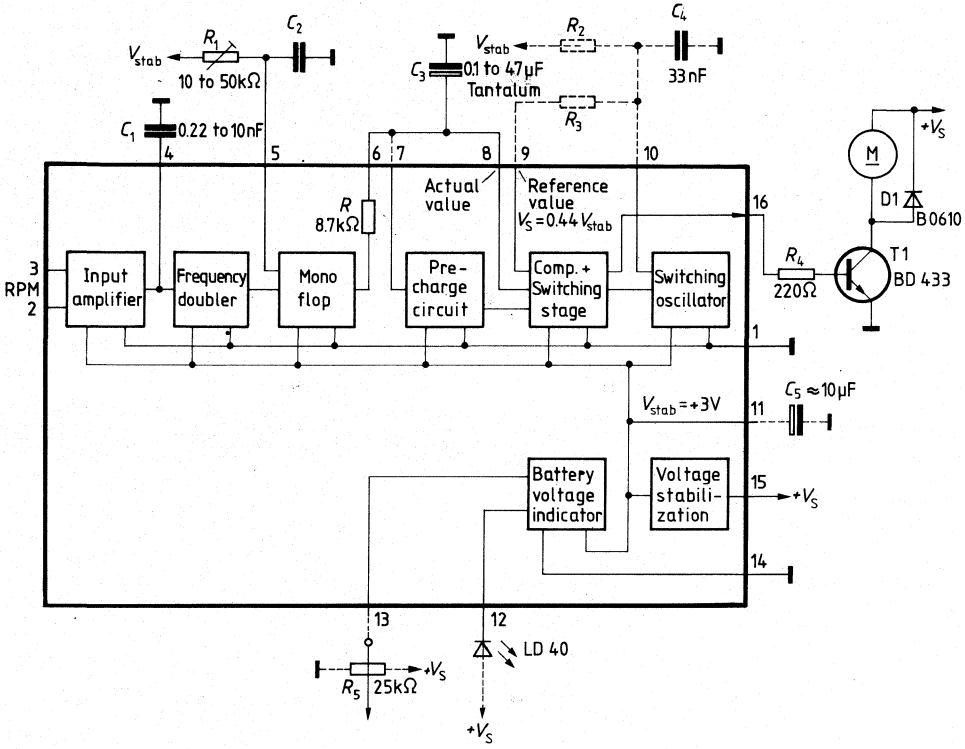
Switching frequency $f = \dfrac{n \cdot p}{30}$ [Hz]

in operation without switching oscillator.

Reference value $V_{REF} = 0.44 \times V_{11}$ [V]
Precharging voltage at C_3 $V_F = 0.87 \times V_{REF}$ [V]
(pin 6 and pin 7 connected)

[1]) A protective resistor of 500 Ω ± 20% is integrated inside the IC.

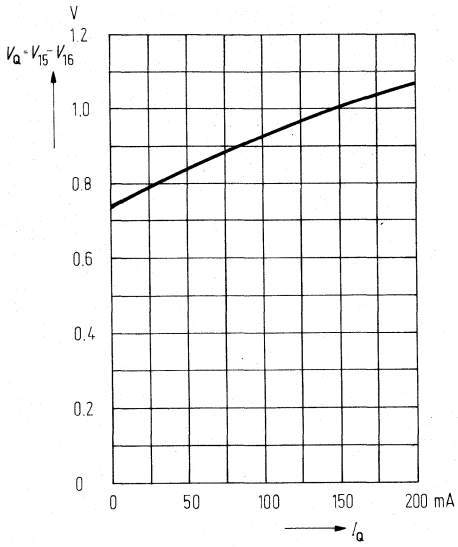
Block Diagram for Speed Control with TCA 955



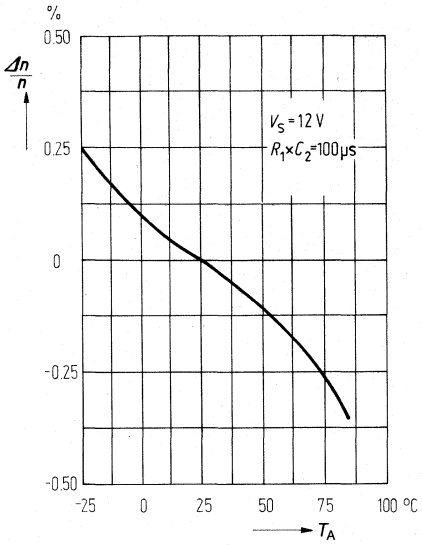
Dimensioning Notes

1. The internal voltage stabilization offers the following advantages:
   — operation with highly varying supply voltage,
   — wide range of supply voltage.
2. In order to receive pulses with a steady duty cycle at the output, symmetrical pulses must be applied to the input.
3. It is recommended to use multipole tachometer generators as this improves the accuracy of control and possibly the power consumption.
4. The power consumption can considerably be reduced by means of the switching frequency oscillator at low electric motor time constants.
5. Higher accuracy can be obtained by using a second-order filter instead of C_3.
6. When using rapidly starting motors, the precharge circuitry reduces overshoots.

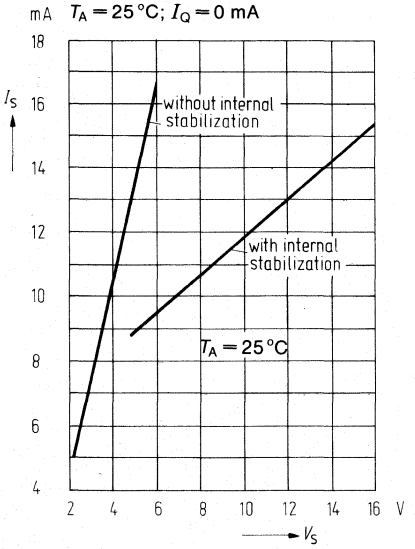
Saturation voltage of output transistor
Output voltage versus output current



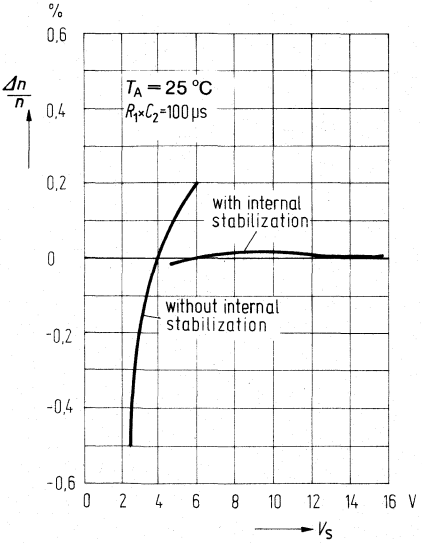
Rpm versus ambient temperature
$V_S = 12$ V; $R_1 \times C_2 = 100$ µs



Current consumption
versus supply voltage
$T_A = 25$ °C; $I_Q = 0$ mA



Rpm versus supply voltage
$T_A = 25$°C; $R_1 \times C_2 = 100$ µs



Intelligent Low-Side Drivers

Selector Guide

Features	Type	
	TLE 4211	**TLE 4214**
Max. current	2 x 2 A	2 x 0.5 A
Operating range V_S	5–32 V	6–25 V
Max. voltage V_S	70 V	70 V
Protection against reverse polarity	±45 V	
Error monitoring	Overload Open circuit Short-circuit to ground Overvoltage	Overload Open circuit Short-circuit to ground Overvoltage Overtemperature
Typ. saturation voltage at I_{max}	0.6 V	0.6 V
Temperature range	−40 °C to +125 °C	−40 °C to +100 °C
Package	P-T66-7-H	P-DIP-8

Preliminary Data **Bipolar IC**

Type	Ordering Code	Package
TLE 4211	Q67000-A8118	P-T66-7-H

Features

- Double low-side driver, 2 x 2 A
- Protection against reverse polarity
- Power limitation
- Temperature monitoring
- Voltage proof up to 70 V
- Integrated power Z diodes
- Error feedback
- Temperature range from −40 °C to +125 °C
- Suitable for applications in automotive electronics
- Short-circuit proof

Application Notes

Applications in industrial electronics require intelligent power switches activated by logic signals, which are also short-circuit proof and provide for error feedback.

The IC contains two of these power switches (low-side driver). In case of inductive loads the integrated power Z diodes clamp the self-induction voltage.

Through TTL signals at the control inputs (active low) both switches can be activated independently of one another. If one of the inputs is not in use, it must be applied to high potential.

The status output (open collector) signals the following malfunctions through low potential:

- Overload
- Underload
- Short-circuit to ground
- Overvoltage

Circuit Description

Input Circuits

The control inputs comprise TTL-compatible Schmitt triggers with hysteresis. Driven by these stages the inverting buffer amplifiers convert the logic signal for driving the NPN power transistors.

Switching Stages

The output stages comprise NPN power transistors with open collectors. Since the protective circuit allocated to each stage limits the power dissipation, the outputs are short-circuit proof to the supply voltage throughout the entire operating range. Positive voltage peaks, which occur during the switching of inductive loads, are limited by the integrated power Z diodes.

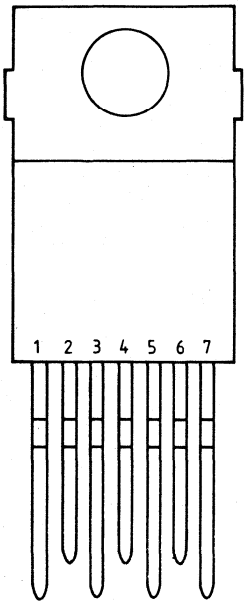
Monitoring and Protective Functions

The outputs are monitored for underload (open circuit), overload, and short-circuit to ground (see table below). In addition, large sections of the circuit are de-activated in case of excessive supply voltages V_S. Linked via OR gate the information regarding these malfunctions effects the status output (open collector, normally high). An internally determined dead time applied to all malfunctions but overvoltage prevents the output of messages in case of short-term malfunctions. Furthermore, a temperature protection circuit prevents thermal destruction. An integrated reverse diode protects the supply voltage V_S against reverse polarities. Similarly the load circuit is protected against reverse polarities within the limits established by the maximum ratings (no short circuit of the load at the same time!). At supply voltages below the operating range an undervoltage detector ensures that neither the status nor the outputs are activated.

Status Output (L = Error)

	Undervoltage	**Operating range**		**Overvoltage**
		L (active)	H (passive)	
Standard operation	H	H	H	L
Overload	H	L	H	L
Underload	H	L	H	L
Short circuits to ground	H	L	L	L

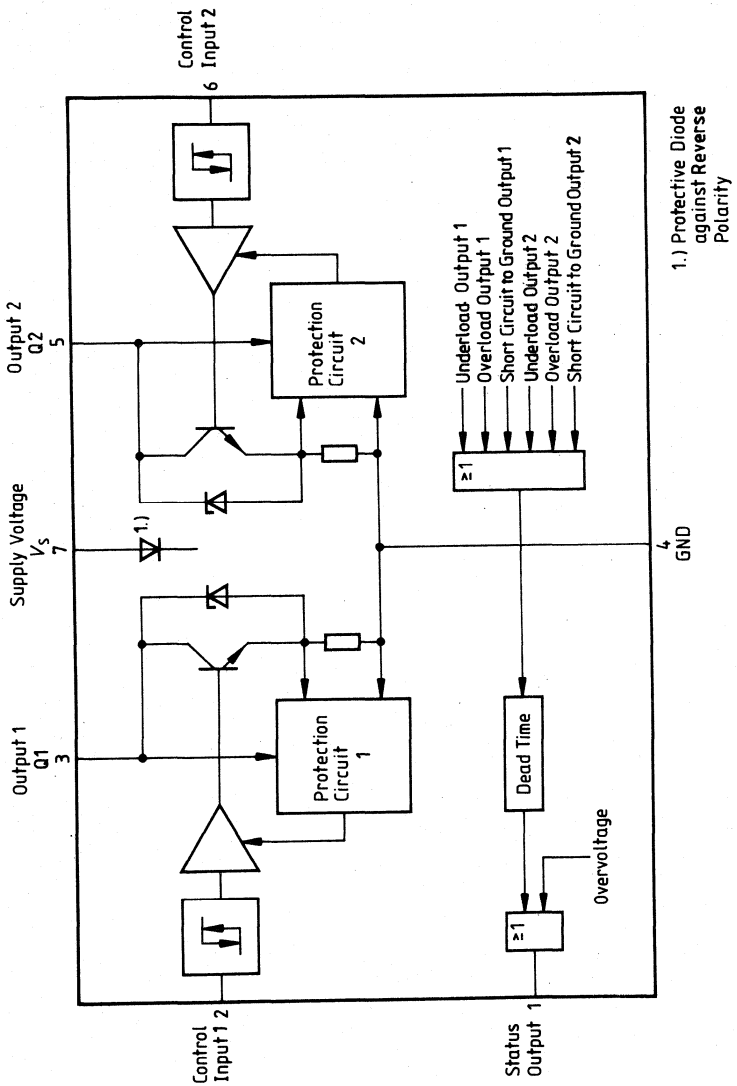
Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	Q STA1	**Status output (open collector)** for both outputs; indicates overload, underload and short-circuits to ground as well as overvoltage at pin 7. In case of malfunction the status output is switched to low after a defined dead time (except overvoltage)
2	I Control 1	**Control input 1 (TTL-compatible)** activates output transistor 1 in case of low-potential
3	Q 1	**Output 1** Short-circuit proof, open collector output with 36 V power Z diode to ground
4	GND	**Ground** Wiring must be designed for a max. short-circuit current (2 x 2.8 A)
5	Q 2	**Output 2** Short-circuit proof, open collector output with 36 V power Z diode to ground
6	I Control 2	**Control input 2 (TTL-compatible)** activates output transistor 2 in case of low-potential
7	V_S	**Supply voltage** In case of overvoltage at this pin large sections of the circuit are de-activated. The status output indicates the malfunction without dead time.

Block Diagram



Maximum Ratings

$T_C = -40\,°C$ to $+125\,°C$

Description	Symbol	min	max	Unit
Voltages				
Supply voltage (pin 7)[1]	V_S	−45	45	V
Supply voltage (pin 7) $t \leq 500$ ms	V_S		70	V
Input voltage (pin 2; pin 6)	V_I	−5	45	V
Output voltage (pin 1)	V_Q	−0.3	45	V
Currents				
Switching current (pin 3; pin 5) internally limited	I_Q			
Current with reverse polarity (pin 3; pin 5) $T_C \leq 85\,°C$	I_Q	−2.8		A
Ground current (pin 4) $T_C \leq 85\,°C$	I_{GND}	−5.6	5.6	A
Output current (pin 1)	I_O		10	mA
Switching energy at inductice load	E		50	mJ
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−50	150	°C
Operating Range				
Supply voltage[2]	V_S	5.0	32	V
Case temperature	T_C	−40	125	°C
Thermal resistance				
system – case	$R_{th\,SC}$		5	K/W
system – air	$R_{th\,SA}$		65	K/W

[1] Refer to page 737: monitoring and protective functions
[2] Lower limit = 4.2 V, if previously V_S greater than or equal to 5 V (turn-on hysteresis)

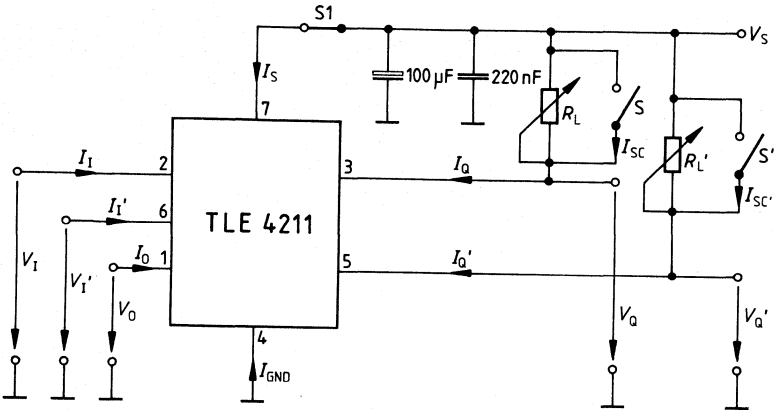
Characteristics

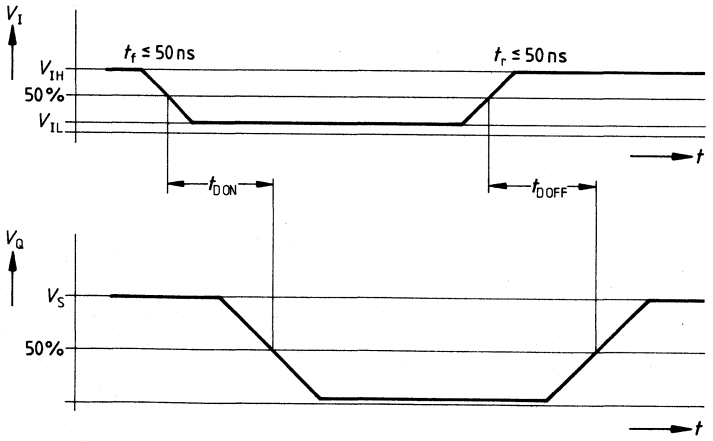
$T_C = 25\,°C$ and $V_S = 12\,V$

Description	Symbol	Measuring conditions	min	typ	max	Unit
General characteristics						
Quiescent current	I_q	$V_I = V_I > V_{IH}$		2	4	mA
Quiescent current	I_q	$V_I = V_I < V_{IL}$		80	120	mA
Overvoltage threshold	V_{SO}	$I_O = 5\,mA$; $V_O < 0.4\,V$	34	36	40	V
Underload voltage switching threshold	V_{QU}	$I_O = 5\,mA$; $V_O < 0.4\,V$		20		mV
Underload current	I_{QU}	$V_Q = V_{QU}$			50	mA
Logic						
Control input H input voltage L input voltage	 V_{IH} V_{IL}		 2.0		 1.0	 V V
Hysteresis of input voltage	ΔV_I			0.7		V
H input current	I_{IH}	$V_I = 5\,V$			10	µA
L input current	$-I_{IL}$	$V_I = 0.5\,V$			10	µA
Status output (open collector) L saturation voltage	 V_{QSat}	 $I_Q = 5\,mA$			 0.4	 V
Status dead time	t_{dS}	[1]	12	20	30	µs
Switching stages						
Saturation voltage	V_{QSat}	$I_Q = 2\,A$; $V_I = V_{IL}$		0.6	0.8	V
Short-circuit current	I_{SC}	$V_Q = V_S$; $V_I = V_{IL}$	2.2	2.5		A
Leakage current	I_Q	$V_Q = V_S$; $V_I = V_{IH}$			300	µA
Switch-on time	$t_{D\,ON}$	see fig. 1; $R_L = 5.6\,\Omega$		5	10	µs
Switch-off time	$t_{D\,OFF}$	see fig. 1; $R_L = 5.6\,\Omega$		5	10	µs
Forward voltage of substrate diode	V_{QF}	$I_Q = -2.0\,A$		1.2	1.5	V
Power Z diode ($V_S = 40\,V$; S_1 open)						
Z voltage	V_Q	$I_Q = 0.1\,A$	34	36	38	V
Internal impedance	R_Z	$0\,A < I_Q < 2\,A$		2		Ω

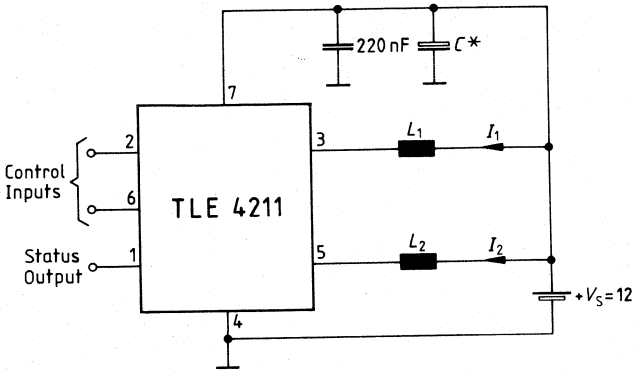
[1] Period from the beginning of the disturbance at one channel (exception: overvoltage) until the 50% value of the status switching edge is reached.

Measuring Circuit



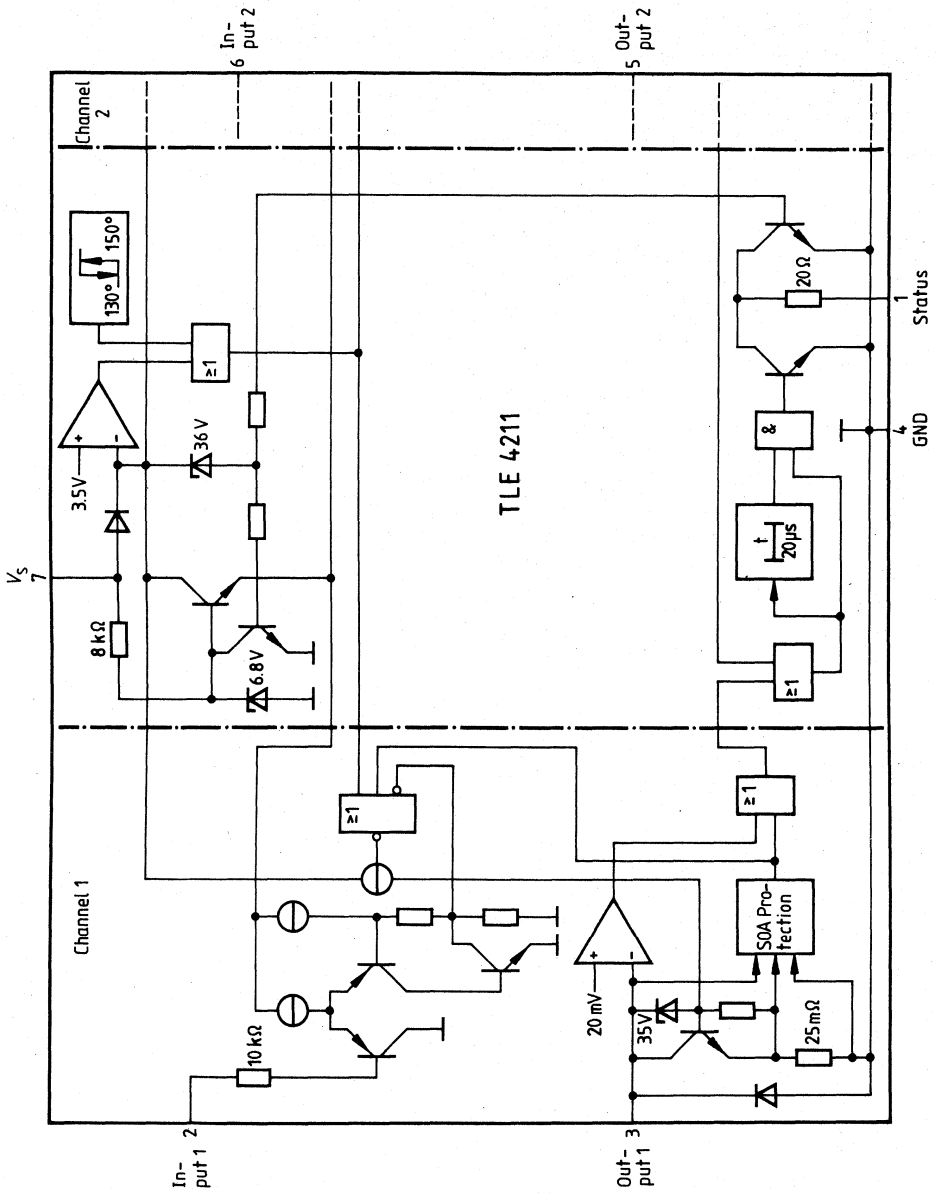


Application Circuit

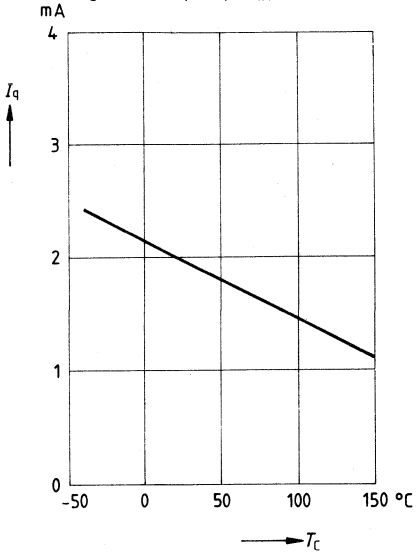


$C^* \geq (L_1 I_1^2 + L_2 I_2^2) / (45\,V - V_S)^2$

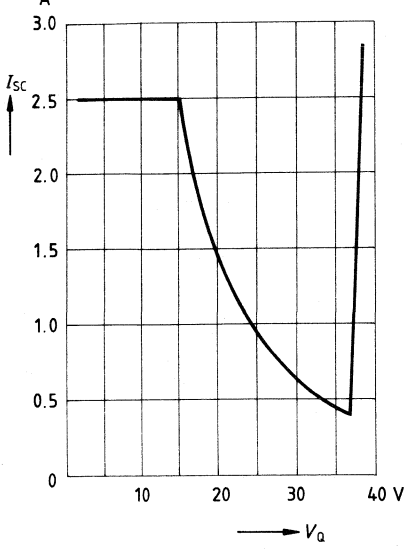
Block Diagram



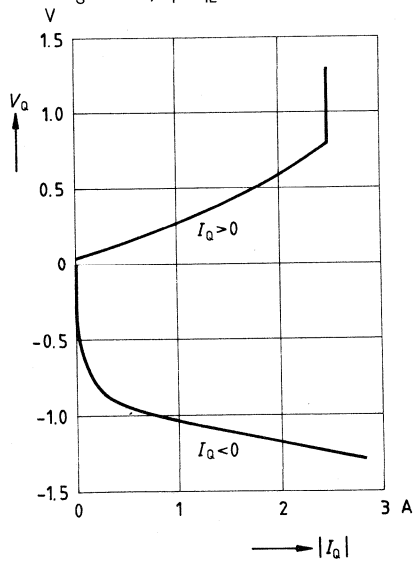
Quiescent current I_q versus case temperature T_C in OFF state
$V_S = 12$ V; $V_I = V_I \geq V_{IH}$



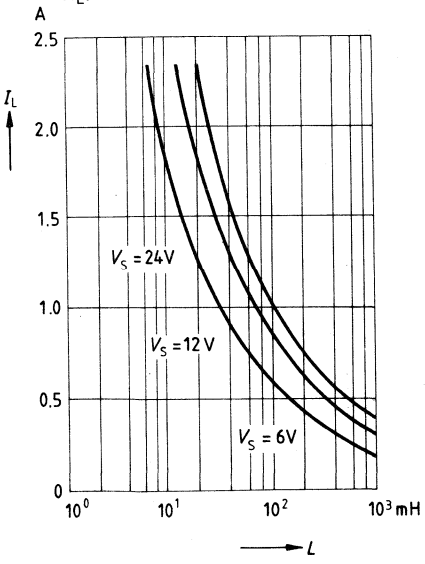
Short-circuit current I_{SC} versus output voltage V_Q
$V_S = 12$ V; $V_I \leq V_{IL}$



Output voltage V_Q versus output current $|I_Q|$
$V_S = 12$ V; $V_I \leq V_{IL}$



Max. load current I_L versus load inductance L
$R_L > 50$ mΩ



Preliminary Data **Bipolar IC**

Type	Ordering Code	Package
TLE 4214	Q67000-A8183	P-DIP-8

Features

- Double low-side driver, 2 x 0.5 A
- Power limitation
- Overtemperature protection
- Integrated free-wheel diodes
- Error feedback
- Voltage proof up to 70 V
- Short-circuit proof
- Temperature range from −40 °C to +100 °C
- Suitable for applications in automotive electronics

Application Notes

Applications in industrial electronics require intelligent power switches activated by logic signals, which are also short-circuit proof and provide for error feedback.

The IC contains two of these power switches (low-side driver). In case of inductive loads the integrated free-wheel diodes clamp the self-induction voltage.

If a "high" signal (> 2.4 V) is applied to the enable input both switches can be activated independently of one another through TTL signals at the control inputs (active high). The inputs are highly resistive and must therefore not be floated, but should always be connected to a fixed potential (noise immunity).

The status output (open collector) signals the following malfunctions through high potential:

- Overload
- Underload
- Short-circuit to ground
- Overvoltage
- Overtemperature

Circuit Description

Input Circuits

The control inputs and the enable input comprise TTL-compatible Schmitt triggers with hysteresis. Driven by these stages the buffer amplifiers convert the logic signal necessary for driving the NPN power transistors to the required form.

Switching Stages

The output stages comprise NPN power transistors with open collectors. Since the protective circuit allocated to each stage limits the power dissipation, the outputs are short-circuit proof to the supply voltage throughout the entire operating range. Positive voltage peaks, which occur during the switching of inductive loads, are limited by the integrated free-wheel diodes.

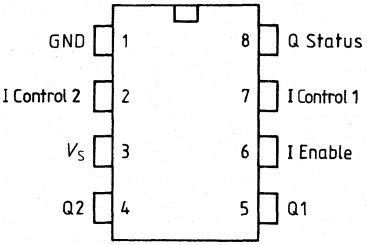
Monitoring and Protective Functions

During the activated status the outputs are monitored for underload (open circuit), overload, and short-circuit to ground (see table below). In addition, large sections of the circuit are de-activated in case of excessive supply voltages V_S. Linked via OR gate the information regarding these malfunctions effects the status output (open collector, active high). An internally determined dead time applied to all malfunctions but overvoltage prevents the output of messages in case of short-term malfunctions. Furthermore, a temperature protection circuit prevents thermal desctruction. An integrated reverse diode protects the supply voltage V_S against reverse polarities. Similarly the load circuit is protected against reverse polarities within the limits estabilished by the maximum ratings (no short circuit of the load at the same time!). At supply voltages below the operating range an undervoltage detector ensures that neither the status nor the outputs are activated. At supply voltages below the operating range the output stages are de-activated.

Status Output (H = Error)

	Undervoltage >3.5 V	**Operating range** L (passive)	H (active)	**Overvoltage**
Standard operation	L	L	L	H
Overload	L	L	H	H
Underload	L	L	H	H
Short circuit to ground	L	H	H	H
Overtemperature	L	H	H	H

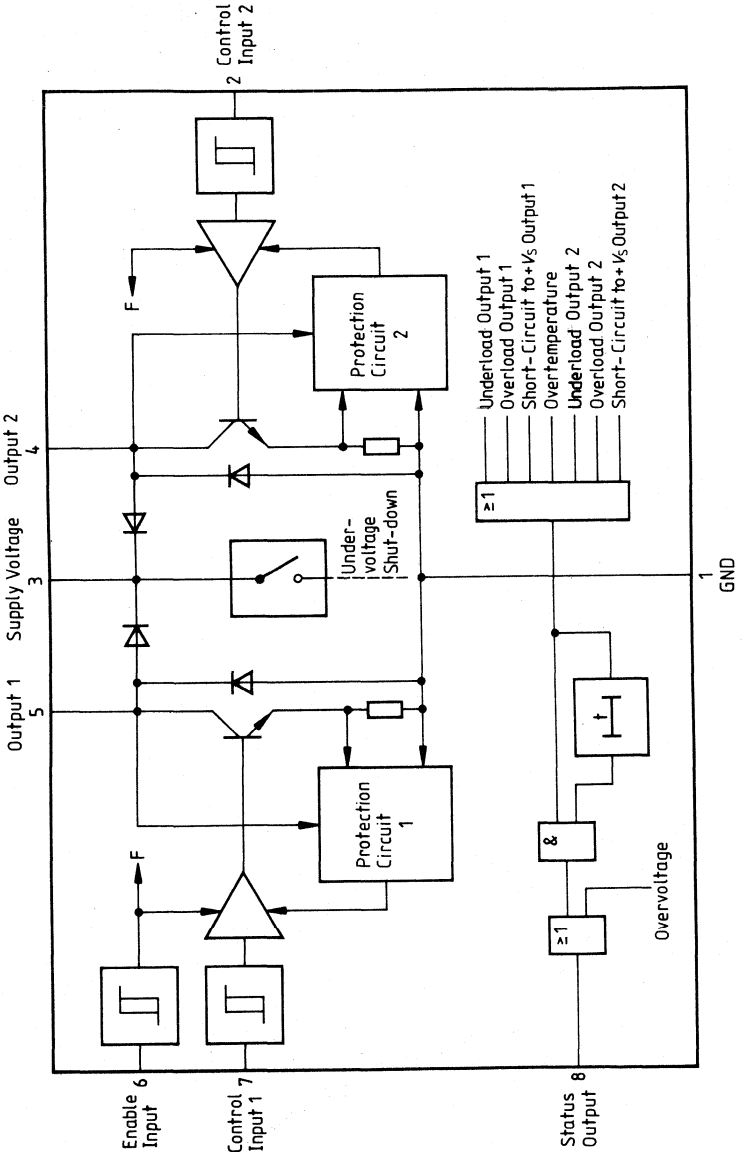
Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	GND	**Ground** Design wiring for the max. short-circuit current (2 x 1 A)
2	I Control 2	**Control input 2** (TTL compatible) activates the output transistor 2 in case of high potential
3	V_S	**Supply voltage** In case of overvoltage at this pin large sections of the circuit are de-activated. The status output indicates this malfunction without dead time.
4	Q2	**Output 2** Short-circuit proof, open collector output for currents up to 0.5 A, with free-wheel diodes to supply voltage.
5	Q1	**Output 1** Short-circuit proof, open collector output for currents up to 0.5 A, with free-wheel diodes to supply voltage.
6	I Enable	**Enable input,** active high
7	I Control 1	**Control input 1** (TTL compatible) activates output transistor 1 in case of high potential
8	Q Status	**Status output** (open collector) for both outputs; indicates over-temperature, overload, underload and short-circuits to ground in the load circuit as well as overvoltage at pin 3. Is switched to high after a defined dead time in case of malfunction (except: overvoltage)

Block Diagram



Maximum Ratings

$T_j = -40\,°C$ to $+150\,°C$

Description	Symbol	min	max	Unit
Voltages				
Supply voltage (pin 3) $t < 0.2$ s	V_S		70	V
Supply voltage (pin 3)	V_S	−1.3	40	V
Input voltage (pin 2; pin 6; pin 7)	V_I	−5	40	V
Output voltage (pin 8)	V_Q	−0.3	40	V
Output voltage (pin 4; pin 5)	V_Q	−0.3	$+V_S$	V
Currents				
Switching current (pin 4; pin 5) Internally limited	I_Q			
Current with reverse polarity (pin 4; pin 5) $t < 0.1$ s	I_Q	−0.7		A
Free-wheel current (pin 4; pin 5)	I_Q		0.7	A
Ground current (pin 1)	I_{GND}	−1.4	2.0	A
Output current (pin 8)	I_Q		10	mA
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−50	125	°C
Operating Range				
Supply voltage[1])	V_S	6	25	V
Ambient temperature P-DIP-8[2])	T_A	−40	100	°C
Ambient temperature Chip[2])	T_A	−40	120	°C
Supply voltage during load short circuit	V_S		16	V
Thermal resistance system – air	$R_{th\,SA}$		91	K/W

[1]) Lower limit = 5 V, if previously V_S greater than or equal to 6 V (turn-on hysteresis)
[2]) $T_j \leq 150\,°C$

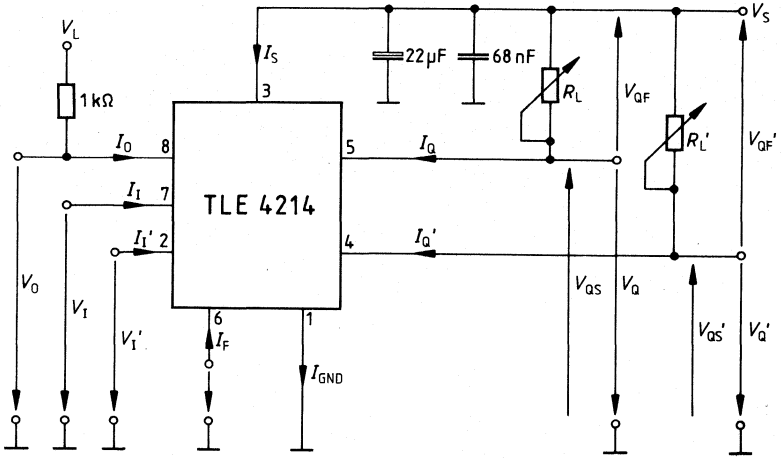
Characteristics

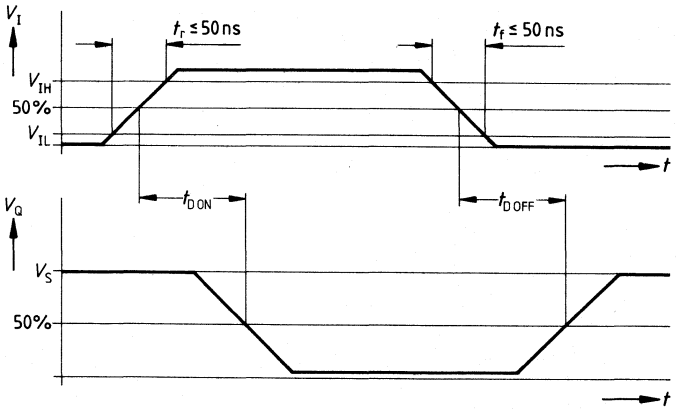
$V_S = 6\ V \ldots 16\ V$ (typ. $V_S = 12\ V$)
$T_j = -40\,°C \ldots +150\,°C$ (typ. $T_j = 25\,°C$)

Description	Symbol	Measuring conditions	min	typ	max	Unit
General characteristics						
Quiescent current	I_q	$V_F < V_{FL}$		2	4	mA
Quiescent current	I_q	$V_I = V_I' > V_{IH}$; $V_F > V_{FH}$		35	50	mA
Overvoltage switching threshold	V_{SO}	$V_L = 5\ V$; $V_O > 4.5\ V$	30	36	40	V
Hysteresis of overvoltage turn-off	ΔV_{SO}	$V_L = 5\ V$; $V_O > 4.5\ V$	4	6	9	V
Underload voltage threshold	V_Q	$V_L = 5\ V$; $V_O > 4.5\ V$	5	20	50	mV
Underload current	I_{QU}	$V_Q = V_{QU}$	10		20	mA
Logic						
Control inputs						
H switching threshold	V_{IH}	pin 2, 7	1.3	1.8	2.1	V
L switching threshold	V_{IL}	pin 2, 7	0.9	1.2	1.5	V
Hysteresis of input voltage	ΔV_I	pin 2, 7	0.4	0.6	1.0	V
H switching threshold	V_{FH}	pin 6	1.6	2.1	2.6	V
L switching threshold	V_{FL}	pin 6	1.5	1.8	2.1	V
Hysteresis of input voltage	ΔV_F	pin 6	0.1	0.3	0.7	V
H input current	I_{IH}	$V_I = 5\ V$; pin 2, 6, 7	0		10	µA
L input current	$-I_{IL}$	$V_I = 0.5\ V$; pin 2, 6, 7	0		10	µA
Status output (open collector)						
L saturation voltage	V_{QSat}	$I_O = 5\ mA$	0.1	0.2	0.4	V
Status dead time	t_{dS}	[1]	8	20	32	µs
Switching stages (also valid for input I' and output Q')						
Saturation voltage	V_{QSat}	$I_Q = 0.5\ A$; $V_I > V_{IH}$; $V_F > V_{FH}$		0.6	0.8	V
Saturation voltage	V_{QSat}	$I_Q = 50\ mA$; $V_I > V_{IH}$; $V_F > V_{FH}$	30	45	100	mV
Output current	I_Q	$V_{Q\,sat} \leq 0.8\ V$ $V_I > V_{IH}$	1	0.5		A
Leakage current	I_Q	$V_Q = V_S = 12\ V$; $V_I < V_{IL}$	0		75	µA
Switch-on time	$t_{D\,ON}$	see fig.; $R_L = 22\ \Omega$; $V_S = 12\ V$	0.2	2	5	µs
Switch-off time	$t_{D\,OFF}$	see fig.; $R_L = 22\ \Omega$; $V_S = 12\ V$	0.2	2	5	µs
Forward voltage of substrate diode	V_{QF}	$I_Q = -0.5\ A$ $t < 0.1\ s$		1.3	1.7	V
Forward voltage of free-wheel diode	V_{QS}	$I_Q = 0.5\ A$ $t < 0.1\ s$		1.3	1.7	V

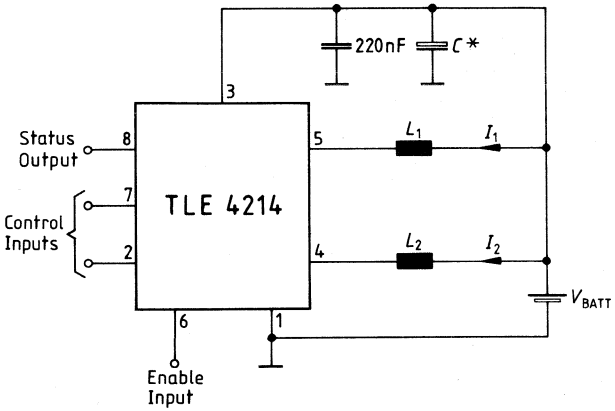
[1] Period from the beginning of the disturbance at one channel (exception: overvoltage) until the 50% value of the status switching edge is reached.

Measuring Circuit



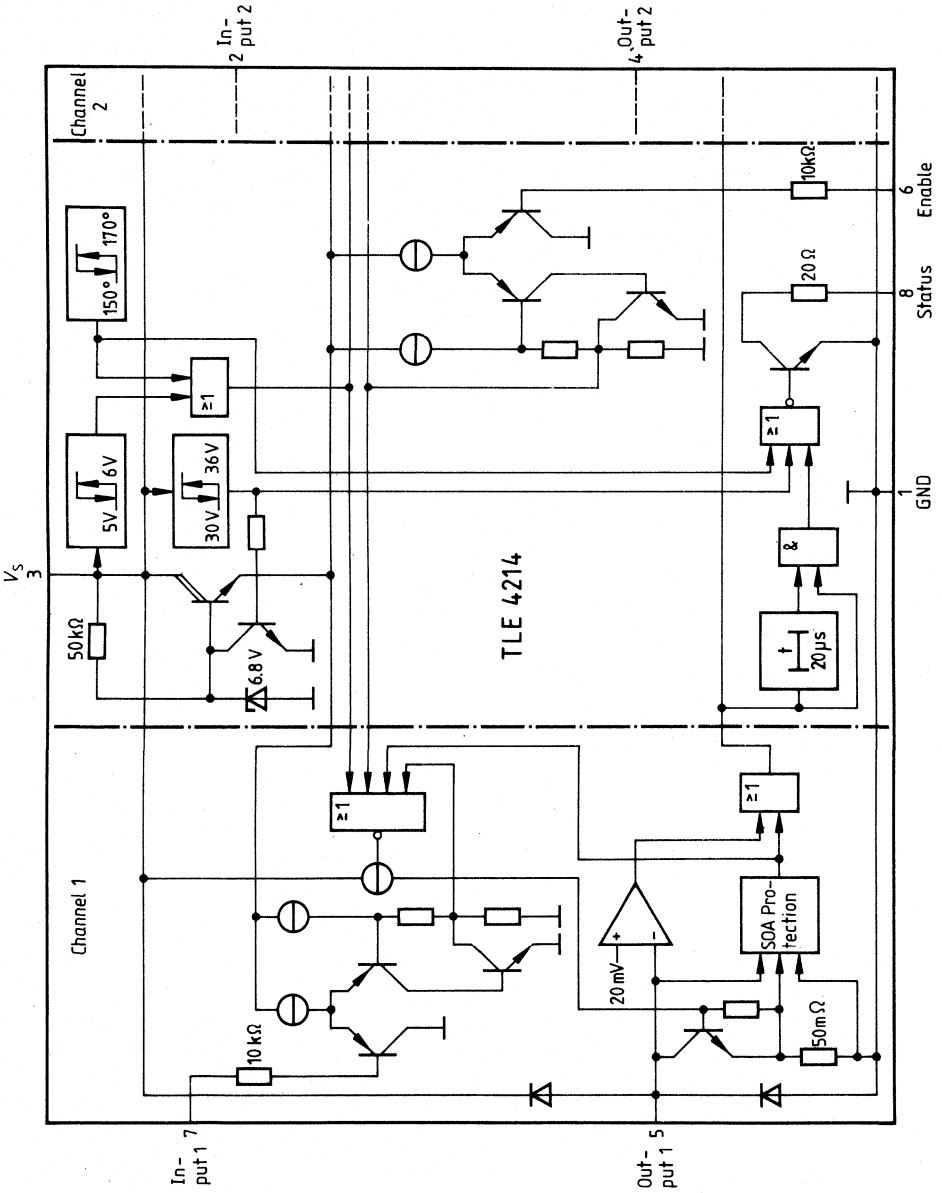


Application Circuit

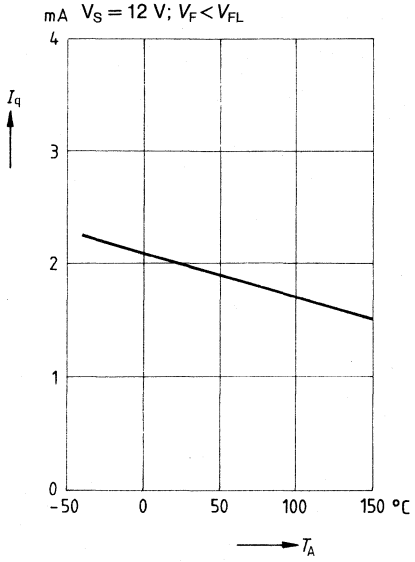


$C^* \geq (L_1 I_1^2 + L_2 I_2^2) / (40\,V - V_{BATT})^2$

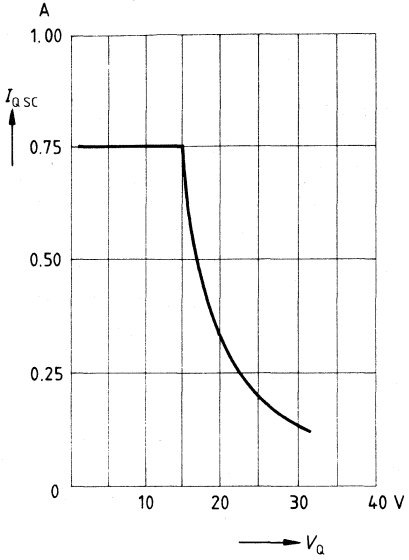
Circuit Diagram



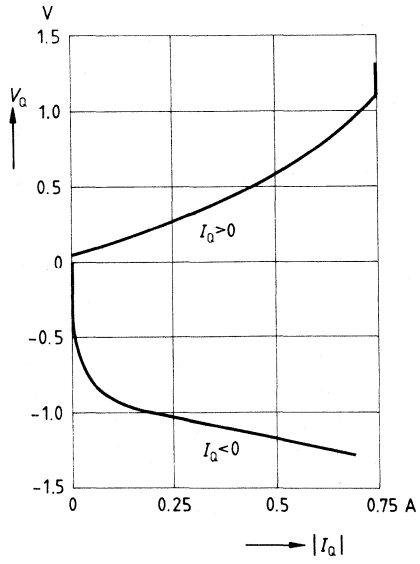
Quiescent current I_q versus ambient temperature T_A in the OFF status



Short-circuit current I_{SC} versus output voltage V_Q



Output voltage V_Q versus output current
$V_S = 12$ V; $V_I > V_{IH}$

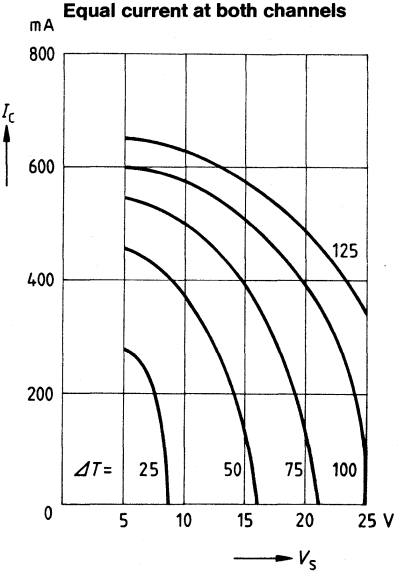


Maximum permissible output currents, being the result of the typical thermal power dissipation in a P-DIP-8 package, for three operating modes.

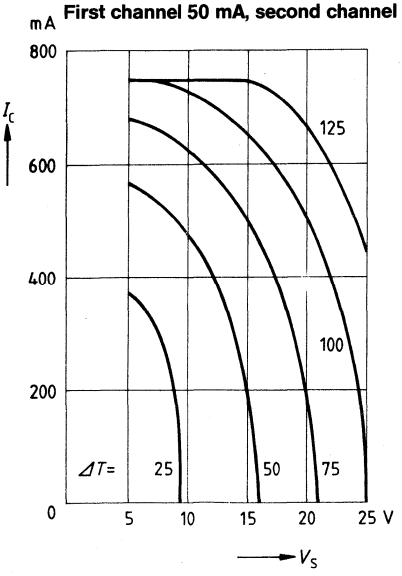
ΔT: Difference between junction and ambient temperature ($T_j - T_A$) [K].

I_C: Max. output current (steady current) per channel.

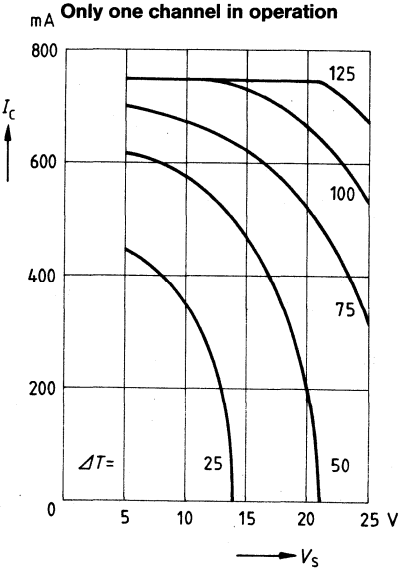
Equal current at both channels



First channel 50 mA, second channel I_C



Only one channel in operation



ICs for Sensors, Hall-Effect ICs, Proximity Switches, Light Sensors

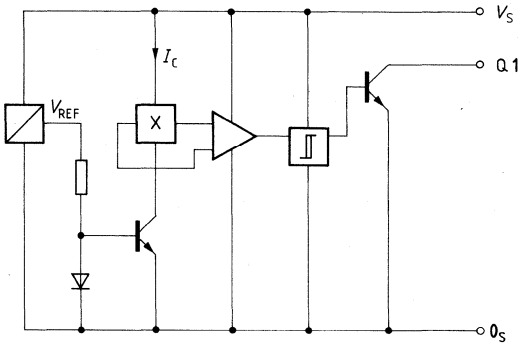
Selector Guide

Type	Package	Temperature range °C	Supply voltage Output current	Magnetic switching thresholds 0 to 70 °C	Main applications
TLE 4901 F[1])	Plastic flatpack	−40 to +135	4.50 to 30 V I_Q = 40 mA	−12/12 mT	Rpm sensor Angle indicator Electronic commutation Flow measurement
TLE 4901 K[1])	MIKROPACK (SMD)				
TLE 4902 F[1])	Plastic flatpack	−40 to +125	4.5 to 6.8 V I_Q = 20 mA	−15/15 mT	Rpm sensor Electronic commutation
TLE 4903 F[2])	Plastic flatpack	−40 to +130	4.3 to 24 V I_Q = 40 mA	18/13 mT	Breakerless triggering Limit switch
TLE 4910 K[3])	MIKROPACK (SMD)	−40 to +135	4.75 to 18 V I_Q = 10 mA	$-\infty < B < +\infty$	Position measurement (e.g. loudspeakers) Electronic pressure gauge Current measurement (potentialfree)

[1]) alternating magnetic field
[2]) unipolar magnetic field
[3]) output voltage proportional to magnetic field

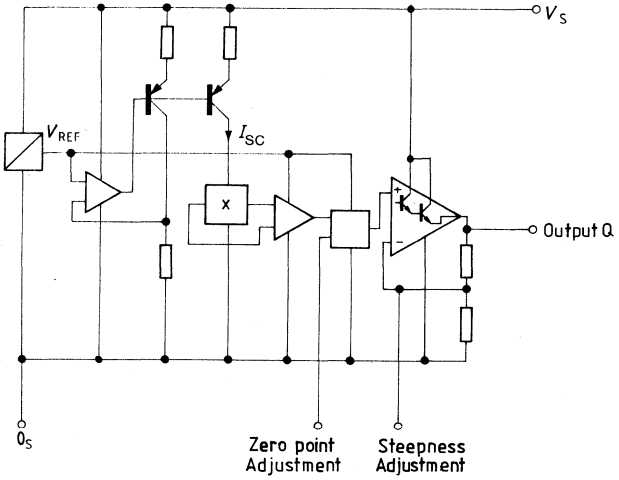
Schematic Circuit Diagrams

Digital Hall-effect IC



On a semiconductor crystal the contactless, magnetically controlled switches contain, a constant voltage regulator, a regulated voltage source for the Hall generator, a differential amplifier, a Schmitt trigger, two driver stages, and an end transistor with open collector. Their use is of advantage when high reliability, no bounce pulses, immunity to dirt and corrosion, and a long service life are required.

Linear Hall-effect IC



The hall generator is fed from a constant voltage source which uses a regulated voltage as reference. The Hall generator is followed by a differential amplifier. In the subsequent stage, the differential signal is converted into a ground-referenced signal.

At this point, the offset can be changed in a manner that is simple and not prone to interference, by the substraction or addition of a current.

The inverted amplifier input has been brought out, so that the steepness of the output characteristic (amplification) can be varied within a wide range by means of external components.

Integrated Hall-Effect Switch for Alternating Magnetic Fields

TLE 4901 F
TLE 4901 K

Preliminary Data

Bipolar IC

Type	Ordering Code	Package
TLE 4901 F	Q67000-A2518	Plastic flatpack
TLE 4901 K	Q67000-A2399	MIKROPACK (SMD)

The Hall-effect IC TLE 4901 is a static contactless switch operated by an alternating magnetic field. The output is switched to the conducting state by the south pole of the magnetic field and blocked by its north pole.

The IC is provided with an integrated overvoltage protection against most of the transients occurring in automotive and industrial applications.

The IC is particularly intended as an rpm sensor or an angle indicator.

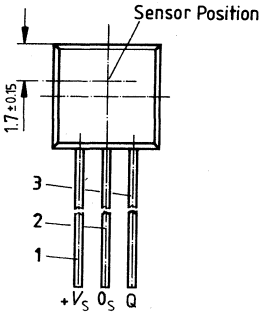
Multiple pole ring magnets are especially suited to switching the IC.

Features

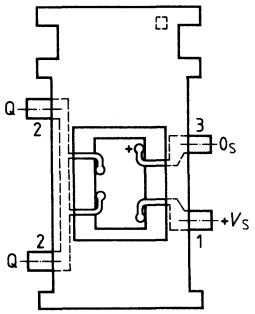
- Low switching thresholds with good long-term stability
- High interference immunity
- Overvoltage protection
- Extended temperature range −40 to +135 °C
- Insensitive to mechanical stress
- Flat plastic package (1.5 mm)

Pin Configurations
(top view)

TLE 4901 F



TLE 4901 K



Pin Descriptions

TLE 4901 F

Pin	Symbol	Function
1	+V_S	Supply voltage
2	0_S	Ground
3	Q	Output

TLE 4901 K

Pin	Symbol	Function
1	+V_S	Supply voltage
2	Q	Output
3	0_S	Ground

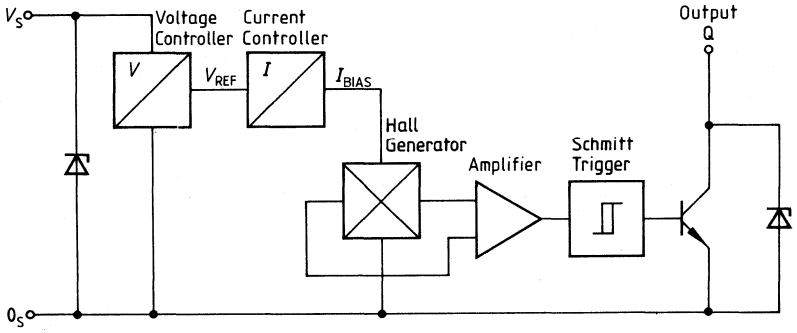
Circuit Description

The circuit includes a Hall generator, amplifier and a Schmitt trigger. The supply and the output terminals have protection circuits with Z characteristics to prevent overvoltage.

A magnetic field perpendicular to the chip surface induces a voltage at the sensor contacts of the integrated Hall generator. This voltage is amplified, Schmitt triggered, and used to control an NPN transistor with a collector output. The output-stage transistor conducts when the applied flux density exceeds the switching level. If the flux density is reduced by the hysteresis flux density, the output stops conducting.

To minimize the effects of supply voltage and temperature variations on the switching level, the Hall sensor is supplied by a stabilized current source, which is in turn derived from a reference voltage.

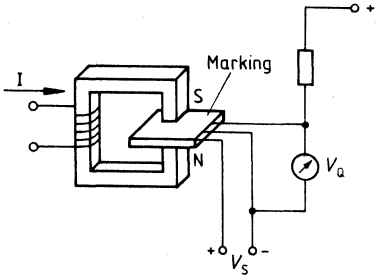
Block Diagram



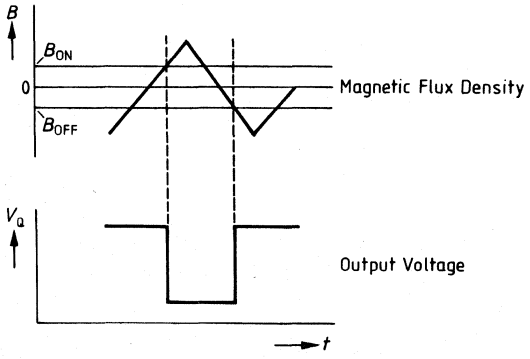
Functional Description

When a magnetic field is applied in the direction shown, and the turn-on flux density is exceeded, the IC's output conducts.

Reversal of the current direction in the electromagnet (i.e. reversal of the magnetic field) and falling below the turn-off flux density, leaves the output non-conducting.



Switching Characteristics



Maximum Ratings

$T_A = -40°C$ to $+135°C$

Description	Symbol	min	max	Unit
Supply voltage	V_S	−1.2	30	V
Output voltage	V_Q		30	V
output off-state				
Output current	I_Q		40	mA
output on-state				
Flux density range	B	unlimited		T
Junction temperature	T_j		150	°C
$t < 70\,000$ h				
Storage temperature	T_{stg}	−55	150	°C
$t < 70\,000$ h				
Thermal resistance				
system – air	$R_{th\ SA}$		250	K/W[1])
Overvoltage limits				
Current through protection devices	I_Z	−200	200	mA
$t < 2$ ms				

Operating Range

Supply voltage	V_S	4.5	30	V
Ambient temperature	T_A	−40	135	°C

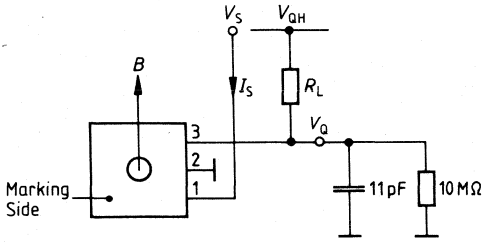
[1]) Thermal resistance of TLE 4901 K depends on type of mounting

Characteristics

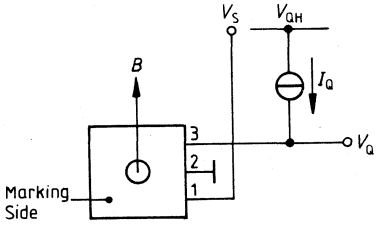
$V_S = 6$ to 16 V; $T_A = -30°C$ to $+125°C$

Description	Symbol	Measurement circuit	min	typ	max	Unit
Supply current $B \leq B_{OFF}$ $B \geq B_{ON}$	I_S	 2 2	 2 3		 8 13	 mA
Flux density of "ON" $T_A = 25°C$ Flux density for "OFF" $T_A = 25°C$	B_{ON} B_{OFF}	2 2	 −10		10 	mT mT
Flux density for "ON" $T_A = -25$ to 85 °C Flux density for "OFF" $T_A = -25$ to 85 °C	B_{ON} B_{OFF}	2 2	 −12		12 	mT mT
Hysteresis $T_A = -25$ to 85 °C	B_H	2	3		14	mT
Flux density for "ON" Flux density for "OFF"	B_{ON} B_{OFF}	2 2	 −15		15	mT mT
Hysteresis	B_H	2	2		15	mT
Output leakage current $B \leq B_{OFF}$	I_{QH}	2		10		µA
Output voltage $I_{QL} = 16$ mA $B \geq B_{ON}$	V_{QL}	2			0.4	V
Transition times of output Fall time Rise time	 t_{HL} t_{LH}	 1 1	 	 0.3 0.5	 1 1	 µs µs

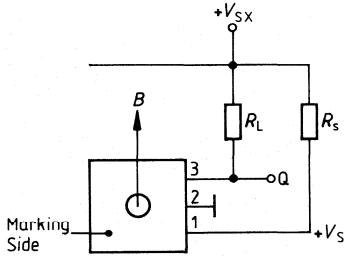
Measurement Circuit 1



Measurement Circuit 2



Application Circuit



For optimum protection against destruction, R_S is required to be as high as possible.

Dimensioning:

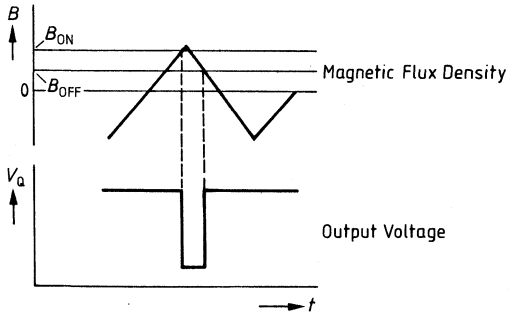
$$R_s = \frac{V_{SX\,min} - V_{S\,min}}{I_{S\,max}}$$

$V_{SX\,min}$ is the minimum supply voltage in each application.

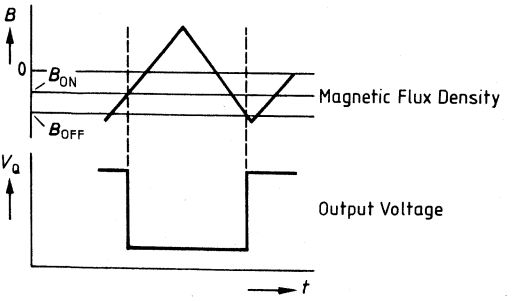
Pulse Diagrams

Flux density	Q
$B > B_{ON}$	L
$B < B_{OFF}$	H

The characteristics include the following extreme cases:
$B_{ON} = B_{ON\ max}$



$B_{OFF} = B_{OFF\ min}$



Integrated Hall-Effect Switch for Alternating Magnetic Fields

TLE 4902 F

Preliminary Data

Bipolar IC

Type	Ordering Code	Package
TLE 4902 F	Q67000-A8048	Plastic flatpack

The Hall-Effect IC TLE 4902 F is a static contactless switch operated by an alternating magnetic field. The output is switched to the conducting state by the south pole of a magnetic field and is blocked by its north pole.

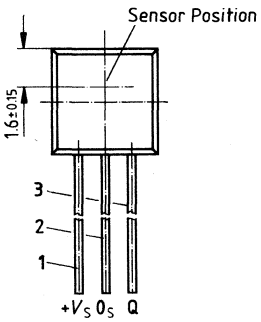
The IC is especially suited to applications as an rpm sensor or an angle indicator.

Features

- Low switching threshold with good long-term stability
- Extended temperature range −40 to +125 °C
- Flat plastic package (1.5 mm)
- Suited to low-cost applications, e.g. electronic commutation of electronic motors
- Insensitive to mechanical stress

Pin Configuration

(top view)



Pin Description

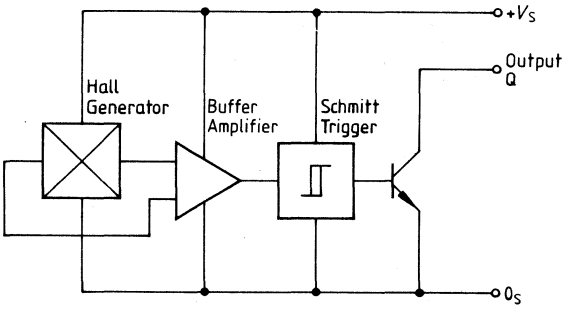
Pin	Symbol	Function
1	$+V_S$	Supply voltage
2	0_S	Ground
3	Q	Open collector output

Circuit Description

The circuit includes a Hall generator, amplifier, a Schmitt trigger and an open collector output.

A magnetic field perpendicular to the chip surface induces a voltage at the sensor contacts of the integrated Hall generator. This voltage is amplified, Schmitt triggered, and used to control an NPN transistor with a collector output. The output-stage transistor conducts when the applied flux density exceeds the switching level. If the flux density is reduced by the hysteresis flux density, the output stops conducting.

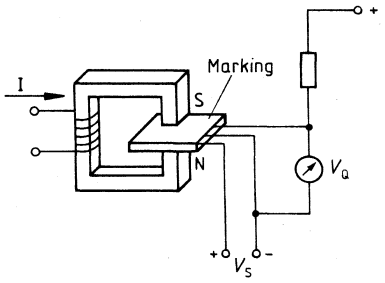
Block Diagram



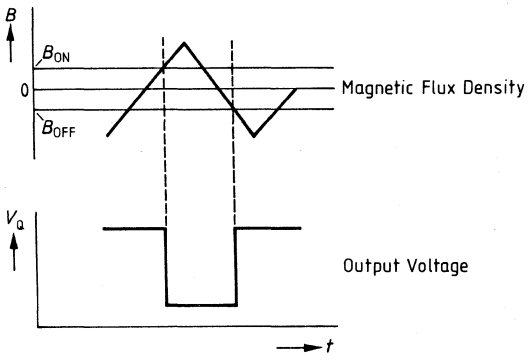
Functional Description

When a magnetic field is applied in the direction shown, and the turn-on flux density is exceeded, the IC's output conducts.

Reversal of the current direction in the electromagnet (i.e. reversal of the magnetic field) and falling below the turn-off flux density, leaves the output non-conducting.



Switching Characteristics



Maximum Ratings

$T_A = -40$ to $+125$ °C

Description	Symbol	min	max	Unit
Supply voltage Output voltage output off-state	V_S V_Q	−0.5	7 30	V V
Output current output on-state	I_Q		20	mA
Magnetic flux density range	B	unlimited		T
Junction temperature $t < 70000$ h Storage temperature $t < 70000$ h	T_j T_{stg}	 −40	150 150	°C °C
Thermal resistance system – air	$R_{th\ SA}$		240	K/W

Operating Range

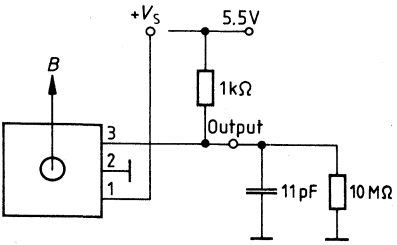
Supply voltage	V_S	4.5	6.8	V
Ambient temperature	T_A	−40	125	°C

Characteristics

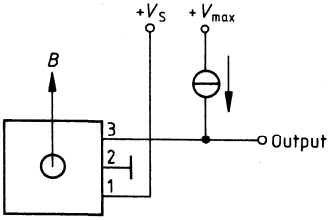
$T_A = 0$ to $+85\,°C$; $V_S = 4.5$ to 5.5 V (unless otherwise specified)

Description	Symbol	Measurement circuit	min	typ	max	Unit
Flux density for "ON" $T_A = 25\,°C$	B_{ON}	2			10	mT
Flux density for "OFF" $T_A = 25\,°C$	B_{OFF}	2	10			mT
Flux density for "ON" Flux density for "OFF"	B_{ON} B_{OFF}	2 2	 −15		15	mT mT
Hysteresis	B_H	2	3		14	mT
Flux density for "ON" $T_A = -40$ to $+125\,°C$; $V_S = 4.5$ to 6.8 V	B_{ON}	2			20	mT
Flux density for "OFF" $T_A = -40$ to $+125\,°C$; $V_S = 4.5$ to 6.8 V	B_{OFF}	2	−20			mT
Hysteresis $T_A = -40$ to $+125\,°C$; $V_S = 4.5$ to 6.8 V	B_H	2	2		15	mT
Output current $B \leq B_{OFF}$	I_{QH}	2			10	µA
Output voltage $B \geq B_{ON}$; $I_{QL} = 16$ mA	V_{QL}	2			0.4	V
Transition times of output Fall time Rise time	 t_{HL} t_{LH}	 1 1	 	 0.3 0.5	 1 1	 µs µs
Supply current $B \leq B_{OFF}$ $B \geq B_{ON}$	 I_S I_S	 2 2	 2 3	 	 5.5 6.5	 mA mA

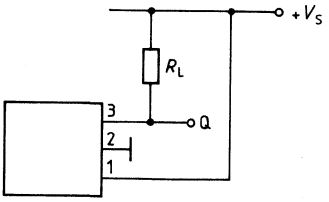
Measurement Circuit 1



Measurement Circuit 2



Application Circuit

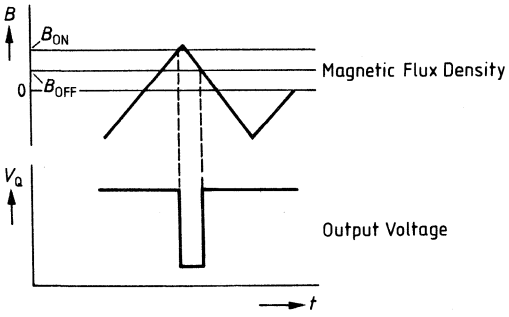


Pulse Diagrams

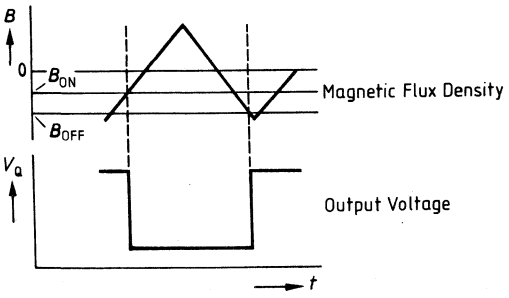
Flux density	Q
$B > B_{ON}$	L
$B < B_{OFF}$	H

The characteristics include the following extreme cases:

$B_{ON} = B_{ON\ max}$



$B_{OFF} = B_{OFF\ min}$



Integrated Hall-Effect Switch for Unipolar Magnetic Fields

TLE 4903 F

Preliminary Data

Bipolar IC

Type	Ordering Code	Package
S TLE 4903 F	Q67000-A8047	Plastic flatpack

The integrated Hall IC TLE 4903 F is a contactless switch operated by a magnetic field.

On reaching the turn-on flux density of the south-pole of a magnetic field, the output conducts. As the flux density strength sinks below the turn-off level, the output stops conducting.

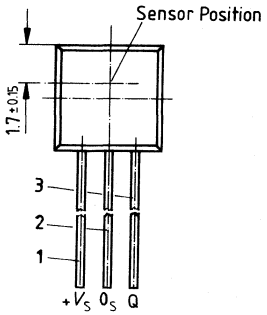
The IC is provided with an integrated overvoltage protection against most of the transients occurring in automotive and industrial applications.

Features

- Low switching thresholds with good long-term stability
- High interference immunity
- Overvoltage protection
- Extended temperature range −40 to +130 °C
- Insensitive to mechanical stress
- Flat plastic package (1.5 mm)

Pin Configuration

(top view)



Pin Description

Pin	Symbol	Function
1	+V_S	Supply voltage
2	0_S	Ground
3	Q	Open collector output

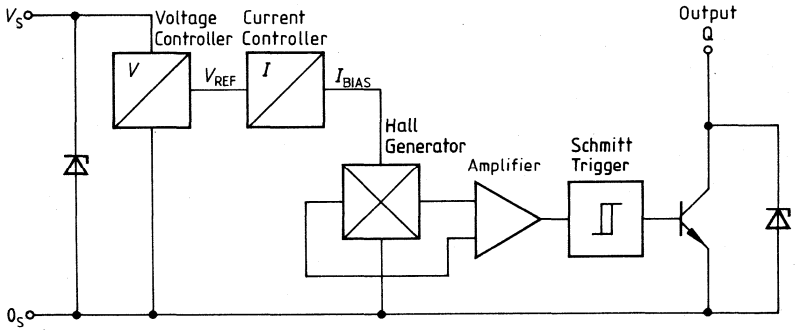
Circuit Description

The circuit includes a Hall generator, amplifier, Schmitt trigger and an open collector output. The supply and the output terminals have protection circuits to prevent overvoltage.

A magnetic field perpendicular to the chip surface induces a voltage at the sensor contacts of the integrated Hall generator. This voltage is amplified, Schmitt triggered and used to control an NPN transistor with a collector output. The output-stage transistor conducts when the applied flux density exceeds the switching level. If the flux density is reduced by the hysteresis flux density, the output stops conducting.

To minimize the effects of supply voltage and temperature variations on the switching level, the Hall sensor is supplied by a stabilized current source, which is in turn derived from a reference voltage.

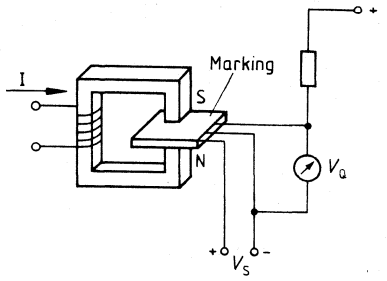
Block Diagram



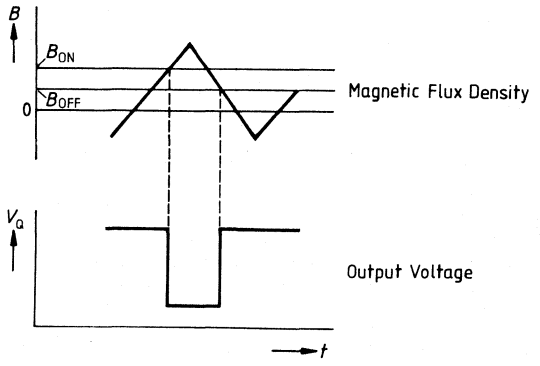
Functional Description

When a magnetic field is applied in the direction shown, and the turn-on flux density is exceeded, the IC's output conducts.

Reduction of the current and falling below the turn-off flux density, leaves the output non-conducting.



Switching Characteristics



Maximum Ratings

$T_A = -40$ to $+130$ °C

Description	Symbol	min	max	Unit
Supply voltage	V_S	−1.2	30	V
Output current	I_Q		40	mA
Junction temperature $t = < 70000$ h	T_j	−40	150	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance system – air	$R_{th\ SA}$		240	K/W
Flux density range	B	$-\infty$	$+\infty$	
Output voltage	V_Q		30	V

Overvoltage Limits

Current through protection devices at pins 1 and 3 $t < 10$ µs		−200	200	mA

Operating Range

Supply voltage	V_S	4.3	24	V
Ambient temperature	T_A	−40	130	°C

Characteristics

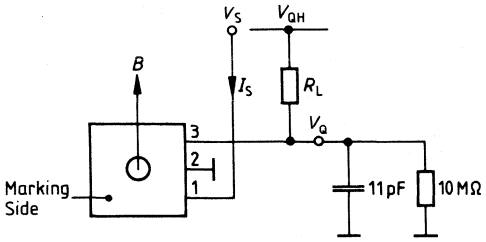
$V_S = 14$ V; $T_A = 25$ °C

Description	Symbol	Test conditions	Test circuit	min	typ	max	Unit
Magnetic Parameters[1]							
Flux density "ON"	B_{ON}	$T_A = 25$ °C $T_A = 0$ to 70 °C $T_A = -30$ to 100 °C $T_A = -30$ to 125 °C	 2	20 18 13 12		50 52 57 58	mT[2] mT mT mT
Flux density "OFF"	B_{OFF}	$T_A = 25$ °C $T_A = 0$ to 70 °C $T_A = -30$ to 100 °C $T_A = -30$ to 125 °C	 2	15 13 8 7		35 37 42 43	mT mT mT mT
Hysteresis ($B_{ON} - B_{OFF}$)	B_H		2	5		15	mT
Output junction current	I_{QO}	$B < B_{OFF}$; $V_{OH} = 24$ V $T_A = 25$ °C				10	µA
Supply current	I_S	$B < B_{ON}$ $B > B_{OFF}$	1 1			13 14	mA mA
Output voltage	V_Q	$I_Q = 30$ mA	2			0.4	V
Rise time Fall time	t_{LH} t_{HL}	$I_Q = 10$ mA $I_Q = 10$ mA				1 1	µs µs
Overvoltage Limit							
Supply voltage Output	V_{SZ} V_{QZ}	$I_S = 16$ mA $I_{QZ} = 16$ mA		32 32		42 42	V V

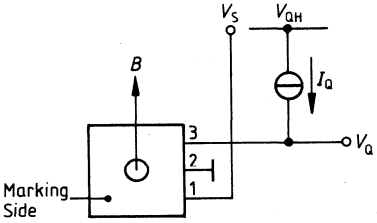
[1] The magnetic parameters are specified for a homogenous magnetic field at the sensor center as shown in the application circuit.

[2] 1 mT = 10 G

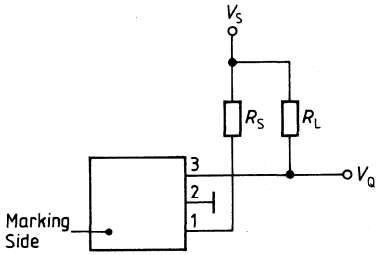
Measurement Circuit 1



Measurement Circuit 2



Application Circuit



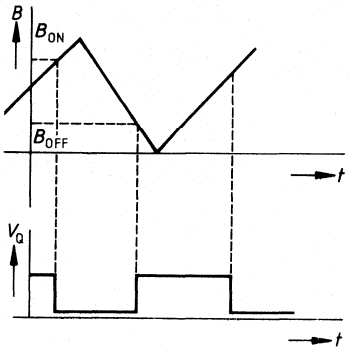
For optimum protection against destruction, R_S is required to be as high as possible.

Dimensioning:

$$R_s = \frac{V_{SX\,min} - V_{S\,min}}{I_{S\,max}}$$

$V_{SX\,min}$ is the minimum supply voltage in each application.

Pulse Diagram



Preliminary Data **Bipolar IC**

Type	Ordering Code	Package
TLE 4910 K	Q67000-A2398	MIKROPACK (SMD)
TLE 4910	in P-DSO-8 package is under development	

The IC TLE 4910 K generates an output voltage proportional to the magnetic flux density. The IC is made northpole or southpole-active by adjusting the zero point. External resistors are used to adjust the zero point of the transfer characteristic as well as the sensitivity of the device. The IC is suited as sensor for industrial applications requiring enhanced temperature and improved data ranges e.g. measurement of pressure, acceleration, distance and torsion.

Features

- Linear output characteristic
- Extended temperature range (−40 to +135 °C)
- Virtually independent of supply voltage and temperature variations
- Reference voltage available (3 V)

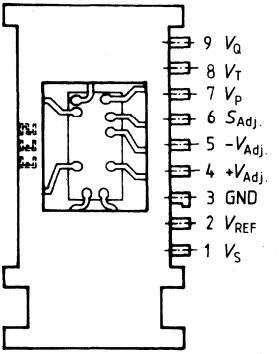
Function

The IC TLE 4910 K can be operated at supply voltages between 4.75 V and 18 V. Its output signal is a voltage with reference to ground which can supply up to 5 mA.

As shown in the block diagram the current for the Hall sensor is supplied by an internal current source. The output signal of the Hall sensor is first amplified in a differential amplifier to a sufficiently high level and then converted into a grounded signal.

The output stage includes an operational amplifier with internal feedback. The op amp inverting input is brought out at a pin and can be used for tuning the sensitivity of the device.

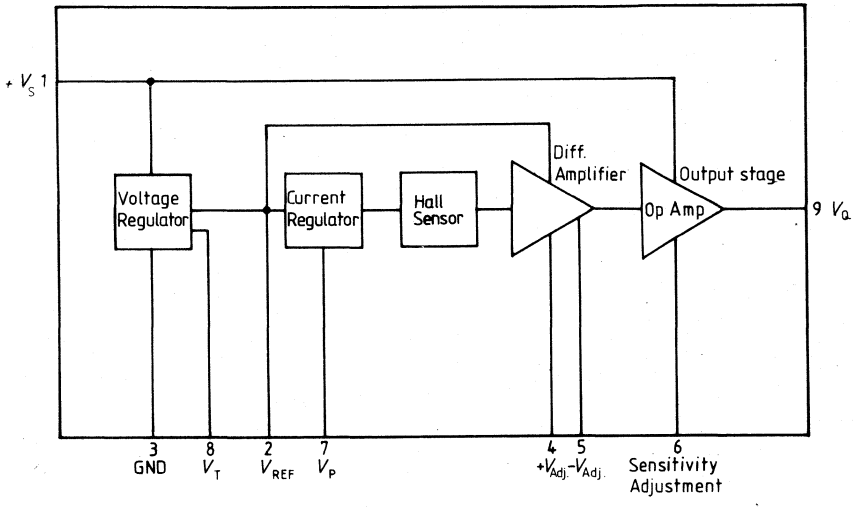
Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	V_S	Supply voltage
2	V_{REF}	Reference voltage
3	GND	Ground
4	$+V_{Adj}$	+Zero adjustment
5	$-V_{Adj}$	−Zero adjustment
6	S_{Adj}	Sensitivity adjustment
7	V_P	Probe voltage
8	V_T	Temperature voltage
9	V_Q	Voltage output

Block Diagram



Maximum Ratings

$T_A = -40\,°C$ to $+150\,°C$; $t < 70000$ h

Description	Symbol	min	max	Unit
Supply voltage	V_S		30	V
Output current	I_Q		10	mA
Induction	B	$-\infty$	$+\infty$	
Zero adjustment current	I_{Adj}	−1	1	mA
Junction temperature Storage temperature	T_j T_{stg}	 −40	125 125	°C °C
Thermal resistance junction – air	$R_{th\ JA}$	depends on mounting		

Operating Range

Supply voltage	V_S	4.75	18	V
Output current	I_Q		5	mA
Ambient temperature $t < 70000$ h	T_A	−40	135	°C

Characteristics

$T_A = 25\,°C$

Description	Symbol	Test circuit	min	typ	max	Unit
Supply current $B < -20$ mT	I_S	1			10	mA
Output voltage $R_L = 10\,k\Omega$; $V_S = 5$ V	V_Q	1	0.05		$V_S - 2$	V
Sensitivity	S	1		30		mV/mT
Magnetic offset	B_0	1	−20		20	mT
Linearity error $B = 0$ to 100 mT	L	1		1	2	%
Temperature coefficient of the magnetic offset	α_{B0}	1		±0.03		mT/K
Temperature coefficient of the sensitivity	α_S	1		±0.05		%/K
Reference voltage	V_{REF}	1	2.9	3.0	3.1	V
Output voltage/Adjustment current Pin 4	V_Q/I_{Adj}	2		0.3		V/µA
Output voltage/Adjustment current Pin 5	V_Q/I_{Adj}	2		−0.3		V/µA
Voltage at pin 4 and 5	V_{Adj}	2	30	70	110	mV
Temperature voltage $V_S = 5$ V; $R = 5.1\,k\Omega$	V_T	3	1.4		1.7	V
Temperature coefficient of the V_T $V_S = 5$ V; $R = 5.1\,k\Omega$	α_{VT}	3	3.5		4.5	mV/K
Output impedance $V_S = 5$ V; $I_Q < 5$ mA	R_Q				10	Ω
Sensitivity change due to V_S changes	$\Delta S/\Delta V_S$	1			0.2	%/V
Magnetic offset voltage due to V_S changes	$\Delta B_0/\Delta V_S$	1			20	µT/V

Test Circuits
Figure 1

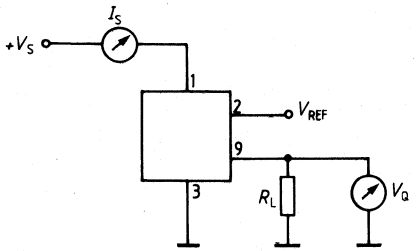


Figure 2

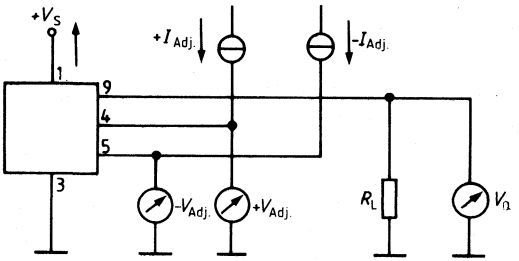
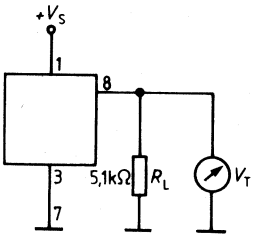
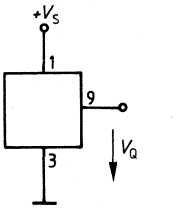


Figure 3



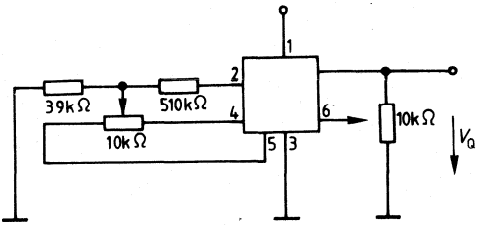
Application Circuits

Figure 4a



IC without Adjustment

Figure 4b

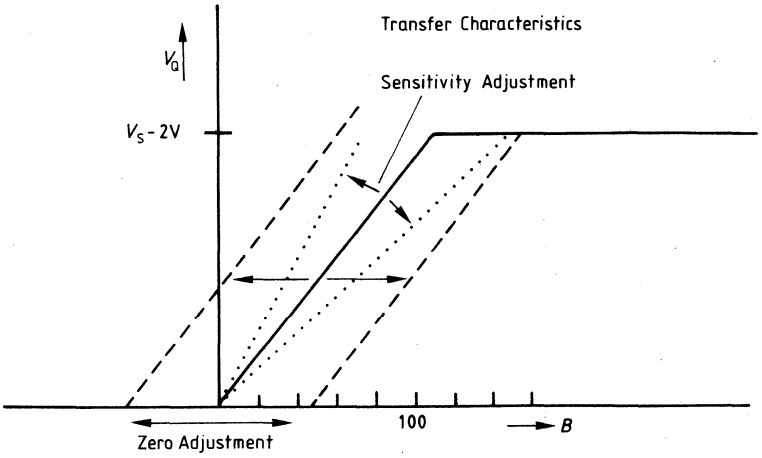


Zero Adjustment

Sensitivity Adjustment

Functional Diagram

Figure 5



Hall-Effect IC with Output Voltage Proportional to Magnetic Field

■ SAS 231 W

Bipolar IC

Type	Ordering Code	Package
■ SAS 231 W	Q67000-A1468-W	Miniature plastic package, 6 pins

The IC SAS 231 generates an output voltage proportional to the magnetic flux density. The output voltage increases when the south pole of a magnet approaches the top surface of the chip. The zero point is adjusted by external components. The steepness of the characteristic curve V_Q as a function of B can be varied by external components.

Maximum Ratings

Description	Symbol	Test conditions	min	typ	max	Unit
Supply voltage	V_S		0		18	V
Output current	I_Q				10	mA
Storage temperature	T_{stg}		−40		125	°C

Operating Range

Supply voltage	V_S		4.75		15	V
Output current	I_Q				5	mA
Ambient temperature	T_A		0		70	°C

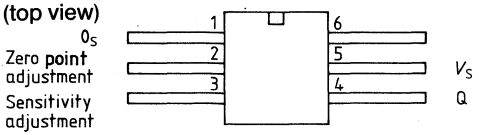
Electrical Characteristics

$V_S = 10$ V, $T_A = 25$ °C, unless otherwise specified

Open-loop supply current consumption	I_S	$R_L = \infty$		6	10	mA
Output voltage	V_Q	$R_L = 10$ kΩ	0.05		V_S-2	V
Steepness (without adjustment)	S		60	100	140	mV/mT
"Zero" component	B_0	$V_Q = 0.5$ V	−35		35	mT
Linearity error (referred to $V_Q = \frac{V_S}{2}$)				2		%
Temperature coefficient	α	$T_A = 0$ °C to 70 °C		0.4		mT/K

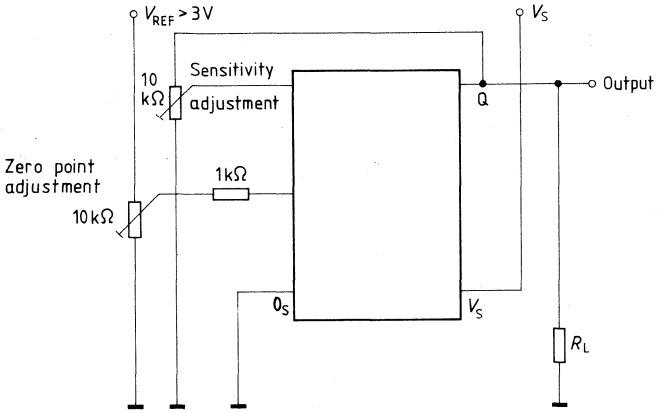
Pin Configuration

(top view)



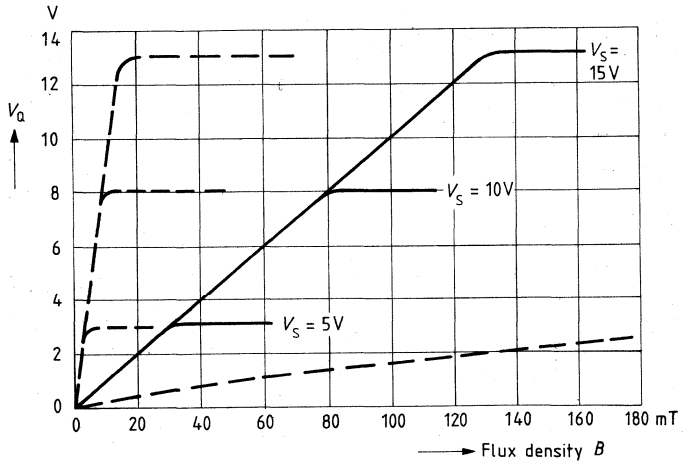
■ Not for new design

Application Circuit



Output Characteristic without Adjustment

Output voltage versus flux density



Type	Ordering Code	Package
S HKZ 101 S[1])	Q67000-S64	Special package
HKZ 101	Q67000-A9001	

The Hall-effect vane switch HKZ 101 is a contactless switch consisting of a monolithic integrated Hall-effect circuit and a special magnetic circuit hermetically sealed in a plastic package. The switch is actuated by a soft-iron vane which is passed through the air gap between magnet and Hall sensor.

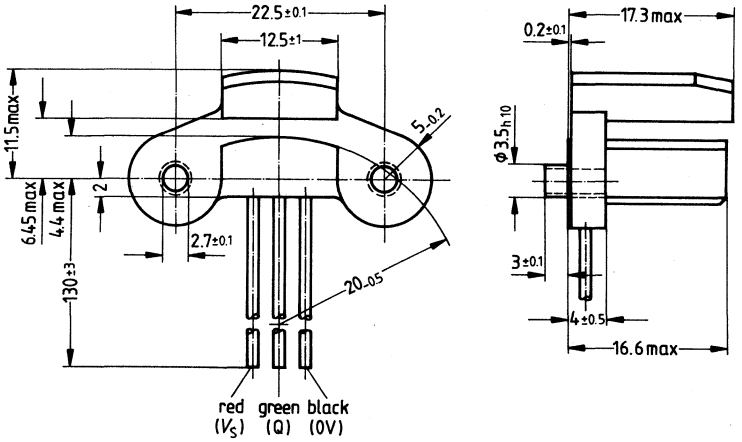
The main application field is in cars, i.e. as a breakerless trigger in electronic ignition systems. Numerous industrial applications can be found in control engineering, especially in those areas where switches must operate maintenance-free under harsh environmental conditions (e.g. rpm sensor, limit switch, position sensor, speed measurement, shaft encoder, scanning of coding disks, etc.).

Features

- Contactless switch with open collector output (40 mA)
- Static switching
- High switching frequency
- Hermetically sealed with plastic
- Unaffected by dirt, light, vibration
- Large temperature and voltage range
- Integrated overvoltage protection
- High interference immunity

[1]) **Note:** The temperature range of the HKZ 101 S has been extended to between −40 °C and +130 °C (previously 0 °C to +70 °C), and the switching-point characteristics have been adapted accordingly.

Special package

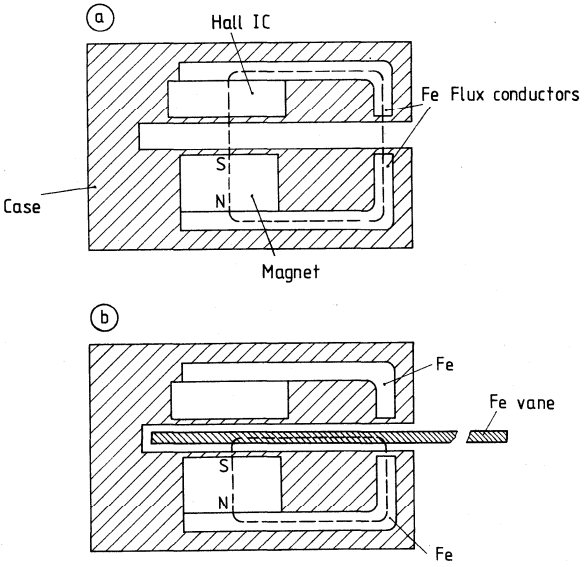


Function

The Hall-effect switch is actuated by a soft-iron vane that passes through the air gap between magnet and Hall-effect sensor. The vane short-circuits the magnetic flux before the Hall-effect sensor, as shown in figure 1. The open collector output is conductive (LOW) when the vane is outside the air gap, and blocks (HIGH) when the vane is introduced into the air gap. The output remains HIGH as long as the vane remains in the air gap. This static function does not require a minimum operating frequency. The output signal shape is independent of the operating frequency.

The circuit features integrated overvoltage protection against most of the voltage peaks occurring in automotive and industrial applications. The output stage has a Schmitt trigger characteristic. Most electronic circuits can be driven directly due to the open collector output current of max. 40 mA.

Figure 1
Principle of Operation



a) Magnetic flux through the Hall-effect switch with no vane in the gap

b) Magnetic flux short-circuited by the soft-iron vane

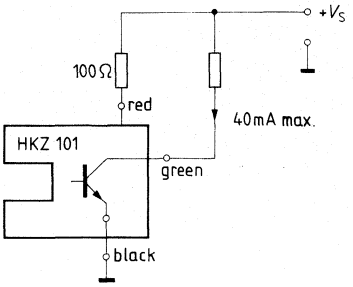
Mechanical Characteristics

The Hall-effect vane switch is hermetically sealed in a special plastic, so that it can also be used under harsh environmental conditions. The package is waterproof, vibration-resistant and resistant to gasoline, oil and salt. Two tubular rivets are incorporated in the package to mount the sensor on its carrier plate. The circuit has three flexible leads for power supply and output.

Application Notes

The output current of the "open collector" must be limited to the maximum permissible value by a load resistor adapted to the application.

For optimum efficiency of the integrated overvoltage protection, it is suggested that a resistor of approx. 100 Ω be provided in the component's power supply to limit the current.



Maximum Ratings

Description	Symbol	Test conditions	min	max	Unit
Supply voltage	V_S		−1.2	24	V
		$T_A = 25\,°C$		30	V
Output voltage in OFF-state	V_Q		−0.8	30	V
Inverse supply current (limited externally)	$-I_S$	$T_A \leq 80\,°C$ $t \leq 1$ h		200	mA
Output current	I_Q	without vane		40	mA
Inverse output current	$-I_Q$			30	mA
Ambient temperature	T_A		−40	135	°C
Storage temperature	T_{stg}		−40	150	°C
Thermal resistance system – air	$R_{th\,SA}$			170	K/W

Operating Range

Supply voltage		V_S		4.5	24	V
Ambient temperature		T_A		−40	130	°C
Vane[1]:	thickness	a		0.5		mm
	width	b		8		mm
	gap length	c		8		mm
	immersion depth	h		4.6	9	mm
	gap height	d		17.3 – h		mm

[1]) see figure 3

Characteristics

$V_S = 5$ V to 18 V,
$T_A = -30$ °C to +130 °C

Description	Symbol	Test conditions	min	max	Unit
Output saturation voltage	$V_{Q\,sat}$	without vane $I_Q = 40$ mA $T_A = -30$ to 110 °C $T_A = 110$ to 130 °C		 0.4 0.6	 V V
Output reverse current Supply current	$I_{Q\,R}$ I_S	with vane without vane		10 12	µA mA
Delay time	t_{LH}, t_{HL}	$I_Q = 40$ mA		1	µs
Overvoltage protection – Supply voltage (V_S) – Output (V_Q)	 V_{SZ} V_{SO}	 $I_S = 16$ mA $I_S = 16$ mA	 32 32	 42 42	 V V

Switching Point Characteristics

Definitions

In most applications, the switching point is set exactly by mechanical adjustment, thus compensating all mechanical tolerances in the system including the scatter of the Hall-effect vane switch. For the function of the device in operation, only the deviations of those characteristics depending on temperature and operating voltage are important.

The characteristic values of the switching points are, therefore, not directly referred to the mechanical dimensions of the vane switch, but to an electrically defined symmetry B_0 according to formula 1):

1) $B_0 = (ON_{left} + OFF_{left} + ON_{right} + OFF_{right}) : 4$
$B_0 = A_0 \pm 0.3$ mm

The definition of the operate and release points is shown in figure 2.

Operate point f_{ON} is obtained by subtracting the measured ON operate value from the reference point B_0:

2) $f_{ON} = ON_{right} - B_0 = B_0 - ON_{left}$

The release point f_{OFF} is calculated from the difference between the appropriate ON and OFF points:

3) $f_{OFF} = ON_{right} - OFF_{right} = OFF_{left} - ON_{left}$

$f_{ON\,0}$ and $f_{OFF\,0}$ are the switching points measured for the individual component under normal conditions ($V_S = 12$ V, $T_A = 25$ °C) within the characteristic device deviation.

The deviations of the operate and release points are defined according to 4):

4) $\Delta f_{ON} = f_{ON} - f_{ON\,0}$
$\Delta f_{OFF} = f_{OFF} - f_{OFF\,0}$

Figure 2
Switching Point Definitions

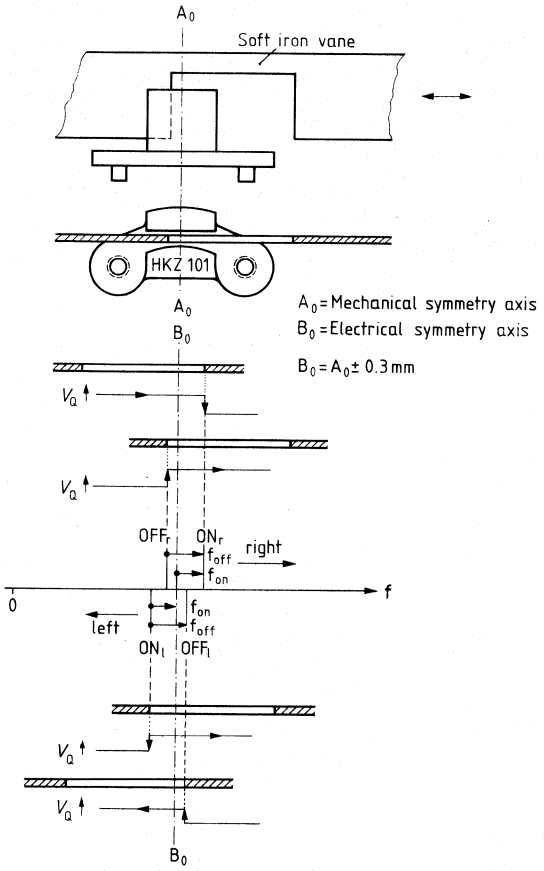
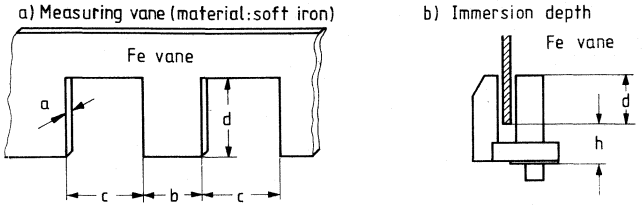


Figure 3
Mechanical Measurement Conditions



Switching Point Characteristics

Vane: a = 0.75 mm, b = 8 mm, c = 10 mm
Position: center of air gap
V_S = 5 V to 18 V

Description	Symbol	Test conditions	min	typ	max	Unit
HKZ 101						
Operate point	$f_{ON\,0}$	V_S = 12 V, T_A = 25 °C	0.85	1.45	2.05	mm
Deviations	Δf_{ON}	T_A = −30 to 25 °C	−0.4	+0.15	+0.7	mm
		T_A = 25 to 80 °C	−0.2	+0.15	+0.4	mm
		T_A = 80 to 130 °C	−0.4	+0.2	+0.7	mm
Release point	$f_{OFF\,0}$	V_S = 12 V, T_A = 25 °C	1.54	2.54	3.54	mm
Deviations	Δf_{OFF}	T_A = −30 to 25 °C	−0.8	+0.3	1.4	mm
		T_A = 25 to 80 °C	−0.4	+0.3	0.8	mm
		T_A = 80 to 130 °C	−0.8	+0.4	1.4	mm
HKZ 101 S[1])						
Operate point	$f_{ON\,0}$	V_S = 12 V, T_A = 25 °C	0.65		2.3	mm
Deviations	Δf_{ON}	T_A = −30 to 130 °C	−0.4		+0.75	mm
Release point	$f_{OFF\,0}$	V_S = 12 V, T_A = 25 °C	0.8		4.9	mm
Deviations	Δf_{OFF}	T_A = −30 to 130 °C	−0.4		+1.5	mm

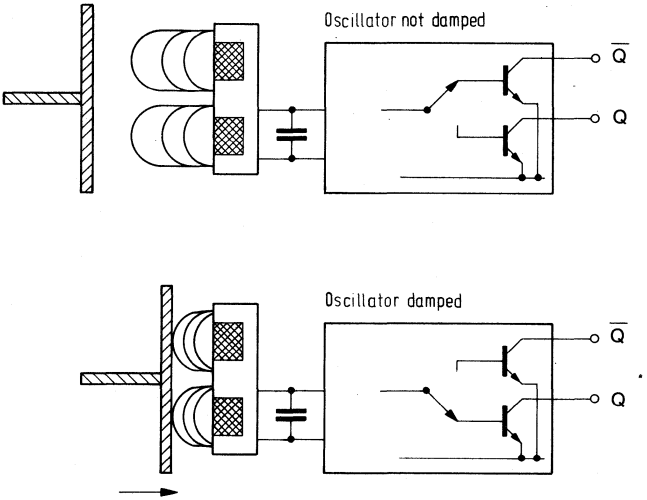
[1]) The switching-pint characteristics of the HKZ 101 S have been adapted to the extended temperature range.

Bipolar IC

Type	Ordering Code	Package
S ■TCA 205 A	Q67000-A1034	P-DIP-14
■TCA 205 K	Q67000-A8275	MIKROPACK, 14 connections (SMD)

This IC is intended for applications in inductive proximity switches. The outputs switch when the oscillation is damped, e.g. by the approach of a metal object.

Operation Schematic



Features

- Large supply voltage range
- High output current
- Antivalent outputs
- Adjustable switching distance
- Adjustable hysteresis
- Turn-on delay

■ Not for new design.

Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage Output voltage	V_S V_Q	30 30	V V
Output current	I_Q	50	mA
Junction temperature Storage temperature range	T_j T_{stg}	125 −55 to 125	°C °C
Thermal resistance system – air TCA 205 A	$R_{th\ SA}$	85	K/W

Operating Range

Supply voltage	V_S	4.75 to 30	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

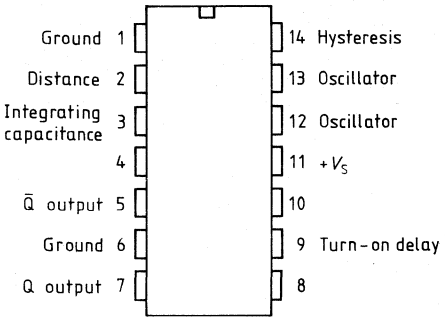
$V_S = 12$ V, $T_A = 25$ °C

Description	Symbol	Test conditions	min	typ	max	Unit
Open-loop supply current consumption	I_S	open pins		1	2	mA
L output voltage per output	$V_{Q\,L}$ $V_{Q\,L}$	$I_{Q\,L}$ = 5 mA $I_{Q\,L}$ = 50 mA		0.8 1.25	1 1.5	V V
H output current per output	$I_{Q\,H}$	$V_{Q\,H}$ = 30 V			10	µA
Integrating capacitance	C_I			10		nF
Internal resistance at 3	$R_{j\,3}$		200	350	660	kΩ
Threshold voltage at 3	$V_{S\,3}$			1.3	1.5	V
Distance adjustment Hysteresis adjustment } circuit 1	R_{di} R_{hy}		6 0			kΩ kΩ
Distance adjustment Hysteresis adjustment } circuit 2	R_{di} R_{hy}	$R_{hy} \rightarrow \infty$ $R_{di} \rightarrow \infty$	6[1]) 6[1])			kΩ kΩ
Turn-on delay	t_{don}			200		ms/µF
Oscillating frequency Switching frequency without C_I	f_{OSC} f_s		0.015		1.5 5	MHz kHz

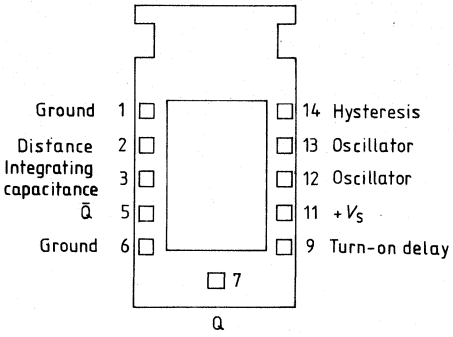
[1]) Parallel connection of R_{hy} to R_{di} may at least amount to 6 kΩ

Pin Configurations
(top view)

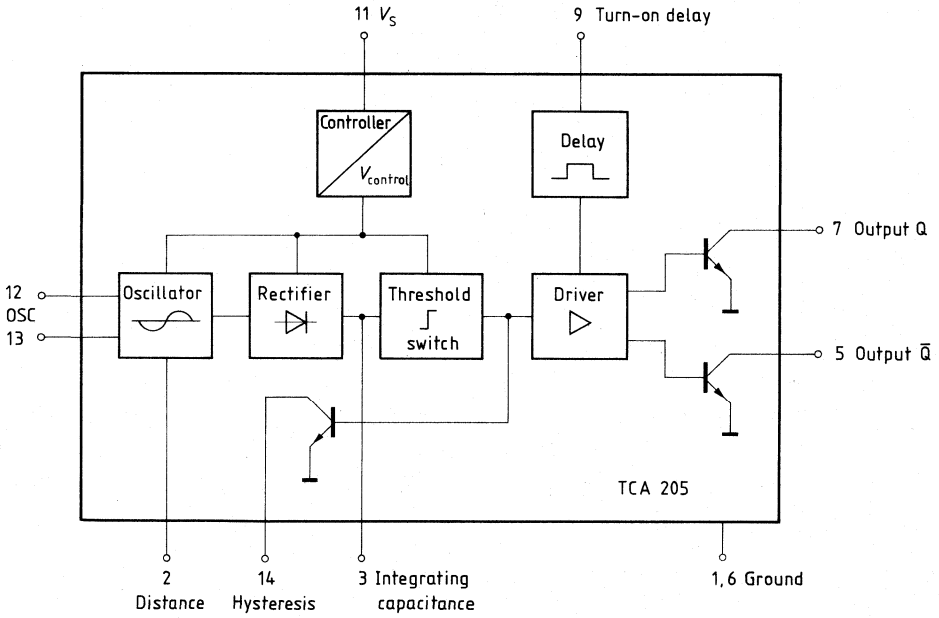
TCA 205 A



TCA 205 K

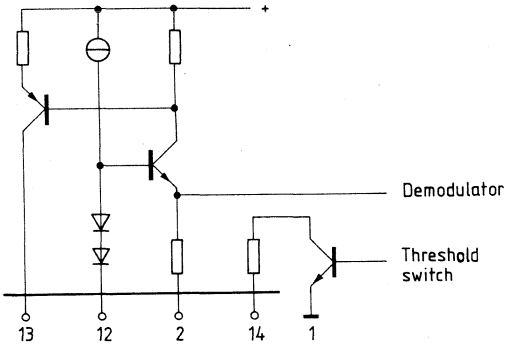


Block Diagram

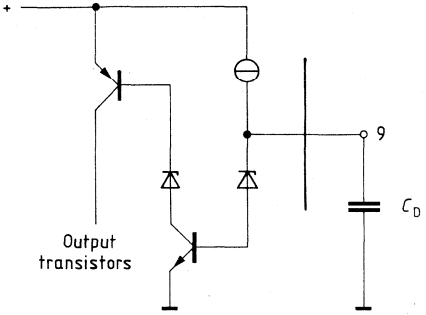


Schematic Circuit Diagrams

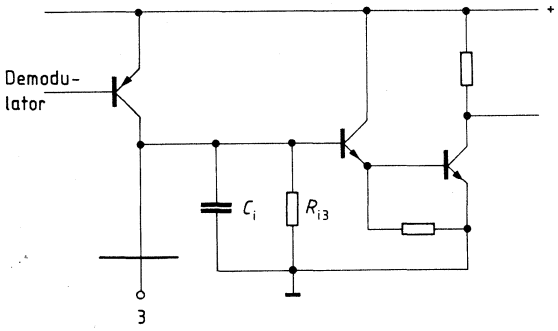
Oscillator



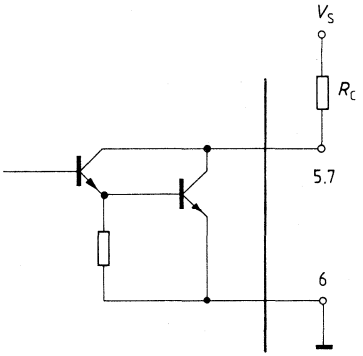
Turn-on delay



Integrating capacitor

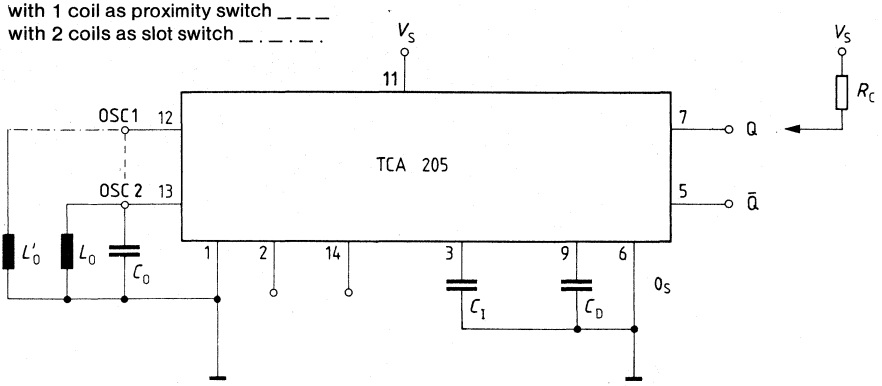


Outputs



Application Circuit

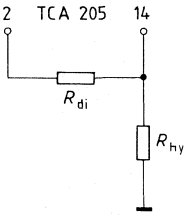
with 1 coil as proximity switch _ _ _
with 2 coils as slot switch _ . _ . _ .



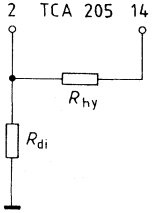
L_0, C_0	oscillator
R_{di}	distance adjustment
R_{hy}	hysteresis adjustment
C_I	integrating capacitor
C_D	delay capacitor

The resistance of distance and hysteresis R_{di} and R_{hy}, for proximity switch TCA 205 A; K may be applied as follows:

1. Series hysteresis



2. Parallel hysteresis

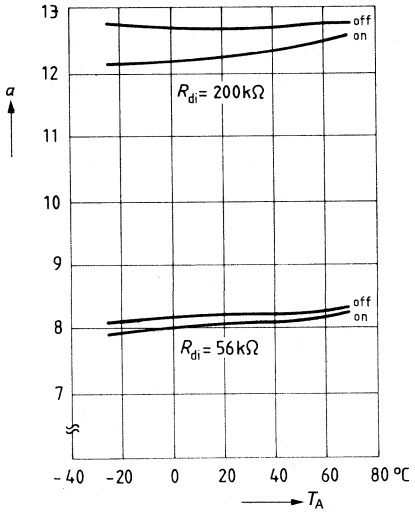


Circuit 1 is more suitable for proximity switches with oscillator frequencies of $f > 200$ kHz to 300 kHz, and small distances. Circuit 2 is more favorable for AF proximity switches having larger distances. This is due to the lower R_{hy} values enabled by circuit 1 (min. 0 Ω) compared with circuit 2 (min. 6 kΩ). Starting at frequencies of 200 kHz, high R_{hy} values effect in addition to the hysteresis also the oscillator phase. Practical applications, however, require little phase response to receive a clear evaluation.

Application Example for a Proximity Switch

Coil data	pot core B65939-A-X22 coil former B65940-A-M1 Ø = 25 mm x 8.9 mm L = 642 µH n = 100 CuLS 30 x 0.05	
Measuring plate	30 mm x 30 mm x 1 mm, Fe	
Circuitry	R_{di} = 56 to 200 kΩ, metal layer R_{hy} = ∞ C_0 = 1500 pF, STYROFLEX f = 162 kHz	circuit 2

Switching distance versus ambient temperature



Type	Ordering Code	Package
S TCA 305 A	Q67000-A2291	P-DIP-14
S TCA 305 G	Q67000-A2305	P-DSO-14 (SMD)
TCA 305 K	Q67000-A2293	MIKROPACK, 10 pins (SMD)
S TCA 355 B	Q67000-A2443	P-DIP-8
S TCA 355 G	Q67000-A2444	similar to SO-8 (SMD)

The devices TCA 305 and TCA 355 contain all the functions necessary to design inductive proximity switches. By approaching a standard metal plate to the coil, the resonant circuit is damped and the outputs are switched.

Operation Schematic: see TCA 205

The types TCA 305 and TCA 355 have been developed from the type TCA 205 and are outstanding for the following characteristics:

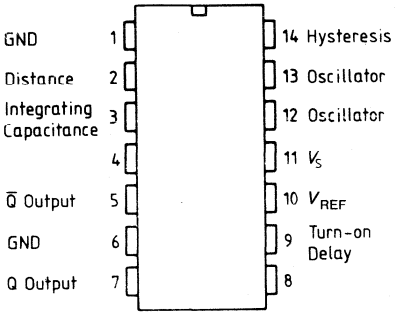
- Lower open-loop current consumption; $I_S < 1$ mA
- Lower output saturation voltage
- The temperature dependency of the switching distance is lower and the compensation of the resonant circuit *TC* (temperature coefficient) is more easily possible.
- The sensitivity is greater, so that larger switching distances are possible and coils of inferior quality can be used.
- The switching hysteresis remains constant as regards temperature, supply voltage and switching distance.
- The TCA 305 even functions without external integrating capacitance. With an external capacitance (or with RC combination) good noise suppression can be achieved.
- The outputs are temporarily short-circuit proof (approx. 10 s to 1 min depending on the package)
- The outputs are disabled when $V_S <$ approx. 4.5 V and they are enabled when the oscillator is working steadily (from $V_{S\,min} = 5$ V)
- Higher switching frequencies can be obtained.
- Miniature packages

Logic Functions

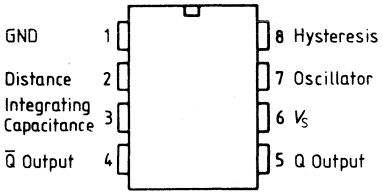
Oscillator	Outputs	
	Q	$\overline{Q}$
not damped	H	L
damped	L	H

Pin Configurations (top view)

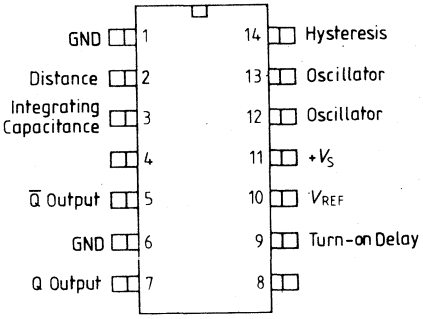
TCA 305 A



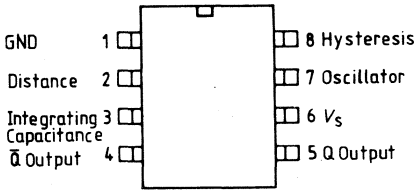
TCA 355 B



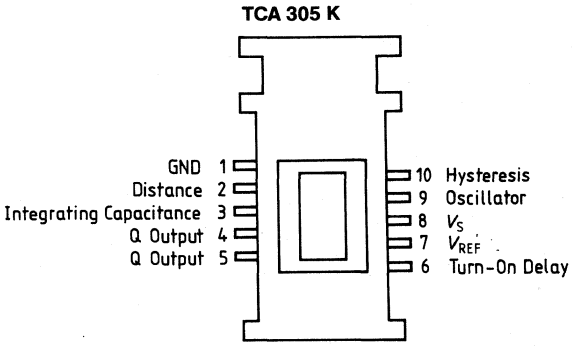
TCA 305 G



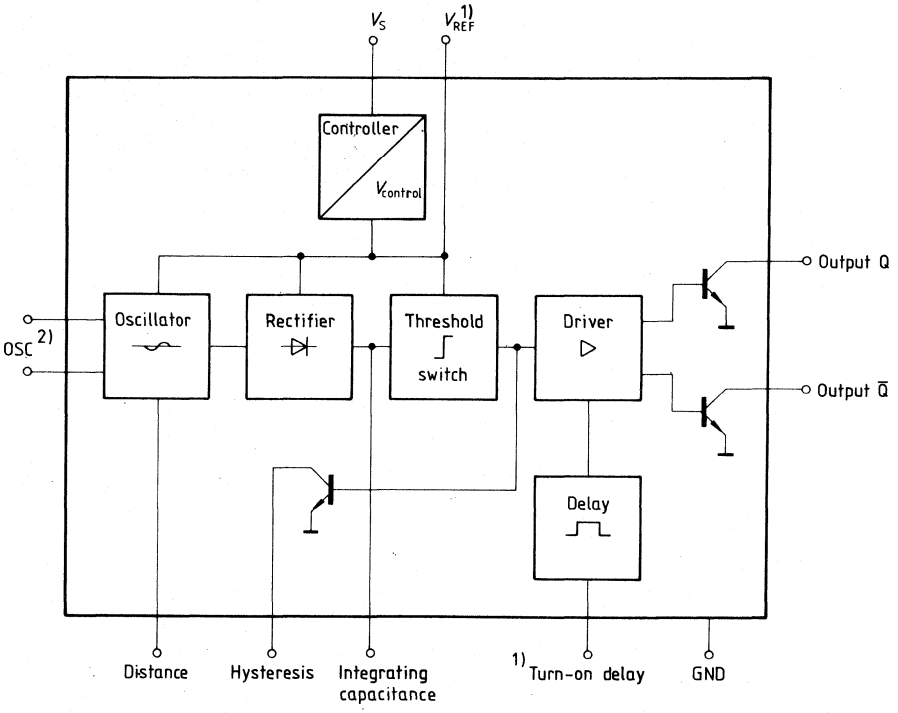
TCA 355 G



TCA 305 K



Block Diagram



1) TCA 305 only
2) Connected internally in case of TCA 355

Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage	V_S	35	V
Output voltage	V_Q	35	V
Output current	I_Q	50	mA
Distance, hysteresis resistance	R_{di}, R_{hy}	0	Ω
Capacitances	C_I, C_D	5	µF
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air TCA 305 A	$R_{th\ SA}$	85	K/W
TCA 305 G	$R_{th\ SA}$	140	K/W

Operating Range

Supply voltage	V_S	5 to 30[1])	V
Oscillator frequency	f_{OSC}	0.015 to 1.5	MHz
Ambient temperature	T_A	−25 to 85	°C

Chacarteristics

$V_S = 12$ V, $T_A = -25$ °C to +85 °C

Description	Symbol	Test conditions	min	typ	max	Unit
Open-loop current consumption	I_S	outputs open		0.6	0.9	mA
Reference voltage	V_{REF}	$I_{REF} < 10$ µA		3.2		V
L output voltage per output	$V_{Q\,L}$	$I_{Q\,L} = 5$ mA		0.04	0.15	V
	$V_{Q\,L}$	$I_{Q\,L} = 25$ mA		0.10	0.35	V
	$V_{Q\,L}$	$I_{Q\,L} = 50$ mA		0.22	0.75	V
H output current per output	$I_{Q\,H}$	$V_{Q\,H} = 30$ V			10	µA
Threshold at 3	$V_{S\,3}$			2.1		V
Hysteresis at 3	V_{hy}		0.4	0.5	0.6	V
Turn-on delay	$t_{D\,ON}$	$T_A = 25$ °C	−25%	600	−25%	ms/µF
Switching frequency w/o C_I	f_s				5	kHz

[1]) Operation at voltages less than 5 V (between approx. 2.5 and 5 V) is possible, if V_{REF} is connected to V_S. In this case V_{REF} is no longer internally stabilized. Additionally, the pin "turn-on delay" is to be applied as follows: If no turn-on delay is needed, this pin has to be connected to V_S. If, however, a turn-on delay is required, the charge current for C_D has to be adjusted with an external resistor between this pin and V_S (recommended value 390 kΩ).

Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage Output voltage	V_S V_Q	35 35	V V
Output current	I_Q	50	mA
Distance, hysteresis resistance	R_{di}, R_{hy}	0	Ω
Junction temperature Storage temperature range	T_j T_{stg}	125 −55 to 125	°C °C
Thermal resistance system – air TCA 355 B TCA 355 G	 $R_{th\ SA}$ $R_{th\ SA}$	 135 200	 K/W K/W

Operating Range

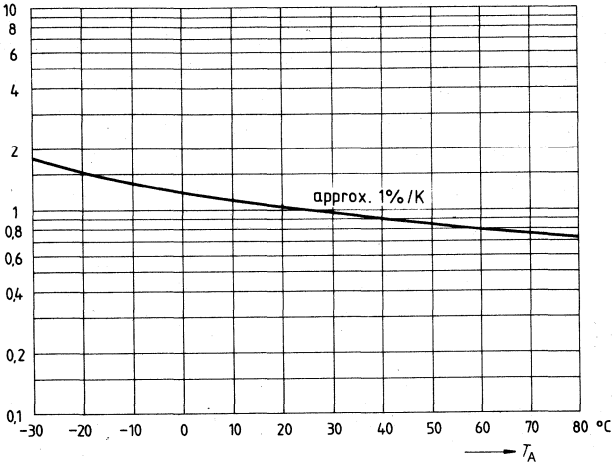
Supply voltage	V_S	5 to 30	V
Oscillator frequency	f_{OSC}	0.015 to 1.5	MHz
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = 12$ V; $T_A = -25$ °C to +85 °C

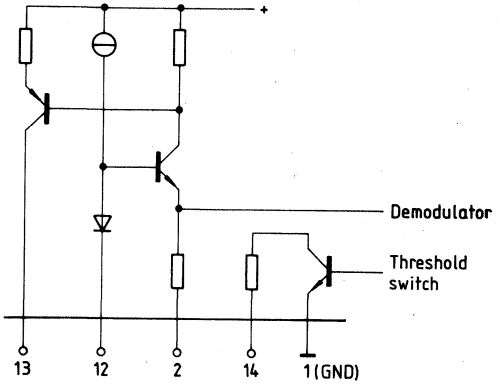
Description	Symbol	Test conditions	min	typ	max	Unit
Open-loop current consumption	I_S	outputs open		0.6	1.0	mA
L output voltage per output	V_{QL} V_{QL} V_{QL}	$I_{QL} = 5$ mA $I_{QL} = 25$ mA $I_{QL} = 50$ mA		0.04 0.10 0.22	0.15 0.35 0.75	V V V
H output reverse current per output	I_{QH}	$V_{QH} = 30$ V			10	µA
Threshold at 3 Hysteresis at 3	V_{S3} V_{hy}		 0.4	2.1 0.5	 0.6	V V
Switching frequency w/o C_I	f_s				5	kHz

Standard turn-on delay referred to $T_A = 25\,°C$

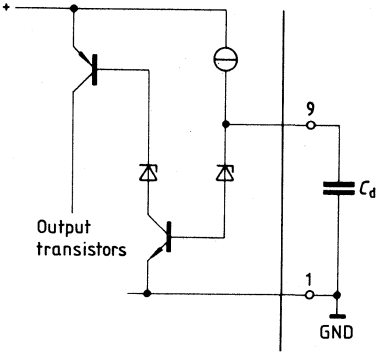


Schematic Circuit Diagrams

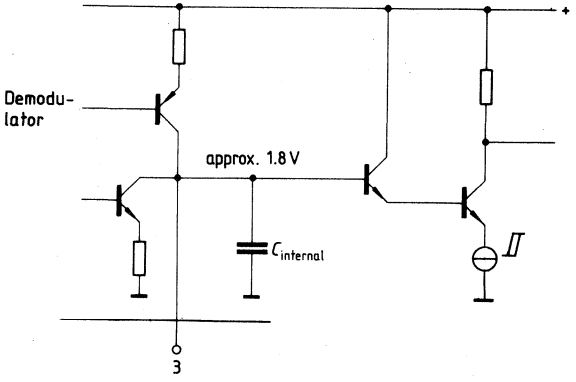
Oscillator



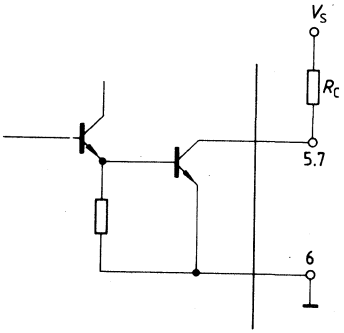
Turn-on delay for TCA 305 A; G



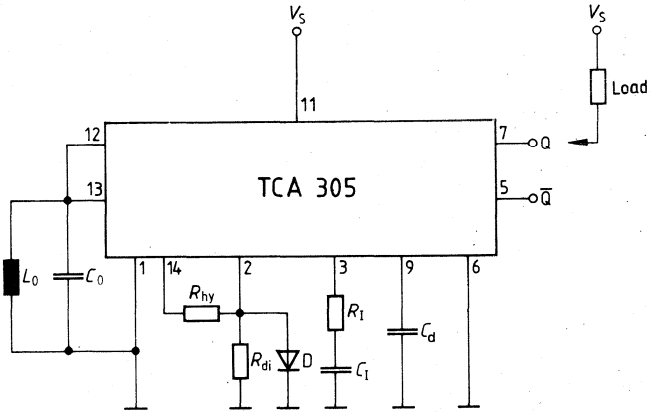
Integrating capacitor

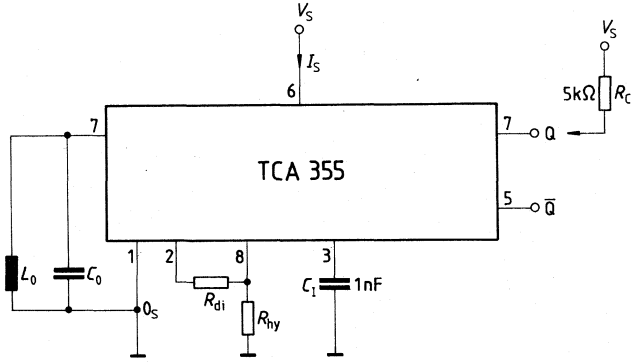


Outputs



Application Circuits





L_0, C_0	Resonant circuit
R_{hy}	Hysteresis adjustment
R_{di}	Distance adjustment
D	Temperature compensation of the resonant circuit; possibly with series resistance for the purpose of adjustment. The diode is not absolutely necessary. Whether it is used or not depends on the temperature coefficient of the resonant circuit.
R_I; C_I	Integration element. At pin 3 (integrating capacitance) we recommend a capacitor of typ. 1 nF. To increase noise immunity this capacitor can be substituted by an RC circuit with, e.g., $R_I = 1$ MΩ and $C_I = 10$ nF.
C_D	Delay capacitor

Dimensioning examples in accordance with CENELEC Standard (flush)

	M 12	M 18	M 30
Ferrite pot core	M33 (7.35x3.6) mm	N22 (14.4x7.5) mm	N22 (25x8.9) mm
Number of turns	100	80	100
Cross section of wire	0.1 CuL	20x0.05	10x0.1
L_0	206 µH	268 µH	585 µH
C_0 (STYROFLEX®)	1000 pF	1.2 nF	3.3 nF
f_{OSC}	appr. 350 kHz	appr. 280 kHz	appr. 115 kHz
Sn	4 mm	8 mm	15 mm
R_A (Metal)	8.2 kΩ + 330 Ω	33 kΩ	22 kΩ + 2.7 kΩ
C_D	100 nF	100 nF	100 nF

Type	Ordering Code	Package
TFA 1001 W	Q67000-A1357	Transparent miniature plastic package, 6 pins

The bipolar IC TFA 1001 W contains a photodiode and an amplifier. At its output (open NPN collector), the TFA 1001 W supplies a current directly proportional to the illuminance. A stabilized voltage of 1.35 V is available as a reference. Another pin permits a linearized characteristic curve at low illuminances and can be used to inhibit the output.

Applications

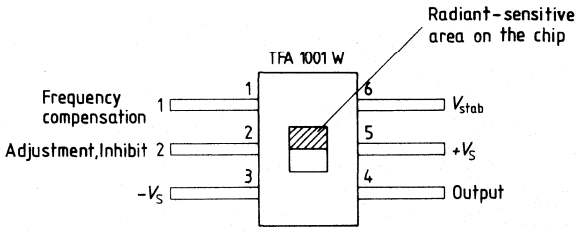
- Exposure meters
- Exposure control systems
- Electronic flashes
- Optical follow-up control
- Smoke detectors
- Linear optocouplers
- Color identification

Features

- High sensitivity
- High output current linearity
- Good spectral sensitivity
- Low current consumption
- Wide modulation range
- Large operating voltage range

Pin Configuration

(top view)



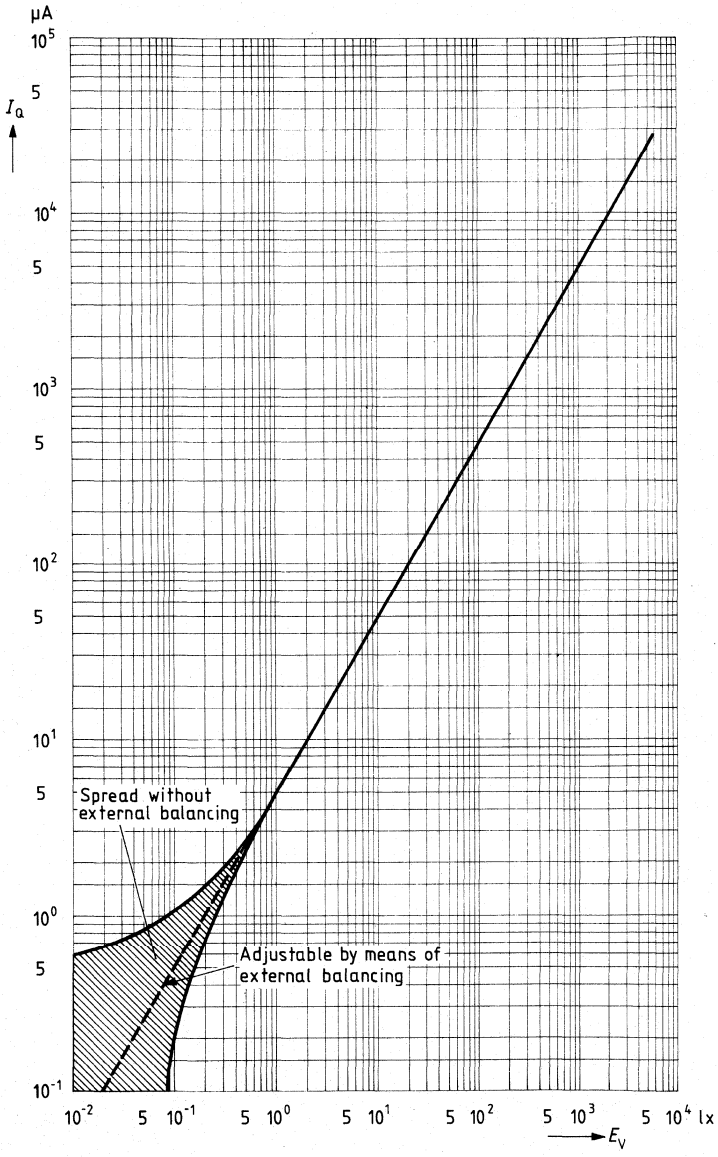
Maximum Ratings

Description	Symbol	min	max	Unit
Supply voltage	V_S		15	V
Output current	I_Q		50	mA
Power dissipation	P_{tot}		200	mW
Junction temperature	T_j		100	°C
Storage temperature	T_{stg}	−40	85	°C
Thermal resistance system – air	$R_{th\ SA}$		250	K/W

Characteristics at $T_A = 25$ °C, supply voltage applied to pin 5

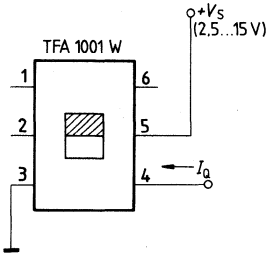
Description	Symbol	min	typ	max	Unit
Supply voltage	V_S	2.5		15	V
Current consumption at $E_v = 0$ lx	I_S	−10		1	mA
Ambient temperature	T_A			70	°C
Illuminance	E_v	0		5000	lx
Sensitivity in range $E_v = 1$ lx to 1000 lx	S	2.5	5	7.5	µA/lx
Output current at					
$E_v = 0.05$ lx	I_Q		0.25		µA
$E_v = 1$ lx	I_Q	2.5	5	7.5	µA
$E_v = 1000$ lx	I_Q	2.5	5	7.5	mA
$E_v = 5000$ lx	I_Q		25		mA
Stabilized voltage at pin 6	V_{stab}	1.2	1.35	1.5	V
Supply voltage dependence of stabilized voltage V_{stab}	$\Delta V_{stab}/\Delta V_S$		2		mV/V
Temperature dependence of stabilized voltage V_{stab}	$\Delta V_{stab}/\Delta T_A$		−0.3		mV/°C

Photocurrent versus illuminance

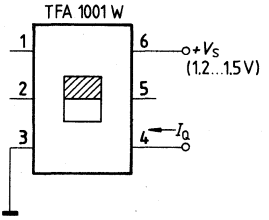


Possible Applications of TFA 1001 W as Light/Current Transducer

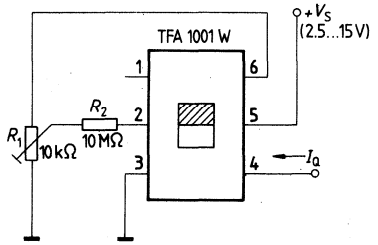
1) for operating voltage 2.5 to 15 V



2) for low operating voltage 1.2 to 1.5 V

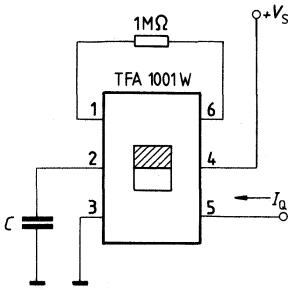


3) for especially low illuminance down to 0.01 lx

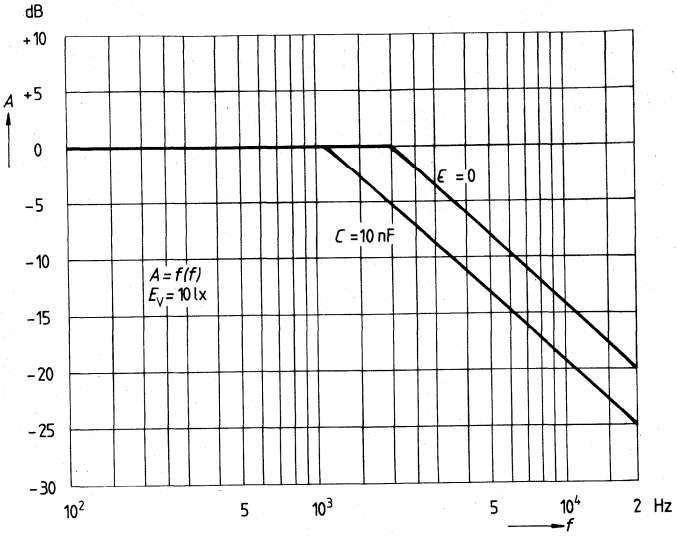


In case of low illuminance (see characteristic: output current versus illuminance), the output current can be balanced by means of the adjustment control R_1. The lower range of the output characteristic can be linearized even more by setting a dark current of about 5 nA.

Dynamic Behavior

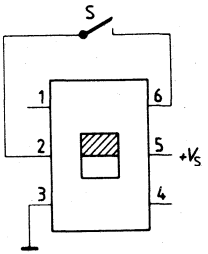


The dynamic behavior can be influenced at pin 2 by connecting capacitors.



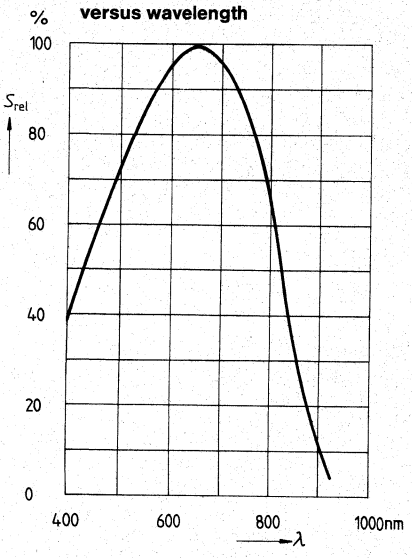
Attenuation $A = \dfrac{I_Q\,(f)}{I_Q\,(f=0)}$

Inhibiting the Output

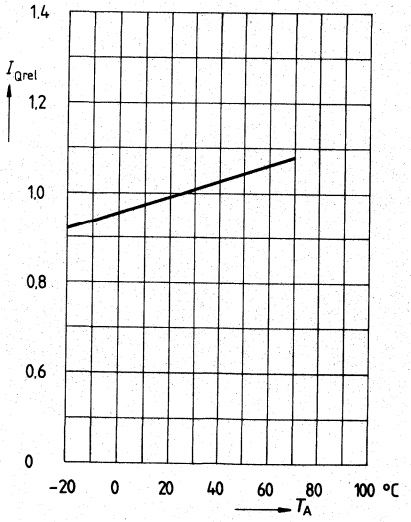


The output can be inhibited by connecting the balancing input with the stabilized voltage (switch, PNP transistor, FET).

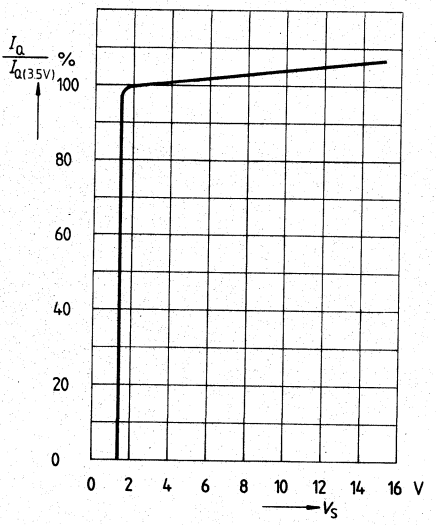
Relative spectral sensitivity versus wavelength



Relative output current versus ambient temperature
in range $E_v = 1$ lx to 1000 lx

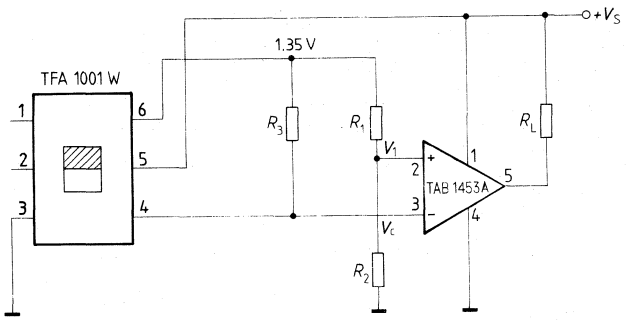


Output current versus supply voltage



Application Examples

Simple threshold switch with TAB 1453 A operational amplifier

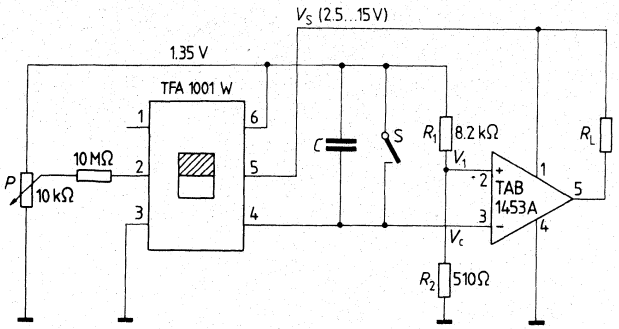


The illustration shows a simple threshold switch as can, for example, be used in cameras to change the aperture or indicate the illuminance. Operational amplifier TAB 1453 A serves as comparator. It has a PNP input and is able to operate at very low supply voltage.

The output is an open collector which can switch currents up to 70 mA.

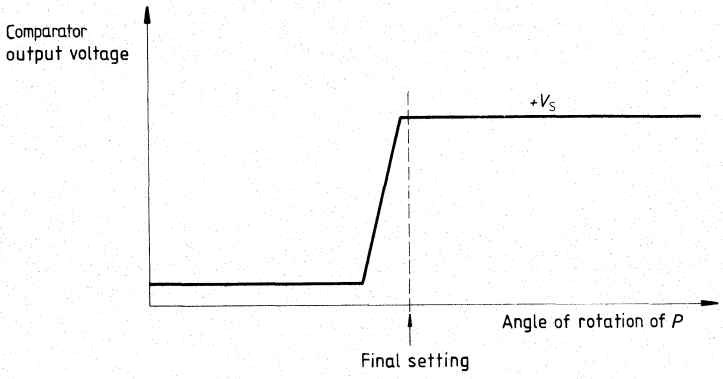
Since the stabilized voltage at pin 6 is used as reference voltage, the circuit is highly independent of the supply voltage.

Shutter Speed or Exposure Control

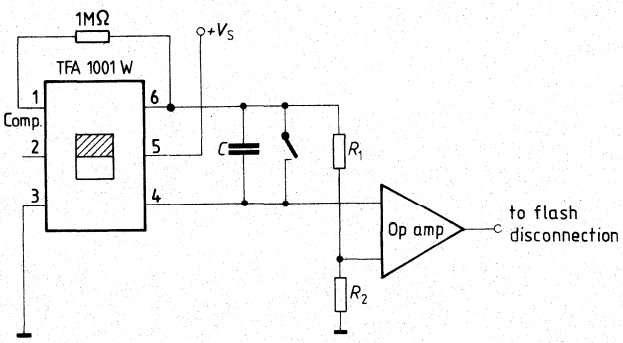


The above illustration shows a light/time control which can be used, for example, to control the shutter speed in cameras or for exposure time control in enlargers. The functioning of this circuit is also largely independent of the supply voltage. A further essential advantage is, that for the major part of the exposure time the comparator input current is insignificant as the corresponding input transistor remains fully off-state. By means of potentiometer P, the operating range can be extended to lower illuminance values. Opening the switch starts the exposure, and capacitor C is charged from pin 4 of the photo IC. The comparator switches if the voltage V_C falls below the reference voltage determined by resistors R_1 and R_2. The relationship between illuminance and time is defined by capacitor C and precision adjustment is possible by means of V_1; V_1, however, must not become less than 0.4 V.

The dark current may be set in the circuit by means of potentiometer *P*. For this purpose, capacitor *C* is removed. *P* is then adjusted in darkness such that the output of the comparator is just blocked. Capacitor C is then inserted. (See illustration below).

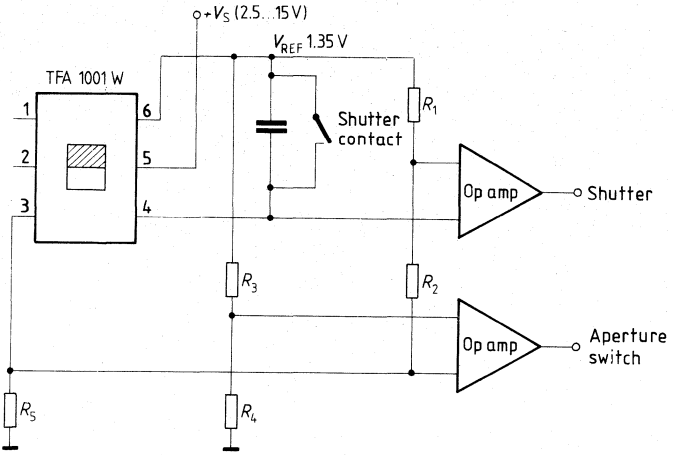


Schematic Circuit Diagram for an Electronic Flash Control



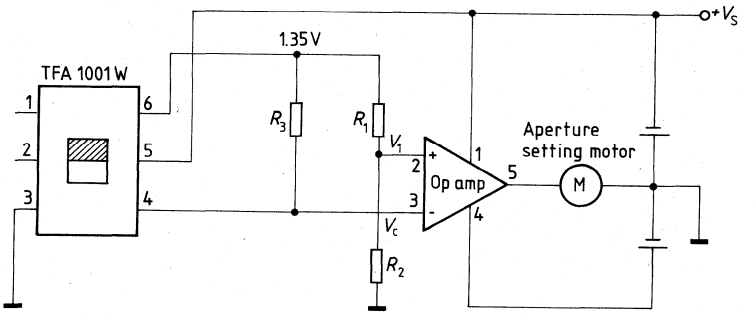
TFA 1001 W can also be used for electronic flash control. It must, however, be ensured that the illuminance does not exceed 5 klx; use a grey filter if necessary. To be able to control very short times, it is useful to connect an additional capacitor to pin 1.

Combined Aperture and Exposure Control



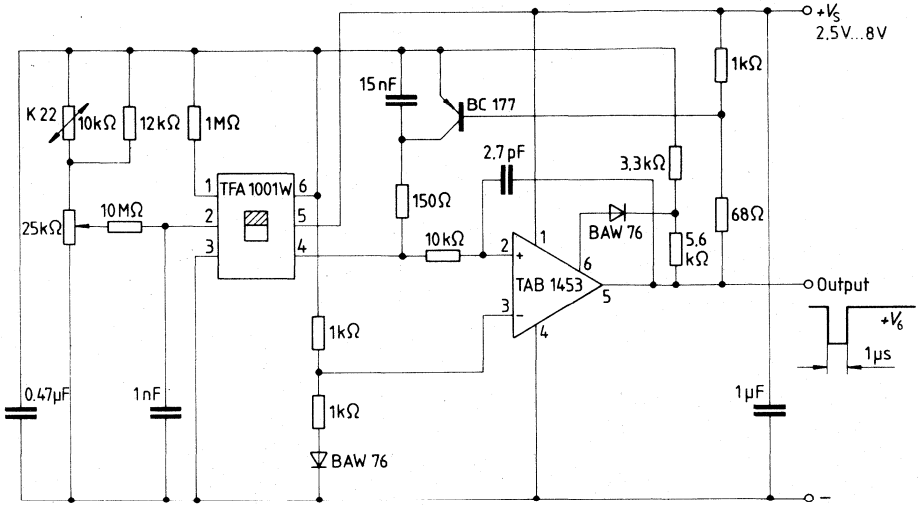
The aperture and exposure control may be combined, with the information for aperture switching being taken from the total current of the photo IC (voltage drop at R_5).

Aperture Follow-up Control for Cine Cameras



The op amp compares the voltage drop at R_3, generated by the photoelectric current, with a reference voltage derived from the stabilized voltage, and controls the aperture via motor M.

Light/Frequency Transducer



Sensitivity: approx. 600 Hz/lx
Range: 4 Hz to 400 000 Hz

- High resolution
- Fully temperature-compensated
- Wide operating voltage range
- High operating voltage suppression
- Wide dynamic range (5 decades)

Particularly suitable for digital processing.

Special CMOS SRAMs, Dual Port RAM

Selector Guide

Type	Package	Features		Temperature range
SAE 81C52 P SAE 81C52 G	P-DIP-16 P-DSO-20 (SMD)	Static CMOS RAM 256 x 8 bits	SAB 8051-compatible	−40...+ 85 °C
SAE 81C54 P SAE 81C54 G	P-DIP-16 P-DSO-20 (SMD)	Static CMOS RAM 512 x 8 bits	SAB 8051-compatible	−40...+110 °C
SAE 81C80 B	PL-CC-44 (SMD)	Dual Port RAM 504 x 8 bits	Multiprocessor system	−40...+110 °C

256 x 8 Bit Static CMOS RAM NMOS-Compatible

SAE 81C52

Preliminary Data

CMOS IC

Type	Ordering Code	Package
SAE 81C52 P	Q67100-H8003	P-DIP-16
SAE 81C52 G	Q67100-H8004	P-DSO-20 (SMD)

The SAE 81C52 is a CMOS silicon gate, static random access memory (RAM), organized as 256 words by 8 bits. The multiplexed address and data bus allows to interface directly to 8-bit NMOS microprocessors/microcomputers without any timing or level problems, e.g. the families SAB 8085, SAB 8086, SAB 8048, SAB 8051, and SAB 80515.

All inputs and outputs are fully compatible with NMOS circuits, except CS 1. Data retention is ensured up to $V_{DD} \geq 1.0$ V. The SAE 81C52 has three different inputs for two chip select modes which allow to inhibit either the address/data lines (AD 0...AD 7) and the control lines ($\overline{WR}$, $\overline{RD}$, ALE, CS 2, CS 3), or only the control lines $\overline{RD}$, $\overline{WR}$.

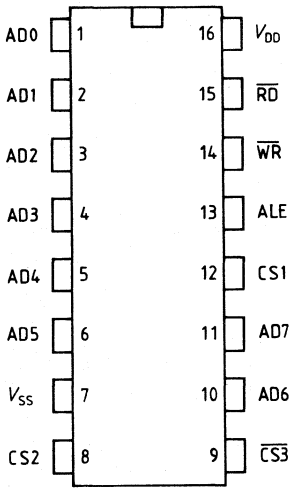
The power consumption is max. 5.5 µW in standby mode and max. 2.75 mW in operation. In standby mode, the power consumption will not increase if the control inputs are on undefined potential.

Features

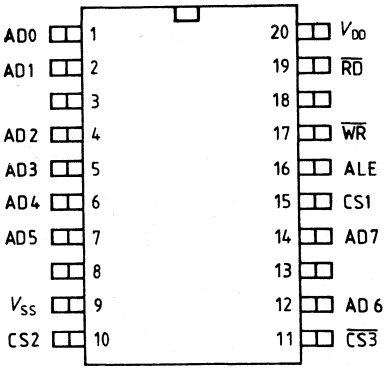
- 256 x 8-bit organization
- Standby mode
- Compatible with the µC/µP families SAB 8085, SAB 8086, SAB 8048, SAB 8051, SAB 80515, etc.
- Very low power dissipation
- Data retention up to $V_{DD} = 1$ V
- Three different chip select inputs for two chip select modes
- No increasing power consumption in standby mode if the control inputs are on undefined potential
- Temperature range −40 °C to +85 °C

Pin Configurations
(top view)

SAE 81C52 P



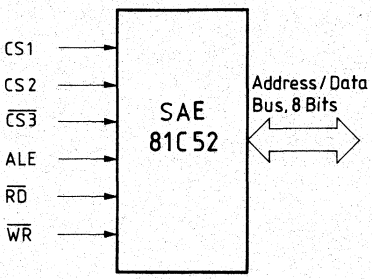
SAE 81C52 G



Pin Description

Pin		Symbol	Function
SAE 81C52 G	**SAE 81C52 P**		
1, 2, 4, 5, 6 7, 12, 14	1...6 10, 11	AD 0...7	Address/data lines
15	12	CS 1	Chip select 1 (standby) active low; inhibits all lines including control lines
16	13	ALE	Address latch enable
17	14	$\overline{WR}$	Write enable
19	15	$\overline{RD}$	Read enable
20	16	V_{DD}	Power supply
9	7	V_{SS}	GND (0 V)
10	8	CS 2	Chip select 2; inhibits control inputs $\overline{RD}$, $\overline{WR}$
11	9	$\overline{CS\ 3}$	Counterpart to CS 2

Logic Symbol

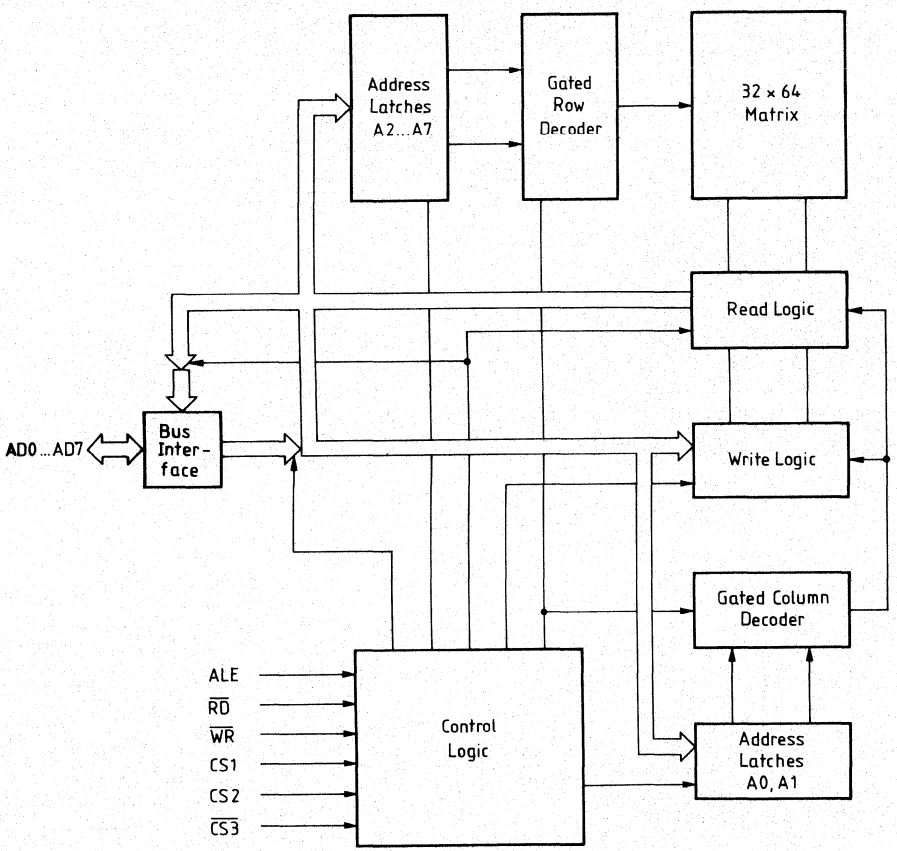


Truth Table

CS 1	CS 2	CS 3	ALE	RD	WR	AD 0...AD 7	Function
L	*	*	*	*	*	Floating (tristate)	Standby
H	X	X	H	H	H	Addresses to memory	Store addresses
H	H	L	L	L	H	Data from memory	Read
H	H	L	L	H	L	Data to memory	Write
H	L	X	L	X	X	Floating (tristate)	None
H	X	H	L	X	X	Floating (tristate)	None

*: Level = V_{SS}...V_{DD}
X: Level = LOW or HIGH

Block Diagram



Maximum Ratings

Description	Symbol	Ratings	Unit
Supply voltage referred to GND (V_{SS}) All input and output voltages	V_{DD} V_{IM}	−0.3 to 6 U_{SS} −0,3 V_{DD} +0.3	V V V
Total power dissipation Power dissipation for each output	P_{tot} P_Q	250 50	mW mW
Junction temperature Storage temperature	T_j T_{stg}	125 −55 to 125	°C °C
Thermal resistance system – air P-DIP-16 P-DSO-20	 $R_{th\ SA}$ $R_{th\ SA}$	 70 95	 K/W K/W

Operating Range

Supply voltage	V_S	4.5 to 5.5	V
Ambient temperature	T_A	−40 to 85	°C

DC Characteristics

$T_A = -40\,°C$ to $+85\,°C$; $V_{DD} = 4.5\,V$ to $5.5\,V$, $V_{SS} = 0\,V$

Description	Symbol	Test conditions	min	max	Unit
Standby supply current	I_{DD}			1	µA
Supply current	I_{DD}	$f = 1$ MHz		500	µA
Standby voltage for data retention	V_{DD}		1.0		V
L input current (for each input)	I_{IL}	$V_I = 0$ to V_{DD}		1	µA
Output leakage current	I_{QLK}	$V_Q = 0$ to V_{DD} tristate		1	µA
L input voltage	V_{IL}	except CS1		0.8	V
H input voltage	V_{IH}	except CS1	2.2		V
L output voltage	V_{QL}	$I_{QL} = 1$ mA		0.4	V
H output voltage	V_{QH}	$I_{QH} = 1$ mA	2.6		V
L input voltage CS1	V_{IL}			1	V
H input voltage CS1	V_{IH}		$V_{DD}-1$		V

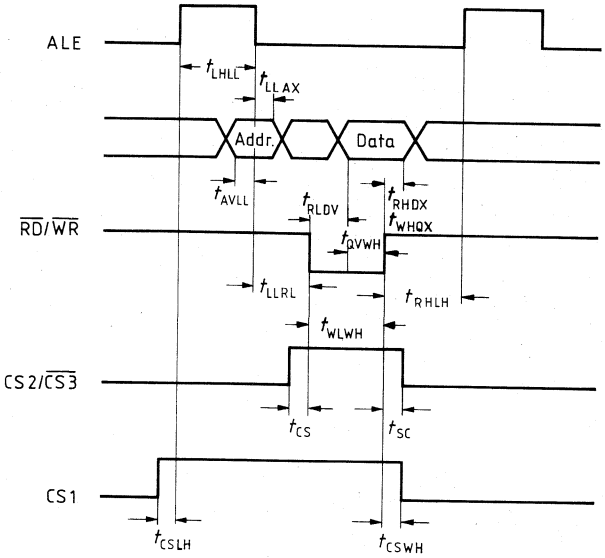
AC Characteristics

$T_A = -40\,°C$ to $+85\,°C$[1]); $V_{DD} = 4.5\,V$ to $5.5\,V$; $V_{SS} = 0\,V$

Description	Symbol	min	max	Unit
ALE pulse width	t_{LHLL}	100		ns
ALE LOW before $\overline{RD}$ LOW	t_{LLRL}	50		ns
$\overline{RD}$ HIGH before ALE HIGH	t_{RHLH}	30		ns
ALE LOW before $\overline{WR}$ LOW	t_{LLWL}	50		ns
$\overline{WR}$ HIGH before ALE HIGH	t_{WHLH}	30		ns
Address setup before ALE	t_{AVLL}	25		ns
Address hold after ALE	t_{LLAX}	20		ns
$\overline{WR}$ or $\overline{RD}$ pulse width	t_{WLWH}	250		ns
Data setup before $\overline{WR}$	t_{QVWH}	100		ns
Data hold after $\overline{WR}$	t_{WHQX}	30		ns
Data hold after $\overline{RD}$	t_{RHDX}		90	ns
Chip select (2, 3) before $\overline{RD}$, $\overline{WR}$	t_{CS}	50		ns
Chip select (2, 3) after $\overline{RD}$, $\overline{WR}$	t_{SC}	50		ns
Chip select 1 before ALE	t_{CSLH}	20		ns
Chip select 1 after $\overline{RD}$, $\overline{WR}$	t_{CSWH}	50		ns
Output delay time	t_{RLDV}		200	ns
Input capacitance to V_{SS} (for each input)	C_I		10	pF

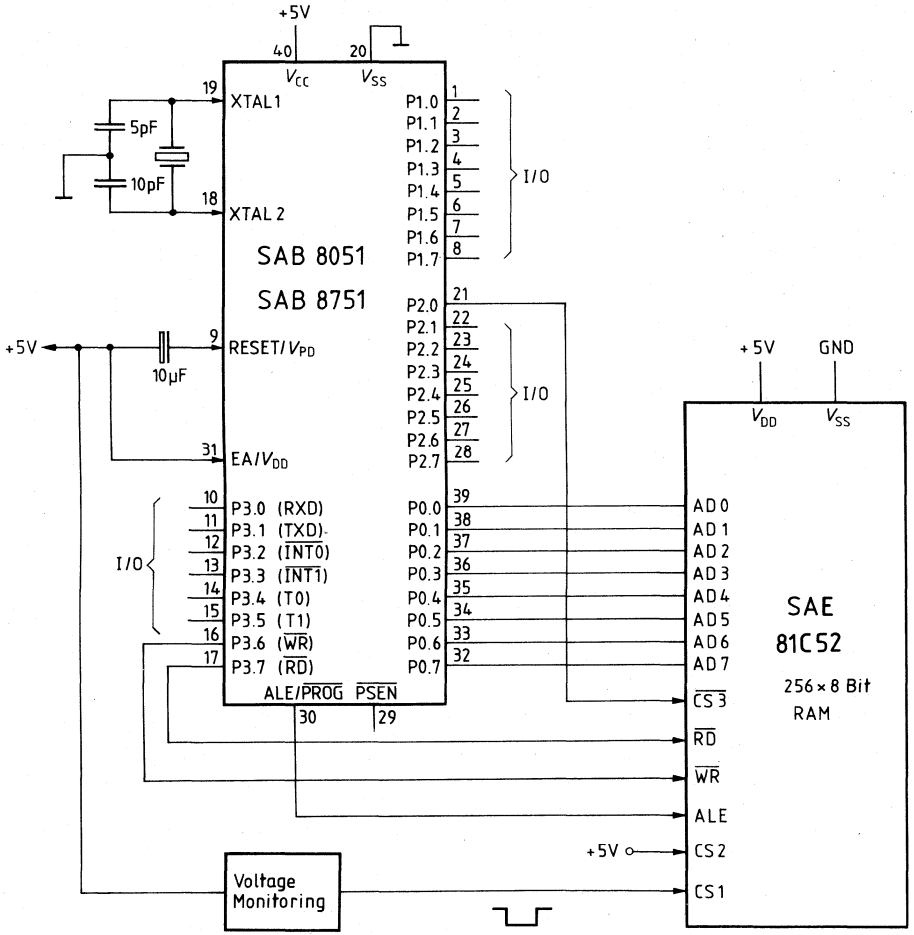
[1]) Values for applications up to 110 °C upon request

Timing Diagram



Application Circuit

SAE 81C52 with the µC SAB 8051



Preliminary Data **CMOS IC**

Type	Ordering Code	Package
SAE 81C54	Q67100-H8486	P-DIP-16
SAE 81C54 G	Q67100-H8487	P-DSO-20 (SMD)

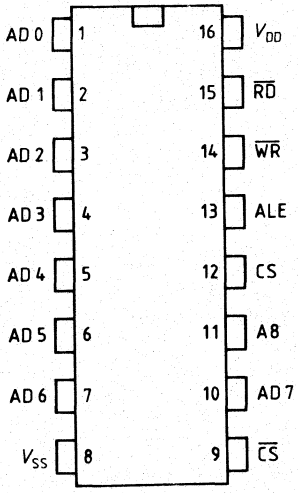
The SAE 81C54 is a static 4096-bit RAM (512 words by 8 bits) in advanced CMOS technology. The address and data bus in the multiplex operation allows direct connection to 8-bit microprocessors and computers, e.g. SAB 8085, SAB 8086, SAB 8088, SAB 8048, SAB 80C48, SAB 8051 and SAB 80C482. Due to its low power dissipation of less than 1 µA in standby mode this component requires only minimum supply current.

Features

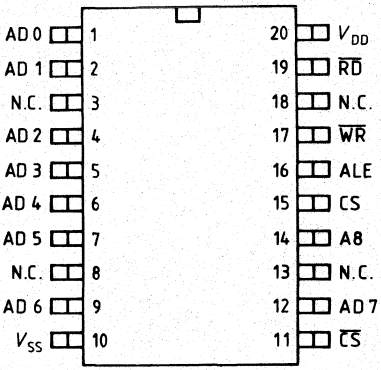
- 512 x 8 bit-organization
- Multiplexed address and data bus
- Tristate address and data lines
- On-chip address register
- Very low current consumption: 1 µA at 6 V during standby
- Dual chip selection
- Wide supply voltage range from 2.5 V to 6 V
- Fully compatible 5 V ± 10 %
- Data retention 1.0 V
- Package P-DIP-16 or P-DSO-20
- Temperature range from −40 °C to +110 °C

Pin Configurations
(top view)

SAE 81C54



SAE 81C54 G



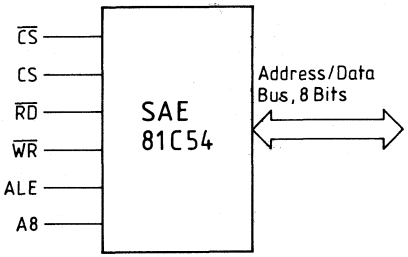
Pin Description

Pin		Symbol	Function
SAE 81C54	**SAE 81C54 G**		
1–7, 10	1, 2, 4-7, 9, 12	AD0–7	Address/data lines
8	10	V_{SS}	Ground
9	11	$\overline{CS}$	Chip select
11	14	A8	Address line
12	15	CS	Chip select
13	16	ALE	Address signal latch enable
14	17	$\overline{WR}$	Write enable
15	19	$\overline{RD}$	Read enable
16	20	V_{DD}	Supply voltage 2.5 to 6 V
	3, 8, 13, 18	N.C.	Not connected

Truth Table for Control and Data Bus Pin Status

$\overline{CS}$	CS	$\overline{RD}$	$\overline{WR}$	AD0-7 during data phase	Function
H	X	X	X	Floating	None
X	L	X	X	Floating	None
L	H	L	H	Data from memory	Read
L	H	H	L	Data to memory	Write

Logic Symbol



Maximum Ratings

Description	Symbol	Ratings	Unit
Ambient temperature	T_A	−40 to 110	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air P-DIP-16	$R_{th\ SA}$	70	K/W
P-DSO-20	$R_{th\ SA}$	95	K/W

DC Characteristics

$T_A = -40$ to $+85$ °C; $V_{DD} = 2.5$ to 6 V; $V_{SS} = 0$ V

Description	Symbol	Test conditions	min	typ	max	Unit
Standby supply current	I_{DD}				1	µA
Operating supply current	I_{DD}	100 kHz ALE		500		µA
Operating supply voltage	V_{DD}		2.5		6	V
Standby supply voltage	V_{DD}	Data retention	1.0		6	V
Input current	I_{IL}	V_I = 0-6 V			1	µA
Output leakage current	I_{QL}	V_Q = 0-6 V floating			1	µA
L input voltage ($V_{DD} < 4.5$ V)	V_I		−0.8		0.6	V
L input voltage ($V_{DD} > 4.5$ V)	V_{IL}		−0.8		0.8	V
H input voltage	V_{IH}		$0.6 \times V_{DD}$		$V_{DD}+0.8$	V
H input voltage	V_{IH}	$V_{DD} = 5$ V	2.0		$V_{DD}+0.8$	V
L output voltage ($V_{DD} < 4.5$ V)	V_{QL}	$I_{QL} = 1$ mA			0.4	V
L output voltage ($V_{DD} > 4.5$ V)	V_{QL}	$I_{QL} = 2$ mA			0.4	V
H output voltage ($V_{DD} < 4.5$ V)	V_{QH}	$I_{QH} = 1$ mA	$0.75 \times V_{DD}$			V
H output voltage ($V_{DD} > 4.5$ V)	V_{QH}	$I_{QH} = 2$ mA	$0.75 \times V_{DD}$			V

AC Characteristics

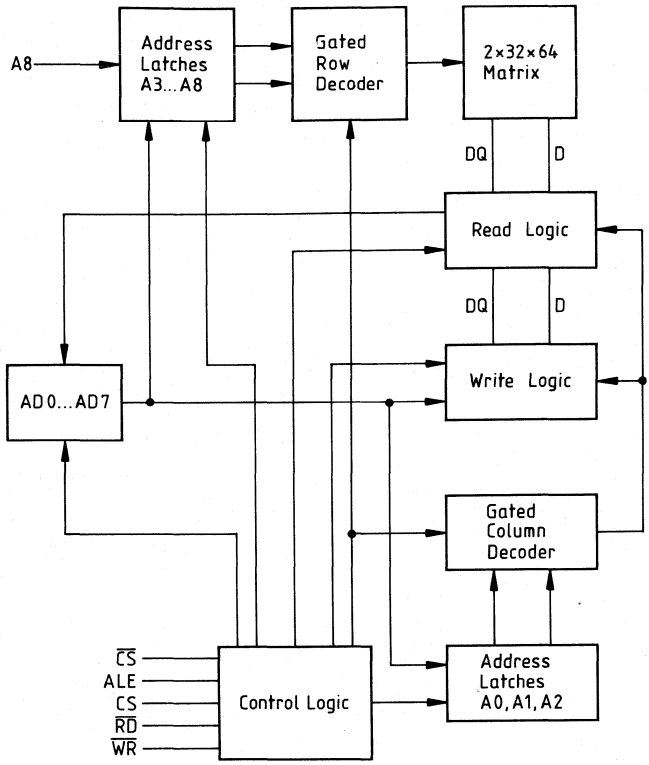
$T_A = -40$ to $+85$ °C; $V_{DD} = 4.5$ to 6 V; $V_{SS} = 0$ V

Description	Symbol	min	max	Unit
ALE pulse width	t_{LL}	40		ns
Address setup before ALE Address hold after ALE	t_{AL} t_{LA}	25 25		ns ns
$\overline{WR}$ pulse width $\overline{RD}$ pulse width	t_{CC} t_{CW}	60 130		ns ns
Data setup before $\overline{WR}$ Data hold after $\overline{WR}$ Data hold after $\overline{RD}$	t_{DW} t_{WD} t_{DR}	70 20	 30	ns ns ns
Access time $\overline{RD}$ to data output Address floating to $\overline{RD}$	t_{RD} t_{AFC}	 0	130	ns ns
CS before ALE CS after $\overline{WR}$ or $\overline{RD}$	t_{CS} t_{SC}	30 10		ns ns
ALE to $\overline{RD}$ or $\overline{WR}$ $\overline{RD}$ or $\overline{WR}$ to ALE = High	t_{LC} t_{CL}	35 25		ns ns

$T_A = -40$ to $+85$ °C; $V_{DD} = 2.5$ to 6 V; $V_{SS} = 0$ V

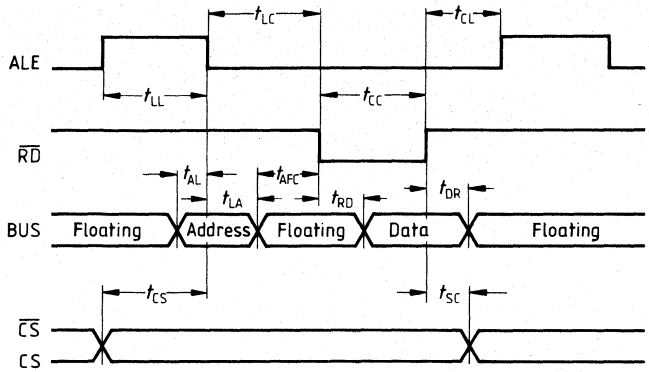
ALE pulse width	t_{LL}	60		ns
Address setup before ALE Address hold after ALE	t_{AL} t_{LA}	40 60		ns ns
$\overline{WR}$ pulse width $\overline{RD}$ pulse width	t_{CC} t_{CW}	200 350		ns ns
Data setup before $\overline{WR}$ Data hold after $\overline{WR}$ Data hold after $\overline{RD}$	t_{DW} t_{WD} t_{DR}	200 60	 95	ns ns ns
Access time $\overline{RD}$ to data output Address floating to $\overline{RD}$	t_{RD} t_{AFC}	 0	350	ns ns
CS before ALE CS after $\overline{WR}$ or $\overline{RD}$	t_{CS} t_{SC}	80 30		ns ns
ALE to $\overline{RD}$ or $\overline{WR}$ $\overline{RD}$ or $\overline{WR}$ to ALE = High	t_{LC} t_{CL}	60 30		ns ns

Block Diagram

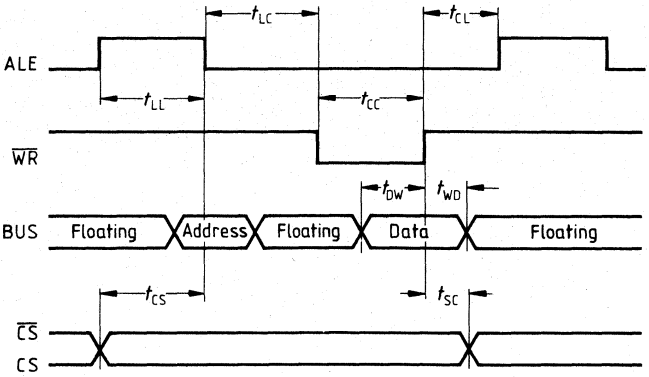


Diagrams

Read



Write



Preliminary Data **CMOS IC**

Type	Ordering Code	Package
SAE 81C80 B	Q67100-H8390	PL-CC-44 (SMD)

The SAE 81C80 B dual port RAM (DPR) is a CMOS memory IC with two processor interfaces and a capacity of 504 bytes. It enables the exchange of data between two microcontrollers without handshake signals and without wait states. Eight scheduling registers support the management of data areas or external resources.

Features

- Processor interface with multiplexed address and data bus as well as with signals ALE, $\overline{WR}$, $\overline{RD}$
- 8051 timing up to 10 MHz
- 8096 timing up to 9 MHz
- SAB 8086 family compatible (with wait states)
- Memory capacity 504 bytes
- All functions fully static
- Standby mode possible
- On-chip oscillator with separate clock output
- 8 scheduling registers
- 3 loadable timers for processor monitoring or as long-term timers
- Internal oscillator monitoring (hardware watchdog)
- 3 outputs to be set via the bus (e.g. to release an interrupt)
- Both processors can operate fully asynchronously
- Data retention down to 1 V
- Package PL-CC-44 for surface mounting
- TTL compatible
- Extended temperature range from −40 °C to +110 °C

Functional Description

The dual port RAM has a capacity of 504 bytes, which can be accessed by both processors. The memory locations are selected via a multiplexed address and data bus and two chip-select inputs. The $\overline{RD}$ and $\overline{WR}$ inputs determine the direction of data transfer. During simultaneous access to the same memory location no undefined states can occur, especially not in such cases, where both processors write to the same memory location. Depending on the internal status of the access control and of real physical sequence, the value will be stored by one of both the ports. Even during simultaneous reading of and writing to the same memory location there will be no mixing of data, i.e. either the previous data or the new data will be read.

Interrupt outputs

The dual port RAM has three outputs that can be directly set and reset by writing to an address (table 1). The interrupt outputs are located in the same address range as the scheduling registers. However, only bit 2 and bit 3 are relevant for the interrupt outputs.

In order not to affect the scheduling registers, at least one of the bits 0 or 1 should not be "1". The function of the outputs is shown in the following diagram:

$\overline{RES}$ pin	Bit 3	Bit 2	Output
1	0	0	No change
1	0	1	1
1	1	0	0
1	1	1	Undefined
0	–	–	0

For addresses of the interrupt outputs refer to table 1

Reset

The reset is necessary to set the DPR control circuits into a defined start state. During a reset, the timer mode registers are loaded with the value $0000XXX0_B$ (for timers 1 and 2) or $00000XX0_B$ (for timer 3). The $\overline{Int}$ outputs are set to "0".

While the reset input is low, outputs $\overline{WD1}$, $\overline{WD2}$ and $\overline{WD3}$ are set low. After the reset pulse, these outputs are high.

A reset is also necessary when the DPR is re-activated by the power-down mode. The contents of the RAM and the oscillator are not affected by the reset.

Power-down (standby)

When the power down pin is activated all inputs (except $\overline{PD}$ and XTAL1, XTAL2) and the oscillator are disabled, so that any levels are allowed at the remaining inputs.

Additionally, an active level at $\overline{PD}$ provides an internal reset. However, to ensure troublefree operation, the de-activation of the power-down mode should be followed by an external reset. The outputs of the ports change to a high-ohmic state, while the outputs CLKO, $\overline{WD0}$, $\overline{WD1}$, $\overline{WD2}$, $\overline{WD3}$, $\overline{INT1}$, $\overline{INT2}$ and $\overline{INT3}$ are set to low.

Scheduling Register

With a dual port RAM various access conflicts may occur:

- Simultaneous reading of the same memory location by both ports
- Simultaneous writing to the same memory location by both ports
- Reading of a logically correlated data area by one port while being changed by the other port.

The first two problems were solved by means of circuit engineering within the DPR. In view of the third problem the 8 scheduling registers represent an aid for the **software**.

Without these scheduling registers the data areas would have to be managed via a common memory location by access flags.

This, however, requires 3 accesses:

- First access: Read the flags and see whether the data area is free
- Second access: Set the flags for a reservation of your own
- Third access: Read the flags and check whether the reservation of your own has not been overwritten by the other port.

The use of the scheduling registers enables the synchronization with **one** access, since the reservation is done during reading and cannot be overwritten by the other port.

This means that the register is **written by reading** unless it was occupied.

These registers are no common memory locations – as described above – but they consist of a sequential logic system.

This sequential logic system has four states **(refer to figure 1)**:

- State 1: Port 1 was previous owner and the register is free
- State 2: Port 1 occupies the register
- State 3: Port 2 was previous owner and the register is free
- State 4: Port 2 occupies the register

The state of a register can be read out from the respective address; however, reading causes a subsequent change in state **(arrows in figure 1)**. During reading a 2-bit information is supplied:

- Bit 0 is the owner bit. It is set if the reading port is or was owner of the register
- Bit 1 is the "occupied" bit. It is set if the register was reserved by a port
- Bit 2 to bit 7 are always 0.

The reservation is performed by reading the register and the enable by writing with $XXXXXX11_B$ (taking the interrupt outputs of bits 2 and 3 into consideration). Thus, when using the scheduling register, a correct listing must comprise the following steps:

1 Read the scheduling register
2 Check whether the "occupied" bit is set and the owner bit is not set
  If it is not, back to 1, otherwise proceed with 3
3 Process data area
4 Enable the scheduling register by writing the value 03_H to the address of the register
5 End

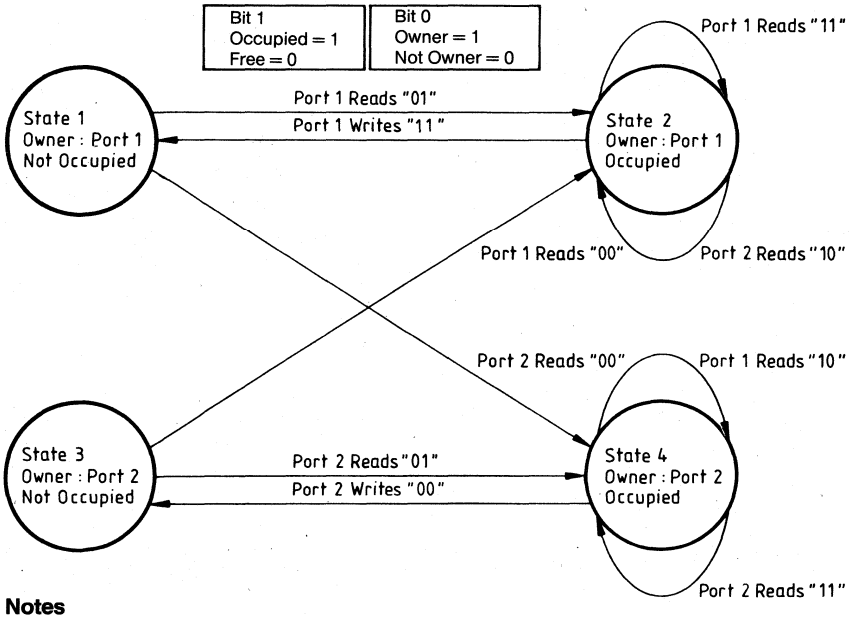
In cases where processing of the data area would be inefficient unless the other processor had access first, this can be initiated by separate evaluation of the "occupied" bit and the owner bit of step 2.

2a Owner bit set? If so, proceed with 5, otherwise with 2b
2b "occupied bit" set? If so, back to 1, otherwise proceed with 3.

Upon simultaneous access by both ports writing is done prior to reading and upon uniform access (both ports read or both ports write) port 1 is given priority to port 2.

For the addresses of the scheduling registers refer to **table 1**.

Figure 1
Status diagram of the scheduling registers
(Concerning the data, only the two "LSBs" are shown in quotation marks)



Notes

[1]) The owner bit indicates who accessed the register last.
[2]) Writing changes the state only if the respective port is "owner" of the register.

Oscillator Watchdog

Whenever the clock frequency drops below a threshold of approx. 100 kHz this output switches to low-potential.

Timer

The three timers are 24-bit counters with a clock frequency of $f_{OSC}/6$. Each counter can be set by writing to 3 specific RAM addresses. The value is simultaneously stored in the RAM

and in a buffer register of the timer. When writing to the low byte all three bytes are transferred in parallel to the reload register. The value in the reload register is maintained in all operating modes until the corresponding low byte is written again. The counters are down counters. The counters can be started by setting bit 7 in the corresponding TMR. Additionally, counter 3 can be started by an external trigger signal TS3, (bit 6 must be reset in the TMR). Each counter can be configured by a timer mode register (TMR). The bits of the TMR have the following meaning:

Bit 0: Protects the reload register against overwriting.
Application: After having written to the reload registers and having started the timer, the parallel RAM area can be used – by writing to the corresponding protection bit – without influencing the reload register (reset stage = 0).

Bit 4: Serves to switch over the output signal polarity (reset state = 0)
Bit 4 = 0; idle state 1, active 0
Bit 4 = 1; idle state 0, active 1

Bit 5: Selects the operating mode (reset state = 0):
Bit 5 = 0 single shot, i.e. when the counter is started the output signal becomes active. After zero has been reached, the output signal returns to idle. To generate another count period the timer must be started again. Thereby the values from the reload register are loaded into the counter.

Bit 5 = 1 auto reload, i.e. the value of the reload register is loaded into the counter when the counter is started. When reaching zero, the counter outputs a pulse ($\sim 48\ t_{OSC}$) and reloads the old value automatically, thus starting the process again, so that a frequency with a 24-bit resolution can be set (shortest period 54 t_{OSC}). If a new start pulse occurs during the count period (even without "STOP"), no pulse is output and the counter is reloaded.

Bit 6: In the reload mode the timer can be stopped by setting this bit (bit 5 must be 0). (During a new start the contents of the counter are lost, but not the contents of the reload registers).

Bit 7: Setting this bit starts the counter.

Only for the registers of timer 1 and 2

Bit 1 to 3: Are used in connection with bit 0 for switching watchdog mode on or off.

Only for the register of timer 3

Bit 1 to 2: Reserved (must always be 0 for proper operation)

Bit 3: Switches **all 3** timers to test mode, i.e. only the upper 12 bits are used to generate the output signal (reset state = 0).

Watchdog Mode

A special mode is provided for timers 1 and 2; it can be used for monitoring the two processors that are connected. In this operating mode an additional register **(for addresses see table 1)** – in the following referred to as control register (CR) – is employed for each timer. The watchdog mode is set by loading the TMR with the value "$101X1111_B$", the polarity of the output signal being freely selectable with bit 4. This mode operates in a similar manner as the auto-reload mode, except that in this case neither the contents of the reload register nor the TMR can be changed.

In the watchdog mode the timer can only be restarted (thus suppressing the output pulse) when first 055_H and then $0AA_A$ are written into the control register. There is no time limit between these two write accesses, however, between these two operations no other value must be written into the timer mode register or into the control register, otherwise the sequence must be started again.

In order to reset the timer into normal mode, the following sequence must be performed: first the value 055_H must be written into the control register, then the value $011X0000_B$ into the TMR and finally the value $0AA_H$ into the control register. If any other value is written into one of the two registers within this sequence, the operation must be started over again. There is no time limit between the accesses.

For operation of the timer in watchdog mode refer to page 861 (example program for the SAB 8051).

Figure 2
Bit assignment of the timer mode register for timer 1 and timer 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Software start (= 1)	Timer stop (= 1) for auto-reload	Mode (auto-reload = 1 single shot = 0)	Polarity of the output pulse (high = 0)	Only for watchdog mode (normal mode = 0)	Only for watchdog mode (normal mode = 0)	Only for watchdog mode (normal mode = 0)	Protection (= 1) protects the reload register against overwriting

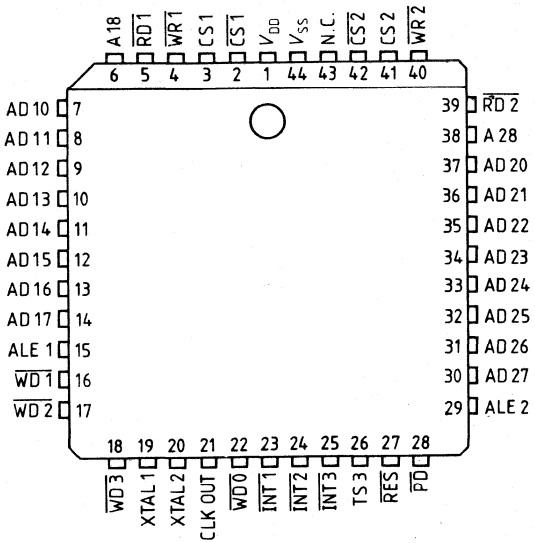
Figure 3
Bit assignment of the timer mode register for timer 3

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Software start (= 1)	Timer stop (= 1) for auto-reload	Mode (auto-reload = 1 single shot = 0)	Polarity of output pulse (high = 0)	Test (= 1) switches timer into test mode	Reserved (normal mode = 0)	Reserved (normal mode = 0)	Protection (= 1) protects the reload register against overwriting

Table 1
Address assignment of the DPR registers

Register		Address
Scheduling register	1	$1F8_H$
Scheduling register	2	$1F9_H$
Scheduling register	3	$1FA_H$
Scheduling register	4	$1FB_H$
Scheduling register	5	$1FC_H$
Scheduling register	6	$1FD_H$
Scheduling register	7	$1FE_H$
Scheduling register	8	$1FF_H$
Timer mode register	1	$1E0_H$
Timer mode register	2	$1E4_H$
Timer mode register	3	$1E8_H$
High byte timer	1	$1E3_H$
Medium byte timer	1	$1E2_H$
Low byte timer	1	$1E1_H$
High byte timer	2	$1E7_H$
Medium byte timer	2	$1E6_H$
Low byte timer	2	$1E5_H$
High byte timer	3	$1EB_H$
Medium byte timer	3	$1EA_H$
Low byte timer	3	$1E9_H$
Control register timer	1	$1EC_H$
Control register timer	2	$1ED_H$
Interrupt output	1	$1F8_H$
Interrupt output	2	$1F9_H$
Interrupt output	3	$1FA_H$

Pin Designation
(top view)



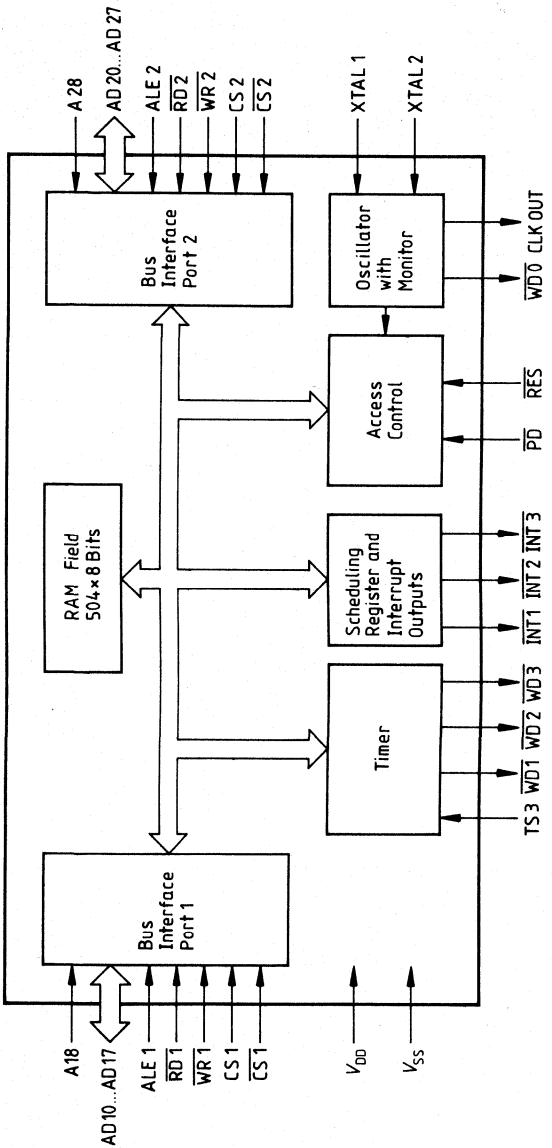
Pin Description

Pin	Symbol	Function
7 8 9 10 11 12 13 14	AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17	Data and address bus port 1
6	A18	Address 8 port 1
37 36 35 34 33 32 31 30	AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27	Data and address bus port 2
38	A28	Address 8 port 2
15 29	ALE1 ALE2	Address latch enable port 1 Address latch enable port 2 These signals serve to separate data from addresses on the bus The address is stored on the falling edge of the signal
5 39	$\overline{RD1}$ $\overline{RD2}$	Read signal port 1 (active low) Read signal port 2 (active low)
4 40	$\overline{WR1}$ $\overline{WR2}$	Write signal port 1 (active low) Write signal port 2 (active low)
3 2	CS1 $\overline{CS1}$	Chip select port 1 Chip select port 1 (active low)
41 42	CS2 $\overline{CS2}$	Chip select port 2 Chip select port 2 (active low) The chip select inputs select a port when both inputs have active level
27	$\overline{RES}$	Reset input Resets the IC to a defined start state if $\overline{RES}$ is low. Simultaneously the outputs $\overline{WDO}$, $\overline{WD1}$, $\overline{WD2}$, $\overline{WD3}$ are switched to low level for the duration of the reset pulse. The oscillator is not affected.

Pin Description

Pin	Symbol	Function
28	$\overline{PD}$	Power down (active low) Disables all inputs and the oscillator
44 1	V_{SS} V_{DD}	Negative supply voltage Positive supply voltage
43	NC	Not connected
19 20	XTAL1 XTAL2	Quartz connection (must be open for external clock supply) Quartz connection or external clock supply
21	CLK OUT	Clock output
22	$\overline{WDO}$	Oscillator watchdog (open drain output) High level indicates that oscillator is in operation
16 17 18	$\overline{WD1}$ $\overline{WD2}$ $\overline{WD3}$	(Open drain output) (Open drain output) (Open drain output) } Outputs of the 3 timers
26	TS3	Hardware signal to start timer 3
23 24 25	$\overline{INT1}$ $\overline{INT2}$ $\overline{INT3}$	(Open drain output) (Open drain output) (Open drain output) Outputs that can be controlled via the port to generate an interrupt at one of the processors, for example.

Block Diagram



Maximum Ratings

(All voltages referred to V_{SS})

Description	Symbol	min	typ	max	Unit
Supply voltage Input voltage	V_{DD} V_I	−0.3 −0.3		6 V_{DD} +0.3	V V
Total power dissipation Power dissipation per output	P_{tot} P_Q			500 50	mW mW
Storage temperature	T_{stg}	−50		125	°C

Operating Range

Supply voltage	V_{DD}	4.5	5	5.5	V
Supply current (without output loading)	I_{DD}			20	mA
Operating frequency	f_S			10	MHz
Standby current	I_{DD}			1	µA
Data retention voltage	V_{DH}	1			V
Ambient temperature	T_A	−40		110	°C

DC Characteristics

$T_A = 25\,°C$

Description	Symbol	Measuring conditions	min	typ	max	Unit
All input signals except XTAL2						
H input voltage	V_{IH}		2.2		$V_{DD}+0.3$	V
L input voltage	V_{IL}		$V_{SS}-0.3$		0.8	V
Input capacitance	C_I				10	pF
Input current	I_I				1	µA
XTAL2 (as external clock input)						
H input voltage	V_{IH}		3.5		$V_{DD}+0.3$	V
L input voltage	V_{IL}		$V_{SS}-0.3$		0.5	V
Input capacitance	C_I				10	pF
Output signals AD10-17, AD20-27						
H output voltage	V_{QH}	$I_Q = 0.5$ mA	2.4		V_{DD}	V
L output voltage	V_{QL}	$I_Q = 1.6$ mA			0.4	V
Output signals $\overline{WD1}$, $\overline{WD2}$, $\overline{WD3}$, $\overline{WDO}$ (Open drain outputs)						
L output voltage	V_{QL}	$I_Q = 1.6$ mA			0.4	V
Output signal CLK OUT						
H output voltage	V_{QH}	$I_{QH} = 0.5$ mA	2.4			V
L output voltage	V_{QL}	$I_{QL} = 1.6$ mA			0.4	V
Load capacitance	C_L				80	pF

AC Characteristics

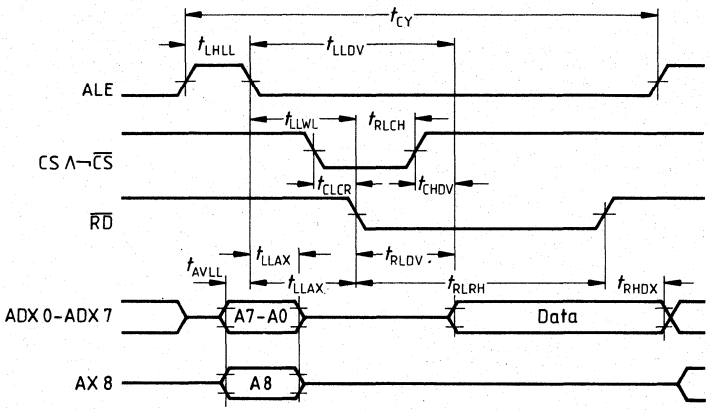
$T_A = 25\,°C$

Description	Symbol	min	max	Unit
Cycle time	t_{CY}	6 t_{OSC}		ns
ALE pulse width	t_{LHLL}	60		ns
Address setup to ALE low	t_{AVLL}	30		ns
Address hold after ALE low	t_{LLAX}	40		ns
$\overline{RD}$ pulse width	t_{RLRH}	2 t_{OSC} +20		ns
$\overline{WR}$ pulse width	t_{WLWH}	2 t_{OSC} +20		ns
ALE low to $\overline{RD}$ or $\overline{WR}$ active	t_{LLWL}	60		ns
$\overline{RD}$ active to valid data out (Chip-selects are active)	t_{RLDV}		2 t_{OSC}[1])	ns
CS active to valid data out ($\overline{RD}$ is active)	t_{CHDV}		2 t_{OSC} −40	ns
Data hold after $\overline{RD}$ high	t_{RHDX}	0	30	ns
ALE low to valid data out	t_{LLDV}		3 t_{OSC} +80	ns
Valid data in after $\overline{WR}$ low	t_{DVWL}		1/2 t_{OSC}	ns
$\overline{WR}$ low to ALE high	t_{WLLL}	3 t_{OSC} +20		ns
Data setup before $\overline{WR}$ high	t_{QVWH}	30		ns
Data hold after $\overline{WR}$ high	t_{WHQX}	40		ns
Delay $\overline{RD}$ low to both Chip select active	t_{RLCH}		40	ns
Delay $\overline{WR}$ low to both Chip select active	t_{WLCH}		40	ns
Setup of chip select to $\overline{RD}$	t_{CLRL}	0		ns
Setup of chip select to $\overline{WR}$ (for disable)	t_{CLWL}	0		ns
Active pulse length of timer outputs	t_{ACT}	48 t_{OSC}		ns
Pulse width of TS 3	t_{THTL}	2 t_{OSC}		ns
Oscillator period	t_{OSC}	83		ns
High time	t_{OSCH}	40		ns
Low time	t_{OSCL}	40		ns
Rise time	t_r		40	ns
Fall time	t_f		40	ns

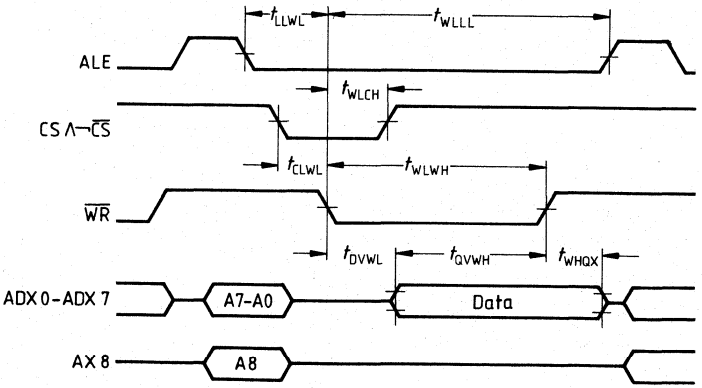
[1]) applies only to $t_{LLWL} > t_{OSC} + 80$ ns

Pulse Diagrams

Read cycle

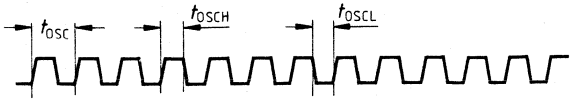


Write cycle



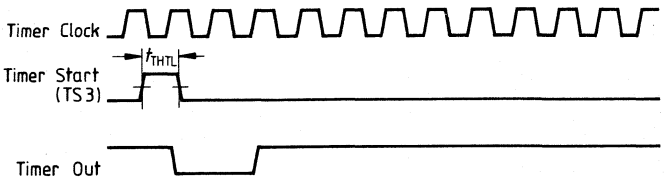
Pulse Diagrams

Oscillator

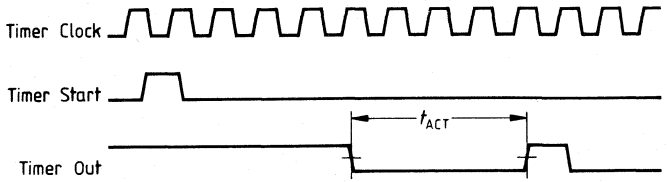


Timer

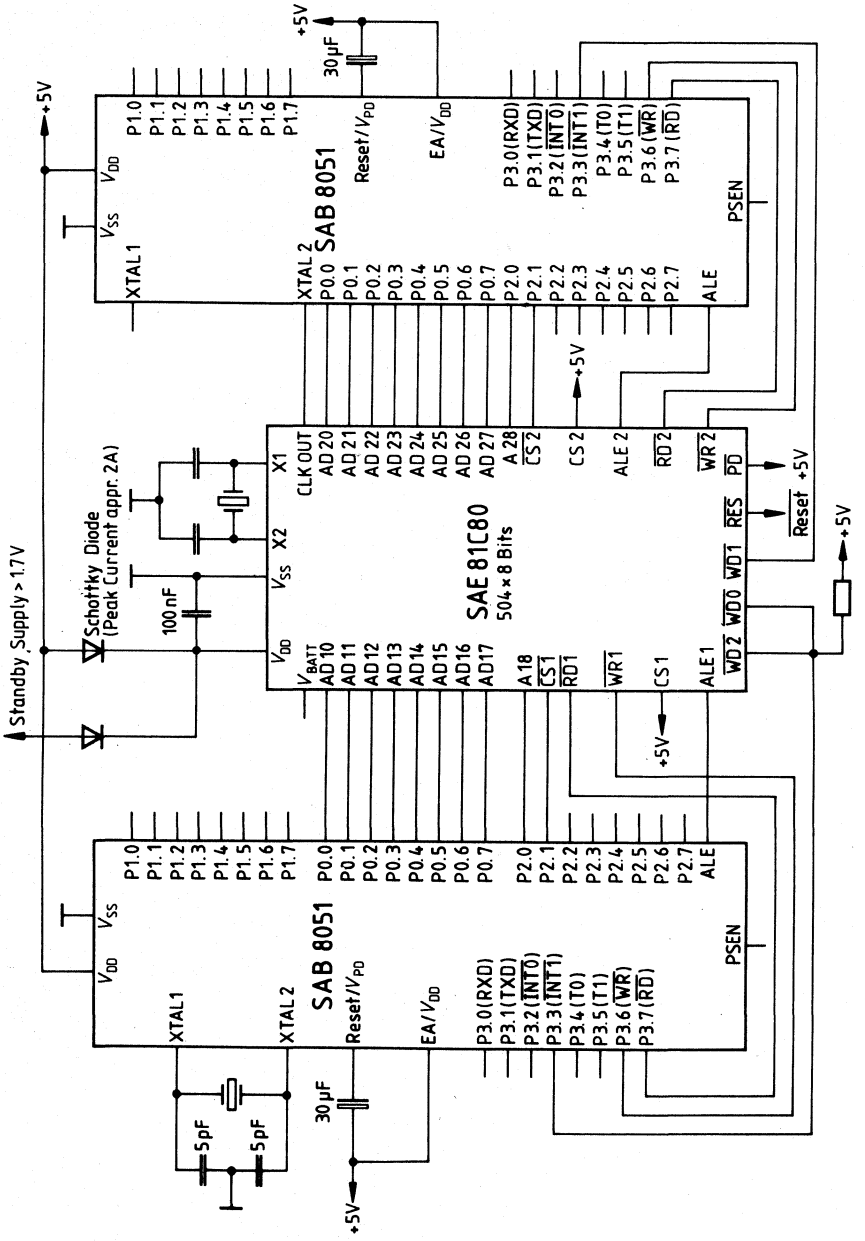
Single-Shot Operation Mode (TMR="80_H", High Byte=Medium Byte="00_H", Low Byte="02_H")



Auto-Reload Operation Mode (TMR="60_H", High Byte=Medium Byte="00_H", Low Byte="05_H")



Application Circuit



SAB 8051 – Program for Timer Operation in Watchdog Mode

```
HBYTE   EQU   1E3H    ;Address high byte reload register
TMR     EQU   1E0H    ;Address timer mode register
KR      EQU   1ECH    ;Address control register
REST1   EQU   055H    ;1st value to restart timer
REST2   EQU   0AAH    ;2nd value to restart timer
WDAUS   EQU   060H    ;Value to switch off watchdog mode

; Load reload register

MOV     DPTR, # HBYTE
CLR     A
MOVX    @ DPTR,A
DEC     DPL
MOV     A, # 0FFH
MOVX    @ DPTR,A
DEC     DPL
MOVX    @ DPTR,A

; Switch on watchdog mode and start timer

MOV     A, # 0AFH
DEC     DPL
MOVX    @ DPTR,A

; Reset timer

MOV     DPTR, # KR
MOV     A, # REST1
MOVX    @ DPTR,A
MOV     A, # REST2
MOVX    @ DPTR,A

; Switch off watchdog mode and stop timer

MOV     DPTR, # KR
MOV     A, # REST1
MOVX    @ DPTR,A
MOV     A, # WDAUS
MOV     DPTR, # TMR
MOVX    @ DPTR,A
MOV     A, # REST2
MOV     DPTR, # KR
MOVX    @ DPTR,A

;

END
```

Safety Counter, Nonvolatile Memories

Selector Guide

Type	Package	Features			Temperature range
SLE 4501	P-DIP-8 and MIKROPACK (SMD)[1]	Nonvolatile safety counter	64x8	22-bit counter	−40°C...+110°C
SLE 4502	P-DIP-8	Prescaler for safety counter	–	3-line bus	−40°C...+110°C
SDE 2506	P-DIP-8 and MIKROPACK (SMD)[1]	EEPROM	128x8	3-line bus	−40°C...+110°C
SDE 2516	P-DIP-8 and MIKROPACK (SMD)[1]	EEPROM	128x8	I²C bus	−40°C...+110°C
SDE 2526	P-DIP-8 and MIKROPACK (SMD)[1]	EEPROM	256x8	I²C bus	−40°C...+110°C

[1]) available upon request

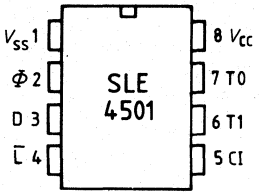
Preliminary Data **MOS IC**

Type	Ordering Code	Package
SLE 4501	Q67100-H8377	P-DIP-8
SLE 4501 K	in preparation	MIKROPACK (SMD)

Features

- Internal generation of programming voltage
- Counting range 22 binary bits, nonvolatile storage
- Count output in serial binary code
- Counting operation is executed under on-chip control and cannot be influenced externally
- Disconnection of the operating voltage, even during a counting operation, has no effect on the stored count
- Once the fusible link has been blown, the count is protected against manipulation by internal safety logic.
- Additional 64x8 bit EEPROM area with serial access (byte organization)
- Non-volatile reprogramming of EEPROM area and count through on-chip control onto defined viewport, thus reliable data storage is ensured.
- Extended temperature range from −40 °C to +110 °C

Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	V_{SS}	Ground
2	Φ	Clock input
3	D	Data input/output
4	$\overline{L}$	Chip select for data input (active high) and indication of storage operation (active low)
5	CI	Count pulse input (active high)
6	T1	Fusible link
7	T0	Control input test operation and fusible link
8	V_{CC}	Operating range

Circuit Description

The nonvolatile counter (NC) has a counting range of 22 binary bits and retains its count even after the operating voltage has been disconnected. The safety logic of the device prevents any alteration other than the intended incrementing of the count, which might be caused by supply voltage failures, e.g. during a counting operation. Before the fusible link blows, a desired count can be preset in a test operation. After the fusible link has blown, the count can only be altered by a count request. Thus it is only possible to increment the counter.

The count is binary coded and can be serially sampled via a three-wire bus (section 4). A counting operation has priority in any case and will terminate any readout operation that has been started.

The 64x8 bit EEPROM area (NVM) is addressed serially by a 1-byte OP code (see programming and readout operation). Addresses 16 through 63 can no longer be reprogrammed after the fusible link is blown. Before the fusible link blows, test input T0 should be set low for normal operation.

An on-chip reset circuit ensures operational reliability. Its functioning is described on page 870.

Counting Operation (figure 1c)

The integrated circuit consists of a 22-step, asynchronous counter and a nonvolatile, electrically reprogrammable memory (EEPROM) for nonvolatile storage of the counter contents.

For reasons of operational reliability, the counting operation is executed entirely under on-chip control. The device includes the necessary sequence control for which it generates an internal clock of approx. 50 kHz. A pulse at input CI causes the asynchronous counter to be incremented by 1.

The new count is stored as nonvolatile information. This storage operation is indicated by low at input/output $\overline{L}$. During storage no other count events are registered, resulting in a dead time of max. 100 ms in the rated-voltage range. The operating voltage must be maintained in the rated-voltage range for at least another 10 ms after the start of a storage operation, or else the last count event might not be permanently stored (response time). Counts that have already been stored are not at all affected if the operating voltage is switched off during a storage operation and thus cannot be manipulated. If the operating voltage is reduced during the counting operation, the dead time and the response time will increase, but storage reliability is not affected due to the integrated programming-duration control. The device is inactive outside the operating-voltage window defined by the reset circuit.

The nonvolatile safety counter includes overflow protection. If all counter bits are 1, any further count pulses are ignored.

Count Readout (figure 1 d)

For sampling the count, input/output $\overline{L}$ is first set low and then the two instruction bits B0, B1 are clocked in. Afterwards pin L is set high.again. With the trailing edge of any further clock pulse Φ the bits appear consecutively at pin D, starting with the most significant bit. The entire count is read out with 22 clock pulses. A low pulse at input/output L switches pin D back to high impedance.

A storage operation (nonvolatile counter or 64x8 bit EEPROM) indicated by a low level at pin $\overline{L}$ has always priority. During this time the device cannot be addressed. A count request will terminate any readout operation that has already been started.

Programming of NVM (figure 1 a)

The input/output $\overline{L}$ must be set low. Then the 8-bit data word (D0 as the 1st bit) is first clocked in, followed by the 8-bit instruction word (consisting of six address bits A0 through A5 and two instruction bits B0, B1). After pin $\overline{L}$ has been set high again, the programming operation, indicated by low at the input/output $\overline{L}$, begins subsequently to another clock pulse Φ. When the internally controlled storage operation has been completed, $\overline{L}$ returns to high. In the rated-voltage range the maximum programming time t_p is 10 ms.

Readout of NVM (figure 1 b)

The input/output $\overline{L}$ must be set low. Then the 8-bit instruction word (consisting of 6 address bits A0 through A5 and two instruction bits B0, B1) is clocked in. After pin $\overline{L}$ has been set high again, one bit (beginning with D0) of the respective data word appears at pin D with the trailing edge of any further clock pulse Φ. The entire data word is read out with eight clock pulses. A low pulse at input/output $\overline{L}$ switches pin D back to high impedance.

Fusible Link (figure 4)

Blowing of the fusible link has the following irreversible effects:

a) The count can now only be altered by count pulses at count input CI.
b) It is no longer possible to program the entire NVM in one operation.
c) Addresses 16 through 63 of the NVM can no longer be reprogrammed.

In order to blow the fusible link, the following conditions must prevail at the inputs (cf. **figure 4**):

a) Test input T0 to 17 V
b) Test input T1 to 17 V with max. 1 µs edge rise time.

The fusible link melts within 100 ms. At test input T0 there is a temporary peak current of up to 100 mA which can be taken from a storage capacitor, for instance.

For the blowing process, test input T0 must be connected according to **figure 4 b**, otherwise the device might be destroyed.

Test Operation (figure 2a, 2b, 2c)

Provided the fusible link has not blown the following test operations are possible (T1 must always be kept low and T0 high):

a) Presetting of count **(figure 2a)**

The input/output $\overline{L}$ is set low and then the 22 bits constituting the required count are clocked in, starting with the most significant bit. Here it should be noted that the counter bits CB0 through CB3 can only be programmed uniformly as 0 or 1. After the two bits of the instruction code have been clocked in, pin $\overline{L}$ is set high again.

Differing values for CB0 through CB3 will lead to undefined counts.

A high on count input CI starts the programming operation, which is indicated by a low at pin $\overline{L}$. In order to activate the safety logic for the preset count, T0 must then be set low and the supply voltage switched off briefly.

b) Erasure of entire NVM **(figure 2b)**
Writing into entire NVM **(figure 2c)**

Input/output $\overline{L}$ is set low and the two bits B0, B1 of the instruction code are clocked in. After switching pin $\overline{L}$ to high, a high at input Φ will start the programming operation which is indicated by a low at input/output $\overline{L}$. Input Φ must be kept high for at least 50 ms because the internal timing control for the NVM is switched off and the programming duration (t_{gpr}) is defined for the length of the Φ pulse.

Instruction Codes

a) T0 low or after blowing the fusible link:

Function	B0	B1
Program NVM	1	0
Read out NVM	1	1
Read out counter	0	1

b) T0 high (test operation):

Started by pulse at CI

Function	B0	B1
Preset counter	0	0

Started by clock pulse Φ

Function	B0	B1
Erase entire NVM Write into entire NVM	1	0

Reset Function

For reasons of operational reliability the device contains an internal reset circuit that limits the active range to that of a voltage window. The lower limit is at a maximum of 4.5 V and the upper limit at a minimum of 5.5 V.

If the supply voltage is outside the window, even if only because of spikes, the device will reset. As soon as the prescribed voltage window has been reached again, a reset routine runs automatically, this being indicated by a low at input/output $\overline{L}$ resulting in a dead time of max. 100 ms in the rated-voltage range.

Maximum Ratings

Description	Symbol	min	typ	max	Unit
Supply voltage Input voltage	V_{CC} V_I	−0.3 −0.3		6 6	V V
Power dissipation	P_D		40		mW
Storage temperature	T_{stg}	−55		125	°C
Thermal resistance system – air	$R_{th\ SA}$		100		K/W

Operating Range

Supply voltage	V_{CC}	4.75		5.25	V
Ambient temperature	T_A	−40		110	°C

Characteristics

Description	Symbol	min	typ	max	Unit
Supply voltage	V_{CC}	4.75		5.25	V
Supply current	I_{CC}		7	10	mA
Inputs[1])	V_I		0.5	0.8	V
(Φ, $\overline{L}$, CI, D, T1)	V_H	2.2		V_{CC}	V
(T0)	V_H	4.95		V_{CC}	V
(Φ, $\overline{L}$, CI, D, T1)	I_H			10	µA
(T0)	I_H			100	µA
Outputs (D, $\overline{L}$)	I_L	1			mA
(open drain, $V_I = 0.5$ V)	I_H			10	A
Counting dead time	t_{dead}			100	ms
Counting response time	t_{resp}			10	ms
Clock Φ	t_H	5		1000	µs
	t_L	5			µs
	t_f	1			µs
Interval start pulse/ trailing edge $\overline{L}$	t_{ST}	5			µs
Count input CI	t_{CI}	5			µs
Programming time NVM (per byte)	t_{pr}			10	ms
Programming time NVM (total memory)	t_{gpr}	50		100	ms
Blowing of fusible link:					
T0	V_H	16.7		17.3	V
	I_H			100	mA
T1	V_H	16.7		17.3	V
	I_H			10	µA
	t_f			1	µs
	t_s	100			ms

[1]) The following particular level conditions apply to the input Φ in case of test operating modes:

Φ (test operation)	V_L		0.5	0.6	V
	V_H	3.0		V_{CC}	V

Block Diagram

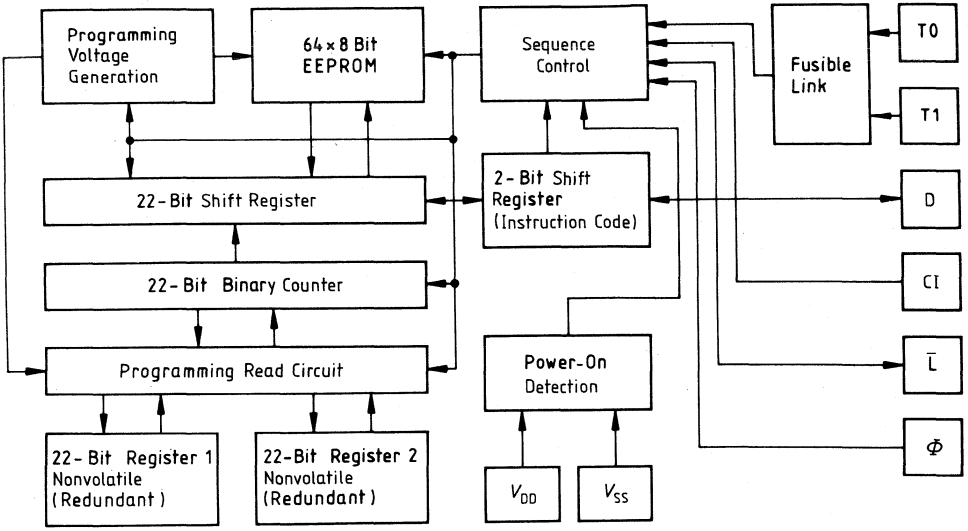


Figure 1a Programming of NVM

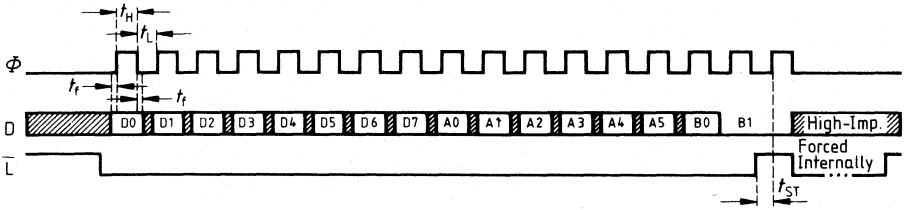


Figure 1b Readout of NVM

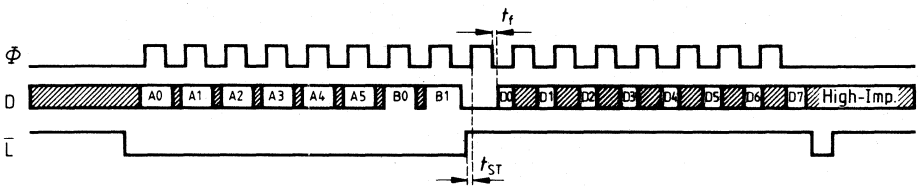


Figure 1c Counting Operation

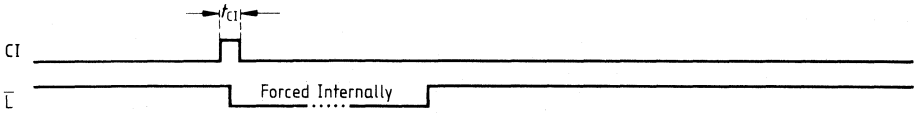


Figure 1d Reading Out Count

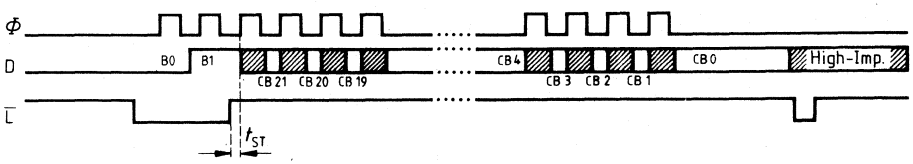


Figure 2a Presetting Count on NC

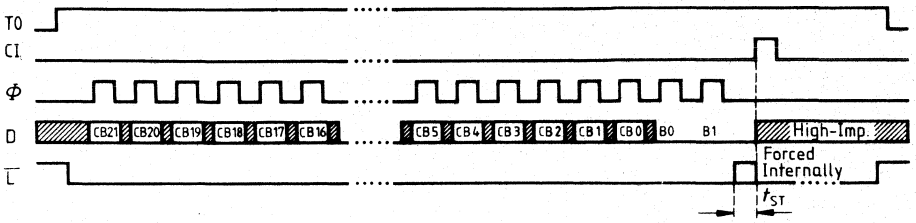


Figure 2b Erasure of Entire NVM

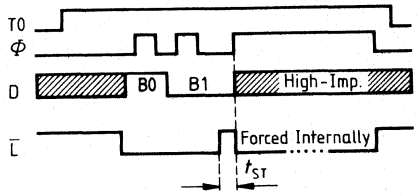


Figure 2c Writing into Entire NVM

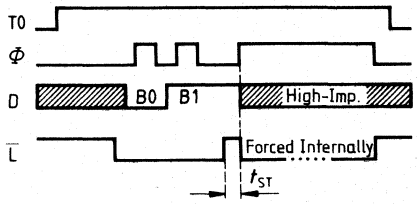


Figure 3
Application Circuit

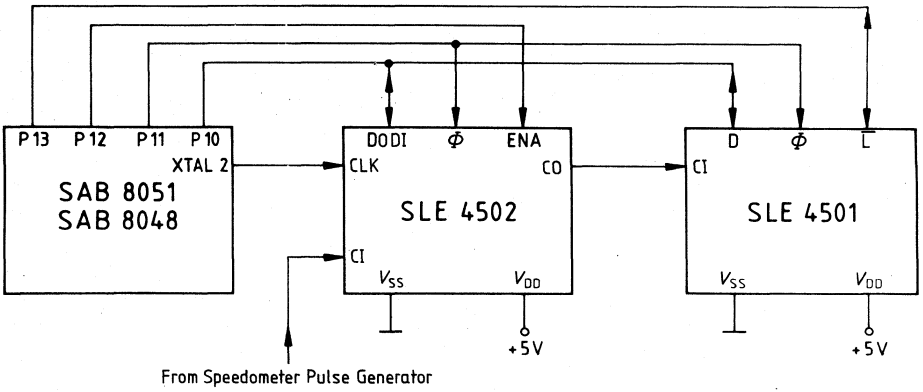
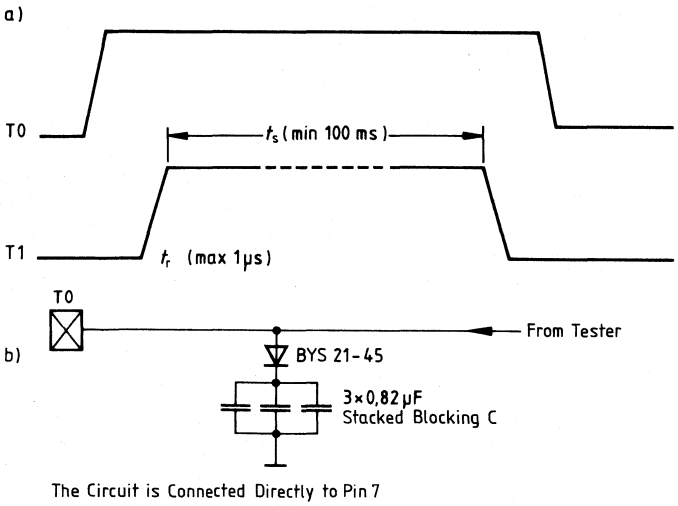


Figure 4
Blowing Fusible Link



Preliminary Data **CMOS IC**

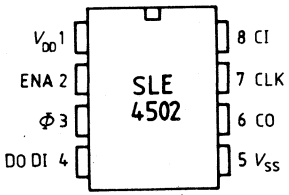
Type	Ordering Code	Package
SLE 4502	Q67100-H8378	P-DIP-8

The SLE 4502 integrated circuit transforms the speed pulses for the SLE 4501 nonvolatile safety counter.

Features

- CMOS technology
- Inputs/outputs protected against latch-up
- NMOS-compatible inputs and outputs
- Low standby current (1 µA)
- Schmitt trigger input for counter
- 4-bit miles counter with a programmable prescaler (between 1 and 6,5 536)
- 16-bit register for miles-counter function with external time base
- 16-bit register for trip counter resettable
- Serial three-wire bus
- Power-fail flag
- Extended temperature range from −40 to +110 °C

Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	V_{DD}	Supply voltage +5 V
2	ENA	Enable input
3	Φ	Clock input for data input/output
4	DO DI	Data output – data input
5	V_{SS}	Supply voltage 0 V
6	CO	Counter output
7	CLK	Clock input for IC timing
8	CI	Count pulse input

Circuit Description

1. Counter Function

The arriving count pulses are sent to the count output via a programmable 16-bit counter and a fixed 4-bit counter. At a 3-MHz clock frequency, the output pulse width is about 42 µs. The contents of the 4-bit counter is readable over the serial interface (first 4 bits).

2. Trip Counter

The output pulses of the programmable divider are counted in an additional 16-bit register. This counter is readable and resettable.

3. Speedometer

The clock frequency reaches a 16-bit interval counter, which is programmable in a 16-bit register, over a 5-bit prescaler. The speed pulses are counted during an interval and stored in a latch at the end of the interval. This latch may be read at any time.

4. Power-Fail Flag

Upon an increase in the supply voltage from 0V to 5V a reset is generated. The power-fail flag indicates this condition. The power-fail flag is reset when it is read out (first bit).

5. Instruction Code

Function	B3	B2	B1	B0
Program divider factor of miles counter	1	1	0	0
Program divider factor of speedometer	1	0	1	0
Reset trip counter	1	0	0	1
Read out miles counter	0	1	0	0
Read out trip counter	0	0	0	1
Read out speedometer	0	0	1	0
Read out power-fail flag	0	1	1	1

Maximum Ratings

Description	Symbol	min	typ	max	Unit
Supply voltage	V_{DD}	−0.3		6	V
Input voltage	V_{IM1}	−0.3		V_{DD} +0.3	V
Power dissipation per output	P_Q			50	mW
Total power dissipation	P_{tot}			150	mW
Storage temperature	T_{stg}	−50		125	°C

Operating Range

Supply voltage	V_{DD}	4.5	5	5.5	V
DC supply current	I_{DDS}			1	µA
Supply current (see measurement circuit)	I_{DD}			1	mA
Operating frequency	f_{CLK}	1		3	MHz
Ambient temperature	T_A	−40		+110	°C

Characteristics

$T_A = 25\,°C$

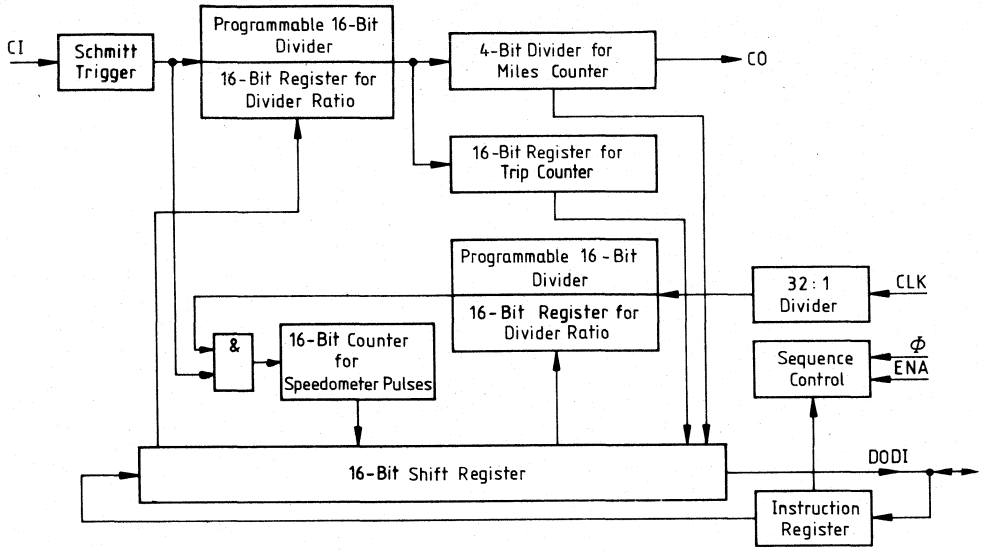
Description	Symbol	min	max	Unit
All input signals except CI				
H input voltage	V_{IH}	2.2	V_{DD}	V
L input voltage	V_{IL}	0	0.8	V
Input capacitance	C_I		10	pF
L input current	I_{IL}		1	µA
H input current	I_{IH}		1	µA
Input signal CI				
H input voltage	V_{IH}	$V_{DD}-1$	V_{DD}	V
L input voltage	V_{IL}	0	1	V
Input cpacitance	C_I		10	pF
L input current	I_{IH}		1	µA
H input current	I_{IH}		1	µA
Hysteresis	V_{Hy}	1	1.5	V
Output signals				
H output voltage $I_Q = 0.5$ mA	V_{QH}	$V_{DD}-0.4$		V
L output voltage $I_Q = 1.6$ mA	V_{QL}		0.4	V

AC Characteristics

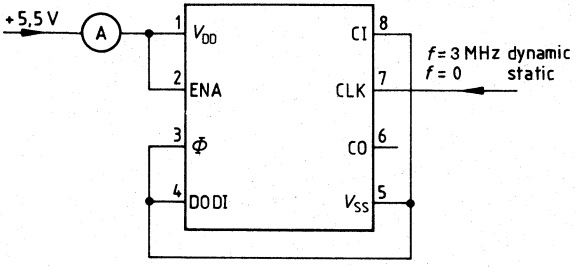
$T_A = 25\,°C$

Clock frequency	f_{CLK}	1	3	MHz
Pulse duration CLK	t_{CLKH}	150	600	ns
Pulse spacing CLK	t_{CLKL}	150	600	ns
Pulse duration Φ	$t_{\Phi H}$	500		ns
Pulse spacing Φ	$t_{\Phi L}$	500		ns
Enable low to Φ	$t_{E\Phi}$	$6/f_{CLK}$		
Φ low to enable	$t_{\Phi E}$	100		ns
Data setup	t_S	100		ns
Data hold	t_H	100		ns
Output delay	t_D		150	ns
Enable low to data high-impedance	t_{HC}		$6/f_{CLK}$	
Output pulse width CO	t_{CO}	$120/f_{CLK}$	$136/f_{CLK}$	
Pulse duration CI	t_{CH}	$3/f_{CLK}$		
Pulse spacing CI	t_{CL}	$3/f_{CLK}$		
Clock frequency at CI	f_{CI}		$f_{CLK}/6$	

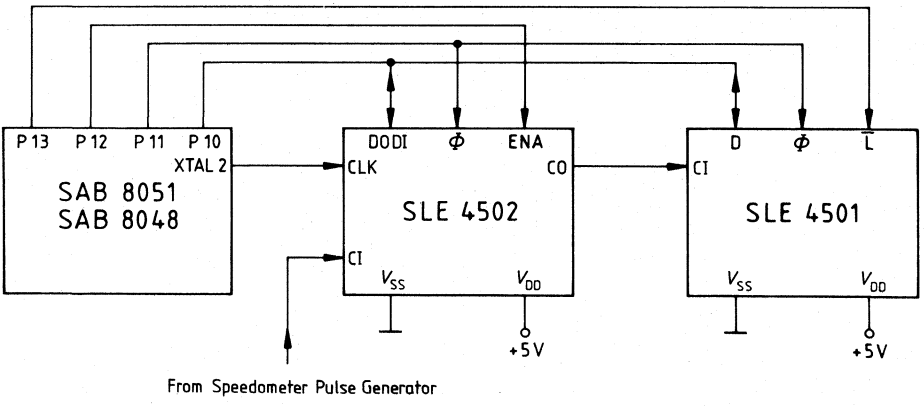
Block Diagram



Measurement Circuit

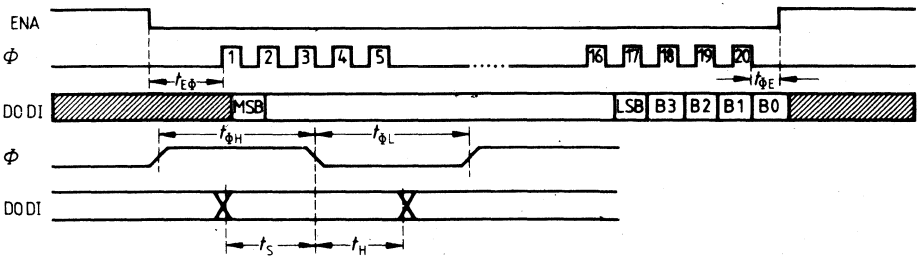


Application Circuit

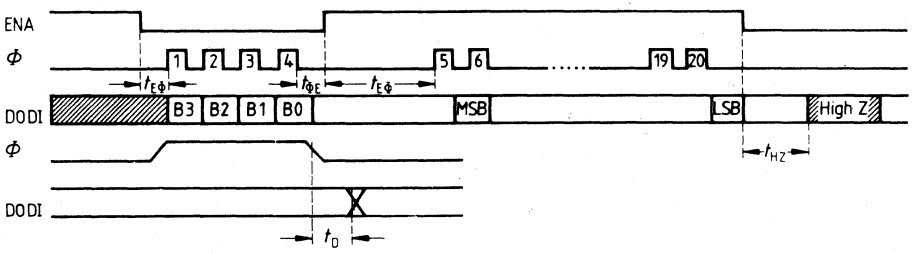


Diagrams

Write



Read



Preliminary Data **MOS IC**

Type	Ordering Code	Package
SDE 2506	Q67100-H8441	P-DIP-8
SDE 2506 K	Q67100-H8473	MIKROPACK (SMD)

Features

- Word-organized reprogrammable nonvolatile memory in n-channel floating-gate technology
- 128 x 8-bit organization
- 5 V supply voltage
- 3 lines between control processor and E²PROM for data transfer and chip control
- Data input (8 bits), address input (7 bits), control information input (1 bit) and data output are serial
- More than 10^5 reprogramming cycles per address
- Data retention longer than 10 years (operating temperature range)
- Unlimited number of read-out operations without refresh
- 5 ms erase/write cycle
- Extended temperature range from −40 °C to +110 °C

Note

Throughout the temperature range between −40 °C and 0 °C the MIKROPACK version can only be read out, not programmed.

Circuit Description

Data Transfer and Chip Control

Three lines having several functions each are required for the data transfer between control processor and E²PROM memory.

a) Data line D
   - bidirectional serial data transfer
   - serial address input
   - clocked input of a control information
   - direct control input

b) Clock line Φ
   - data input, address input and control bit input
   - data output
   - start read-out with takeover of data from memory in shift register or start data-change during reprogramming

c) Chip activation line $\overline{CE}$
   - chip reset and data input (active high)
   - chip activation (active low)

Prior to activating the chip, the data, address and control information is clocked in via the bidirectional data bus. These data are maintained in the shift register during reprogramming and read-out up to the second clock pulse. The following data formats have to be input:

a) Memory read-out: one 8-bit control word, consisting of
   - 7 address bits A0 to A6 (at first A0 being LSB)
   - 1 control bit, SB = "0", after A6

b) Memory reprogramming (erasure and/or writing) 16-bit input information, consisting of
   - 8 bits D0 to D7 new memory information (at first D0 being LSB)
   - 7 bits A0 to A6 address information (at first A0 being LSB after D7)
   - 1 bit control information, SB = "1", after A6

Memory read-out (see page 893)

After data input and with SB = "0" the read-out operation of the selected word address is started by the transition of $\overline{CE}$ from "1" to "0". The information being on the data line during chip activation is of no influence.

With the first clock pulse after $\overline{CE}$ = "0" the data word is taken over from the selected memory address into the shift register. After termination of the first Φ pulse the data output is in the low impedance state. With every following clock pulse another data bit is pushed to the output. Through the transition of $\overline{CE}$ from "0" to "1" the data line returns to the high impedance state.

Reprogramming (see page 894)

In general, a full reprogramming operation consists of an erasure operation and a subsequent writing operation. During erase all bits of the selected word are set into the uniform "1" state, during writing "0" states are produced according to the information in the shift register.

A reprogramming operation is started when after data input and due to chip activation an information SB = "1" is in the relevant cell. Whether an erase or a writing operation is then taking place depends on the information that is on data line D during chip activation.

For erasure into state "1" a "1" must be present at the data input during transition of $\overline{CE}$ to low. If, however, a writing process is to be started in state "0", a "0" has to be present at the data line during chip activation.

Afterwards, a start pulse at the clock input Φ is required for the programming start. The control information has to remain stable at D until the leading edge of the start pulse is reached. The active data change starts with the trailing edge of this start pulse. The programming process is terminated by suppression of the chip activation, i.e. by $\overline{CE}$.

The reprogramming of a word initiates with start and sequence of an erase procedure. $\overline{CE}$ being "1" stops the erasure. The control bit SB = "1" (in the shift register) which is also necessary for the write process remains stable even after the termination of the erasure. Thus, for writing the selected word, only the data line D has to be changed over from "1" to "0", the chip has to be activated again by $\overline{CE}$ = "0" and the data change has to be started by the start pulse.

An erase and a write process can also be executed separately. In order to obtain a safe "1" in all 8 bits of the selected memory address by the erase process, a data word is, however, to be entered with 8 times "1" before erasure. During the writing of a word which has not been erased before, the "0" states of the previous and the actual information are added.

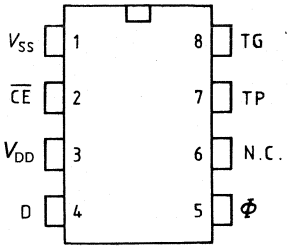
Test Mode – Total Erasure

The test mode is activated, if the input TP (pin 7) is set from 0 V to 5 V = V_{DD}. To erase the entire memory the test mode is to be turned on and the address 0 (A0 to A6) together with the control bit SB = 1 is to be entered. The subsequent programm sequence is identical to the erasure of address 0. As soon as the erase procedure has terminated due to $\overline{CE}$ changing over from 0 to 1, the test mode is to be turned off.

RESET

A memory which has not been selected is automatically in reset state by state $\overline{CE}$ = "1". All flipflops of the sequence control are reset. However, the information in the shift register is maintained and will only be changed by shifting the data. The reset state is also set in the case of the turning-on of the memory (power-on) by an on-chip circuit.

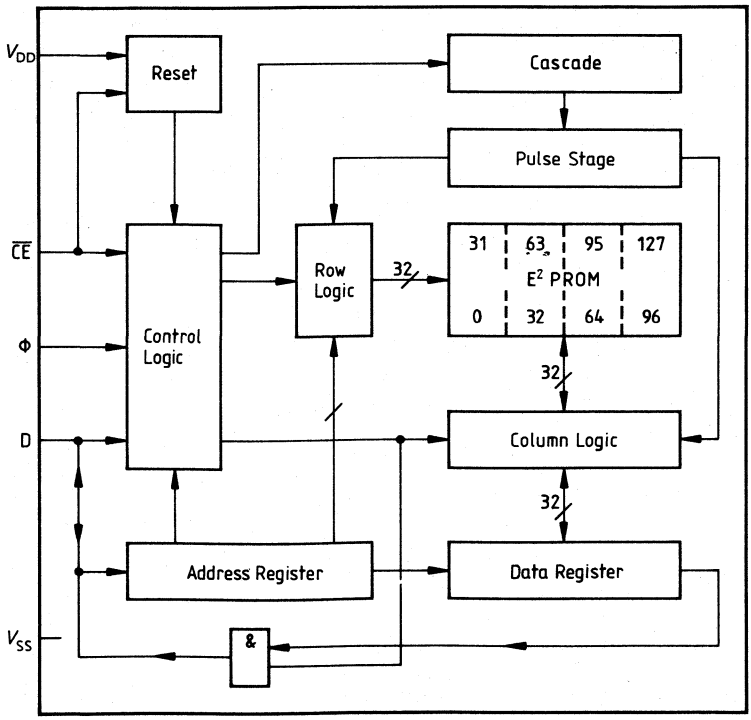
Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	V_{SS}	Ground
2	$\overline{CE}$	$\overline{CE} = 1$ for data input/output $\overline{CE} = 0$ for reprogramming
3	V_{DD}	+5 V supply voltage
4	D	Data input/output bidirectional data line For reprogramming D = 1 erase D = 0 write
5	Φ	Clock
6	N.C.	Not connected
7	TP	Test input, at V_{SS}
8	TG	Test input, remains open

Block Diagram



Maximum Ratings

Description	Symbol	min	max	Unit
Supply voltage Input voltage	V_{DD} V_I	−0.3 −0.3	6 6	V V
Power dissipation	P_D		40	mW
Storage temperature Junction temperature	T_{stg} T_j	−55	125 125	°C °C
Thermal resistance system – air	$R_{th\ SA}$		100	K/W

Operating Range

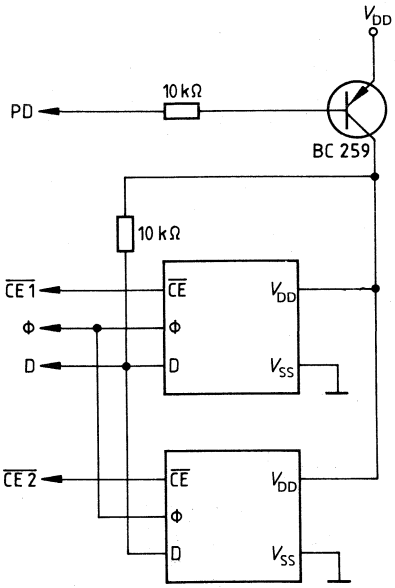
Supply voltage Ambient temperature	V_{DD} T_A	4.75 −40	5.25 110	V °C

Characteristics

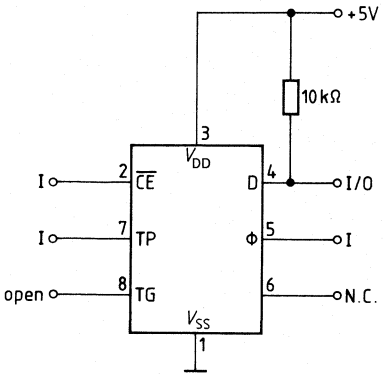
$T_A = 25\,°C$

Description	Symbol	Measuring conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.75	5	5.25	V
Supply current	I_{CC}	($V_{DD} = 5.25$ V)			3	mA
Inputs						
Input voltage (D, Φ, $\overline{CE}$)	V_L				0.8	V
Input voltage (D, Φ, $\overline{CE}$)	V_H		2.4			V
Input current (D, Φ, $\overline{CE}$)	I_H	($V_H = 5.25$)			10	µA
Data output D (open drain)						
L output current	I_L	($V_L = 0.8$ V)			0.5	mA
H output current	I_H	($V_H = 5.25$ V)			10	µA
Clock pulse Φ						
Clock High period	t_H		2.5		60	µs
Clock Low period	t_L		5			µs
Edge spacing $\overline{CE}$ to D	Δt		2.5			µs
Edge spacing $\overline{CE}$ to Φ	t_{AKT}		5			µs
Data hold time (before/after Φ trailing edge	t_{HD}		2.5			µs
Data delay time (after Φ trailing edge)	t_{DD}		2.5			µs
Rise time	t_r				1	µs
Fall time	t_f				1	µs
Chip erase duration	t_{er}		5		20	ms
Write duration	t_{wr}		5		20	ms
Full erasure duration	$t_{tot\,er}$		20		25	ms

Application Circuit

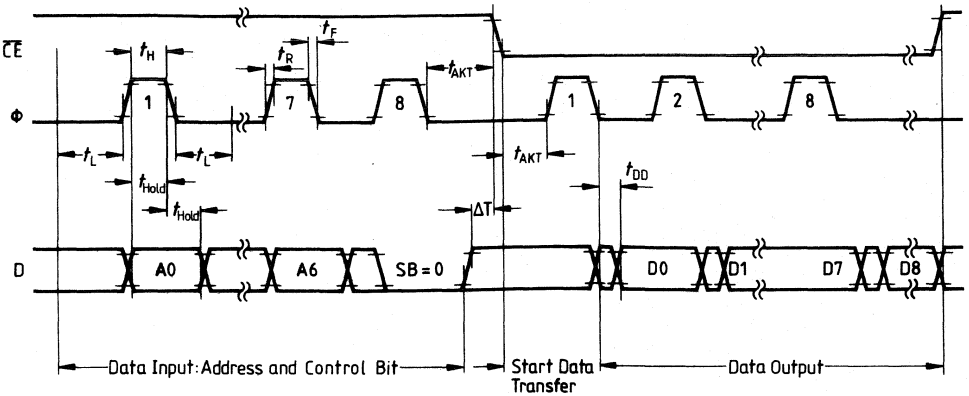


Measurement Circuit



Diagrams

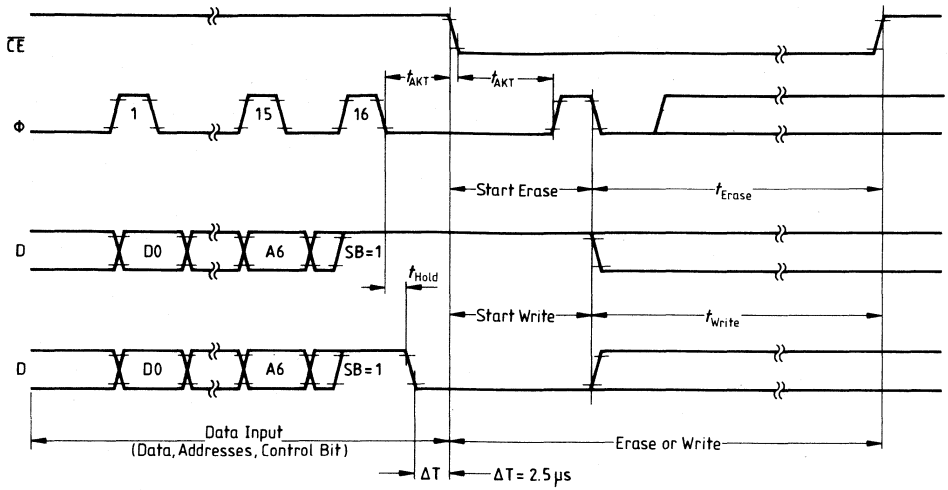
Read

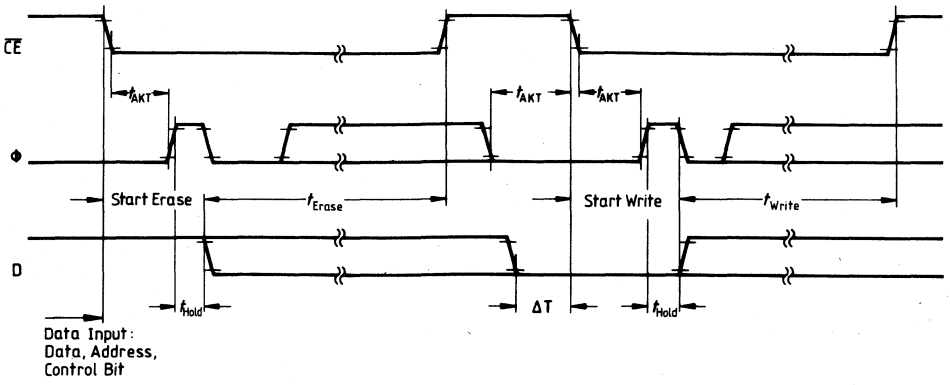


t_{AKT} = 5 µs; t_R = t_F = 1 µs
t_{Hold} = 2.5 µs; t_L = 5 µs
t_{DD} = 2.5 µs; t_H = 2.5 µs
ΔT = 2.5 µs

Diagram

Reprogramming





Nonvolatile Memory
1-KBit E²PROM with I²C Bus Interface

SDE 2516

Preliminary Data

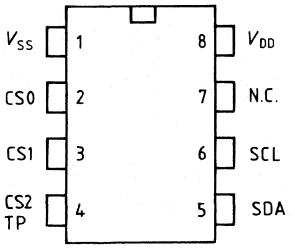
MOS IC

Type	Ordering Code	Package
SDE 2516	Q67100-H8442	P-DIP-8

Features

- Word-organized reprogrammable nonvolatile memory in n-channel floating-gate technology (E²PROM)
- 128 x 8-bit organization
- +5 V supply voltage
- Serial 2-line bus for data input and output (I²C bus)
- Reprogramming mode, typ. 15 ms erase/write cycle
- Reprogramming by means of on-chip control (without external control)
- Data retention longer than 10 years
- More than 10^5 reprogramming cycles per address
- Extended temperature range from −40 °C to +110 °C

Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	V_{SS}	Ground
2	CS0	Chip select input
3	CS1	Chip select input
4	CS2/TP	Test operation control
5	SDA	Data line
6	SCL	Clock line I^2C bus
7	N.C.	Not connected
8	V_{DD}	Supply voltage

Control Word Input Key

CS/E CS/A	Chip select for data input to memory Chip select for data output from memory
WA	Memory word address
DE DA	Data word for memory Data word read out from memory
D0 to D7	Data bits
ST	Start condition
SP	Stop condition
As	Acknowledge bit from memory
Am	Acknowledge bit from master
CS0, CS1, CS2	Chip select bits
A0 to A6	Memory word address bits

Maximum Ratings[1])

Description	Symbol	Ratings	Unit
Supply voltage range Input voltage range	V_{DD} V_I	−0.3 to 6 −0.3 to 6	V V
Power dissipation	P_D	50	mW
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air	$R_{th\ SA}$	100	K/W

Operating Range

Supply voltage	V_{DD}	4.75 to 5.25	V
Ambient temperature	T_A	−40 to 110	°C

[1]) does not apply to the input CS2/TP in "test mode/full erase" operation

DC Characteristics

Description	Symbol	min	typ	max	Unit
Supply voltage	V_{DD}	4.75		5.25	V
Supply current	I_{DD}			8	mA
Inputs SCL/SDA					
Low level	V_{IL}			1.5	V
High level	V_{IH}	3.0		V_{DD}	V
High current $V_{IH} = V_{DD\ max}$	I_H			10	µA
Output SDA					
Low current $V_{QL} = 0.4$ V	I_{QL}			3.0	mA
Leakage current $V_{QL} = V_{DD\ max}$	I_{QH}			10	µA
Inputs CSO, CS1, CS2/TP					
Low level	V_{IL}			0.2	V
High level	V_{IH}	4.5		V_{DD}	V
High current	I_{IH}			100	µA
Clock frequency	f_{SCL}			100	kHz
Reprogramming duration (erase and write)	t_{prog}		15	30	ms
Input capacitance	C_I			10	pF
Full erase duration (Test mode full erase)	t_{er}			50	ms
Condition	$V_{CS2/TP}$	11	12	13	V

I²C Bus Interface (Figure 1 and 2)

The I²C bus is a bidirectional 2-line bus for the transfer of data between various integrated circuits. It consists of a serial data line SDA and a serial clock line SCL. Both lines require an external pull-up resistor to V_{DD} (open drain output stages).

The possible operational states of the I²C bus are shown in **figure 1.** In the quiescent state, both lines SDA and SCL are high, i.e. the output stages are disabled. As long as SCL remains "1", information changes on the data bus indicate the start or the end of a data transfer between two components. The transition on SDA from "1" to "0" is a start condition, the transition from "0" to "1" a stop condition. During a data transfer the information on the data bus will only change when the clock line SCL is "0". The information on SDA is valid as long as SCL is "1".

In conjunction with an I²C bus system, the device can operate as a receiver and as a transmitter (slave receiver/listener, or slave transmitter/talker). Between a start and a stop condition, information is always transmitted in byte-organized form (8 bits). Between the trailing edge of the 8th transmission pulse and a 9th acknowledge clock pulse, the device sets the SDA line to low as a reception confirmation, if the chip select conditions have been met. During the output of data, the data output becomes high in impedance if the master receiver leaves the SDA line high during the acknowledge clock pulse.

The signal timing required for the operation of the I²C bus is summarized in **figure 2** (high-speed-mode).

Control Functions of the I²C Bus

The device is controlled by the controller (master) via the I²C bus in two operating modes: read cycle, and reprogramming cycle, including erase and write to a memory address. In both operating modes, the controller, as transmitter, has to provide 3 bytes to the bus after the start condition. Each byte has to be followed by an acknowledge bit. A rapid read mode enables the reading of data immediately after the slave address has been input. During a memory read, at least eight additional clock pulses are required to accept the data from the memory, before the stop condition may follow. In the programming case, the active programming process is only started by the stop condition after data input.

With a 3-bit chip select word (CS0, CS1, CS2) it is possible for the user to individually address 8 memories connected in parallel. Chip select is achieved when the three control bits logically correspond to the selected conditions at the three select inputs CS0, CS1, CS2.

Memory Read

After the input of the first two control words and 18 SCL pulses, a resetting of the start condition and the input of a third control word, the memory is set ready to read. During acknowledge clock no. 9, the memory information is transferred in parallel to the internal data register. Subsequent to the trailing edge of the acknowledge clock, the data output is low-impedance and the first data bit can be sampled. With each shift clock, an additional bit reaches the output. After reading a byte, the internal address counter is automatically incremented through the master receiver acknowledge, so that any number of memory locations can be read one after the other. At address 127, an overflow to address 0 is initiated. With the stop condition, the data output returns to high-impedance mode. The internal sequence control of the memory component is reset from the read to the quiescent state with the stop condition.

Memory Reprogramming

The reprogramming cycle of a memory word comprises an erase and a subsequent write process. During erase, all eight bits of the selected word are set into "1" state. During the write process, "0" states are generated according to the information in the internal data register, i.e. according to the third input control word.

After the 27th and last clock of the control word input, the active programming process is started by the stop condition. The active reprogramming process is executed under on-chip control and can be terminated by addressing the device via SCL and SDA.

The time required for reprogramming depends on component deviation and data patterns. Therefore, with rated supply voltage the erase/write process is max. 30 ms, or typically, 15 ms. For the input of a data word without write request (write request is defined as data bit in the data register set to "0"), the write process is suppressed and the programming time is shortened. During a subsequent programming of an already erased memory address, the erase process is suppressed again, so that the reprogramming time is also shortened.

Switch-on Mode and Chip Reset

After the supply voltage V_{DD} has been connected, the data output will be in the high-impedance mode. As a rule, the first operating mode to be entered should be the read process of a word address. Subsequent to the data output and the stop condition, the internal control logic is reset. In case of a subsequent active programming operation, however, the stop condition will not reset the control logic.

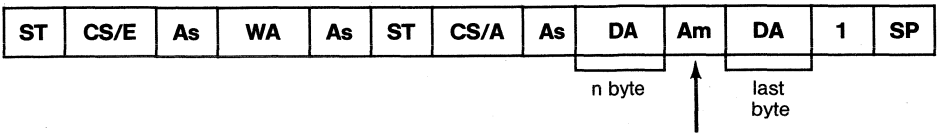
Test Mode – Chip Erase

The address register is loaded with address 0, the data register with FF (hex) by entering the control word "programming". Input CS2/TP, however, is connected from 0 V to +12 V immediately before the stop condition is generated. The subsequent stop condition initiates the chip erase procedure.

The control word has to be entered under the device address 0 (CS0 = L, CS1 = L, CS2 = L). After the full erase has been terminated, input CS2/TP must again be connected to 0 V.

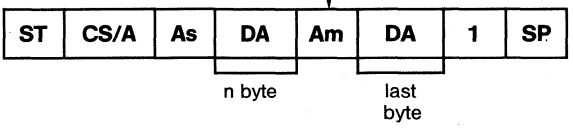
Control Word Input Read

a) complete (with word address input)

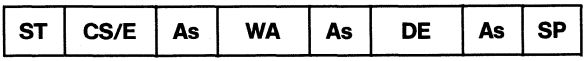


Automatic incrementation of the word address

b) shortened (read out starts with last used word address)



Control Word Input Programming



(Reprogramming starts after this stop condition)

Control Word Table

Clock No.	1	2	3	4	5	6	7	8	9	(Acknowledge)
CS/E	1	0	1	0	CS2	CS1	CS0	0	0	through memory
CS/A	1	0	1	0	CS2	CS1	CS0	1	0	through memory
WA	X	A6	A5	A4	A3	A2	A1	A0	0	through memory
DE	D7	D6	D5	D4	D3	D2	D1	D0	0	through memory
DA	D7	D6	D5	D4	D3	D2	D1	D0	0	through master

Diagrams

Operational states of the I²C bus

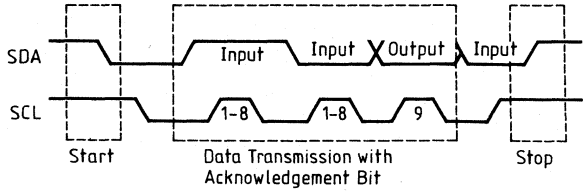


Figure 1

Timing conditions for the I²C bus (high-speed mode)

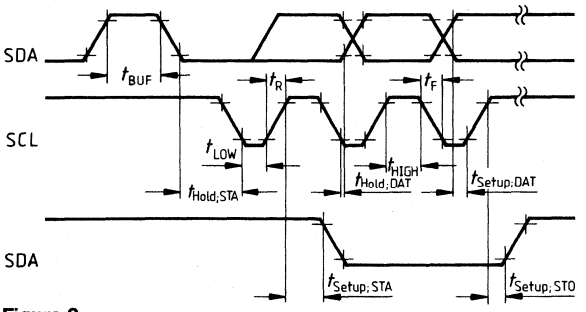


Figure 2

t_{BUF}	$t > t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{Hold;\ STA}$	$t > t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 µs	Clock LOW period
$t_{HIGHmin}$	4 µs	Clock HIGH period
$t_{Setup;\ STA}$	$t > t_{LOWmin}$	Start condition setup time, only valid for repeated start code
$t_{Hold,\ DAT}$	$t > 0$ µs	Data hold time
$t_{Setup;\ DAT}$	$t > 250$ ns	Data setup time
t_r	$t < 1$ µs	Rise time of both the SDA and SCL line
t_f	$t < 300$ ns	Fall time of both the SDA and SCL line
$t_{Setup;\ STO}$	$t > t_{LOWmin}$	Stop condition setup time

Note

All values refer to V_{IH} and V_{IL} level

Nonvolatile Memory
2-KBit E²PROM with I²C Bus Interface

SDE 2526

Preliminary Data

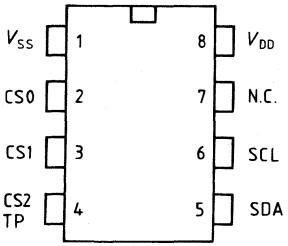
MOS IC

Type	Ordering Code	Package
SDE 2526	Q67100–H8443	P-DIP-8

Features

- Word-organized reprogrammable nonvolatile memory in n-channel floating-gate technology (E²PROM)
- 256 x 8-bit organization
- +5 V supply voltage
- Serial 2-line bus for data input and output (I²C bus)
- Reprogramming mode, typ. 15 ms erase/write cycle
- Reprogramming by means of on-chip control (without external control)
- Data retention longer than 10 years
- More than 10^5 reprogramming cycles per address
- Extended temperature range from −40 °C to +110 °C

Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	V_{SS}	Ground
2 3 4	CS0 CS1 CS2/TP	Chip select input Chip select input Test operation control
5 6	SDA SCL	Data line Clock line } I^2C bus
7	N.C.	Not connected
8	V_{DD}	Supply voltage

Control Word Input Key

CS/E CS/A	Chip select for data input to memory Chip select for data output from memory
WA	Memory word address
DE DA	Data word for memory Data word read out from memory
D0 to D7	Data bits
ST	Start condition
SP	Stop condition
As	Acknowledge bit from memory
Am	Acknowledge bit from master
CS0, CS1, CS2	Chip select bits
A0 to A7	Memory word address bits

Maximum ratings[1])

Description	Symbol	Ratings	Unit
Supply voltage Input voltage	V_{DD} V_I	−0.3 to 6 −0.3 to 6	V V
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance system – air	$R_{th\ SA}$	100	K/W

Operating Range

Supply voltage	V_{DD}	4.75 to 5.25	V
Ambient temperature	T_A	−40 to 110	°C

DC Characteristics

Description	Symbol	min	typ	max	Unit
Supply voltage Supply current	V_{DD} I_{DD}	4.75		5.25 10	V mA
Inputs SCL/SDA					
Low level High level High current $V_{IH} = V_{DD\ max}$	V_{IL} V_{IH} I_H	 3.0		1.5 V_{DD} 10	V V µA
Output SDA					
Low current $V_{QL} = 0.4$ V	I_{QL}			3.0	mA
Leakage current $V_{QL} = V_{DD\ max}$	I_{QH}			10	µA
Inputs CSO, CS1, CS2/TP					
Low level High level High current	V_{IL} V_{IH} I_{IH}	 4.5		0.2 V_{DD} 100	V V µA
Clock frequency	f_{SCL}			100	kHz
Reprogramming duration (erase and write)	t_{prog}		15	30	ms
Input capacitance	C_I			10	pF
Full erase duration (test mode full erase)	t_{er}			50	ms
Condition	$V_{CS2/TP}$	11	12	13	V

[1]) does not apply to the input CS2/TP in "test mode – full erasure" operation

I²C Bus Interface (Figure 1 and 2)

The I²C bus is a bidirectional 2-line bus for the transfer of data between various integrated circuits. It consists of a serial data line SDA and a serial clock line SCL. Both lines require an external pull-up resistor to V_{DD} (open drain output stages).

The possible operational states of the I²C bus are shown in **figure 1**. In the quiescent state, both lines SDA and SCL are high, i.e. the output stages are disabled. As long as SCL remains "1", information changes on the data bus indicate the start or the end of a data transfer between two components. The transition on SDA from "1" to "0" is a start condition, the transition from "0" to "1" a stop condition. During a data transfer the information on the data bus will only change when the clock line SCL is "0". The information on SDA is valid as long as SCL is "1".

In conjunction with an I²C bus system, the device can operate as a receiver, and as a transmitter (slave receiver/listener, or slave transmitter/talker). Between a start and a stop condition, information is always transmitted in byte-organized form (8 bits). Between the trailing edge of the 8th transmission pulse and a 9th acknowledge clock pulse, the device sets the SDA line to low as a reception confirmation, if the chip select conditions have been met. During the output of data, the data output becomes high in impedance if the master receiver leaves the SDA line high during the acknowledge clock pulse.

The signal timing required for the operation of the I²C bus is summarized in **figure 2** (high-speed mode).

Control Functions of the I²C Bus

The device is controlled by the controller (master) via the I²C bus in two operating modes: read cycle, and reprogramming cycle, including erase and write to a memory address. In both operating modes, the controller, as transmitter, has to provide 3 bytes to the bus after the start condition. Each byte has to be followed by an acknowledge bit. A rapid read mode enables the reading of data immediately after the slave address has been input. During a memory read, at least eight additional clock pulses are required to accept the data from the memory, before the stop condition may follow. In the programming case, the active programming process is only started by the stop condition after data input.

With a 3-bit chip select word (CS0, CS1, CS2) it is possible for the user to individually address 8 memories connected in parallel. Chip select is achieved when the three control bits logically correspond to the selected conditions at the three selct inputs CS0, CS1, CS2.

Memory Read

After the input of the first two control words and 18 SCL pulses, a resetting of the start condition and the input of a third control word, the memory is set ready to read. During acknowledge clock no. 9, the memory information is transferred in parallel to the internal data register. Subsequent to the trailing edge of the acknowledge clock, the data output is low-impedance and the first data bit can be sampled. With each shift clock, an additional bit reaches the output. After reading a byte, the internal address counter is automatically incremented through the master receiver acknowledge, so that any number of memory locations can be read one after the other. At address 255, an overflow to address 0 is initiated. With the stop condition, the data output returns to high-impedance mode. The internal sequence control of the memory component is reset from the read to the quiescent state with the stop condition.

Memory Reprogramming

The reprogramming cycle of a memory word comprises an erase and a subsequent write process. During erase, all eight bits of the selected word are set into "1" state. During the write process, "0" states are generated according to the information in the internal data register, i.e. according to the third input control word.

After the 27th and last clock of the control word input, the active programming process is started by the stop condition. The active reprogramming process is executed under on-chip control and can be terminated by addressing the device via SCL and SDA.

The time required for reprogramming depends on component deviation and data patterns. Therefore, with rated supply voltage the erase/write process is max. 30 ms, or typically, 15 ms. For the input of a data word without write request (write request is defined as data bit in the data register set to "0"), the write process is suppressed and the programming time is shortened. During a subsequent programming of an already erased memory address, the erase process is suppressed again, so that the reprogramming time is also shortened.

Switch-on Mode and Chip Reset

After the supply voltage V_{DD} has been connected, the data output will be in the high-impedance mode. As a rule, the first operating mode to be entered should be the read process of a word address. Subsequent to the data output and the stop condition, the internal control logic is reset. In case of a subsequent active programming operation, however, the stop condition will not reset the control logic.

Test Mode – Chip Erase

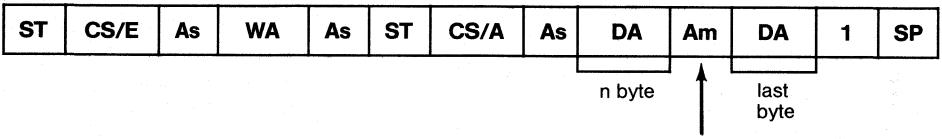
The address register is loaded with address 0, the data register with FF (hex) by entering the control word "programming". Input CS2/TP, however, is connected from 0 V to +12 V immediately before the stop condition is generated. The subsequent stop condition initiates the chip erase procedure.

The control word has to be entered under the device address 0 (CS0 = L, CS1 = L, CS2 = L).

After the full erase has been terminated, input CS2/TP must again be connected to 0 V.

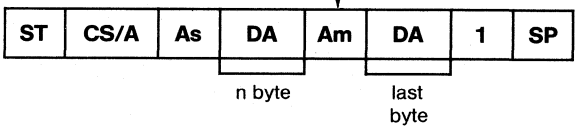
Control Word Input Read

a) complete (with word address input)

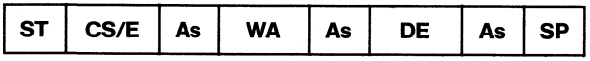


Automatic incrementation of the word address

b) shortened (read out starts with last used word address)



Control Word Input Programming



(Reprogramming starts after this stop condition)

Control Word Table

Clock N	1	2	3	4	5	6	7	8	9	(Acknowledge)
CS/E	1	0	1	0	CS2	CS1	CS0	0	0	through memory
CS/A	1	0	1	0	CS2	CS1	CS0	1	0	through memory
WA	A7	A6	A5	A4	A3	A2	A1	A0	0	through memory
DE	D7	D6	D5	D4	D3	D2	D1	D0	0	through memory
DA	D7	D6	D5	D4	D3	D2	D1	D0	0	through master

Diagrams

Operational states of the I²C bus

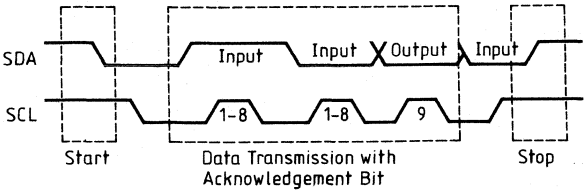


Figure 1

Timing conditions for the I²C bus (high-speed mode)

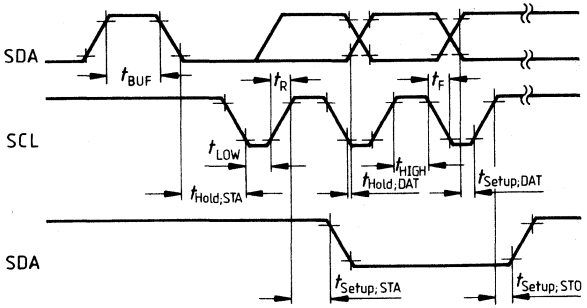


Figure 2

t_{BUF}	$t > t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{Hold;\,STA}$	$t > t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 µs	Clock LOW period
$t_{HIGHmin}$	4 µs	Clock HIGH period
$t_{Setup;\,STA}$	$t > t_{LOWmin}$	Start condition setup time, only valid for repeated start code
$t_{Hold;\,DAT}$	$t > 0$ µs	Data hold time
$t_{Setup;\,DAT}$	$t > 250$ ns	Data setup time
t_r	$t < 1$ µs	Rise time of both the SDA and SCL line
t_f	$t < 300$ ns	Fall time of both the SDA and SCL line
$t_{Setup;\,STO}$	$t > t_{LOWmin}$	Stop condition setup time

Note

All values refer to V_{IH} and V_{IL} level

Infrared Preamplifiers

Type	Ordering Code	Package
TDE 4060	Q67000-A8134	P-DIP-8
TDE 4060 G	Q67000-A8135	similar to P-DSO-8 (SMD)
TDE 4061	Q67000-A8136	P-DIP-14
TDE 4061 G	Q67000-A8137	P-DSO-14 (SMD)

Features

- Very low quiescent current of 650 µA, hence specially suited to battery-powered systems
- Supply voltage 4 V to 6.5 V
- Good ambient light suppression
- External circuitry needs no inductors
- Broad frequency range up to 200 kHz
- Output signal demodulated/non-demodulated, as required
- Temperature range from −40 to +110 °C

Functional Description

The digital signals picked up by an infrared sensor diode must be amplified and demodulated if necessary. This is done by the IC TDE 4061 with integrated demodulator or TDE 4060 without demodulator. Thus their application possibilities include the full range of infrared signal transmission, in particular automotive, industrial and entertainment electronics.

The use of fast bipolar technology enables the processing of high frequencies with low current consumption. Furthermore, the number of external components used could greatly be reduced in comparison with previous design concepts.

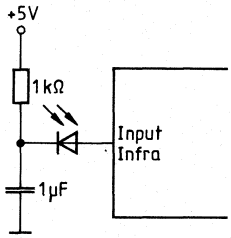
Functional Description and Application Notes

Dimensioning and Design

The ICs are suitable for applications in all infrared systems. The optimum external circuitry varies according to the chosen carrier frequency.

Infrared Sensor Diode

The cathode of this diode is connected to the positive supply (e.g. the +5 V supply to the IC). This means that any variation on this line will be conducted across the diode's junction capacitance to the input. It is therefore recommended to insert an RC lowpass network between the positive rail and the cathode of the diode.



Input Infra

The high-impedance input requires driving currents in the nanoampere range. It is therefore recommended to place the anode of the infrared diode as close as possible to the input.

Capacitor C_S

Due to C_S, the preamplifier has an RC highpass characteristic. But the capacitor C_S also has an effect in conjunction with C_{REG} and the double-T network. Above all, the overshoot behavior is influenced by the combination of the external components. The following two combinations are indicators for a useful infrared system:

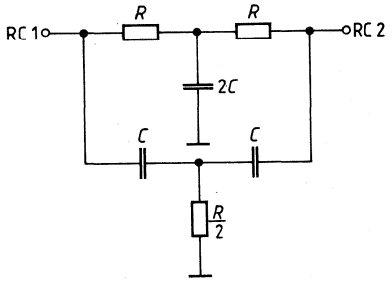
Carrier frequency approx. 30 kHz yields $C_S = 100$ nF
Carrier frequency approx. 120 kHz yields $C_S = 10$ nF

Capacitor C_{REG}

The gain of the preamplifier is adjustable; the greater the HF input signal, the more the gain is attenuated. C_{REG} determines the time constant. Experience shows 470 nF to be appropriate when bi-phase codes are used (e.g. in TV). In the case of signal codes with no advance setup signal, C_{REG} can be reduced to approx. 10 nF. Low capacitances lead to the risk of circuit oscillating.

Double-T network between RC1 and RC2

The inclusion of a double-T filter has proved to be the best solution in all applications. The cutoff frequency is given by the following formula: $\omega_{CO} = \frac{1}{RC}$



The cutoff frequency must be identical to the infrared carrier frequency and can be determined by various combinations of R and C. But the maximum value of R must not exceed 100 kΩ, otherwise the voltage drop in the dc path will be too large. If the circuit oscillates the gain should be reduced by trying lower values of R.

Output

The output is an open collector. In its conducting state, the output transistor carries a maximum collector current of 1 mA. To reduce the risk of oscillations due to feedback from the output to the input, the collector current should be held as low as possible. If the collector current is kept below 200 µA, oscillation will be almost impossible in even the worst case PCB layout. Long PCB tracks may need a decoupling capacitor to ground at the output.

Miscellaneous

The pin configuration was chosen such that any possible cross-talk between critical pins is kept to a minimum. This principle should also be kept in mind when designing the layout. A decoupling capacitor should be considered for the power supply, especially because of the current swings generated at the output.

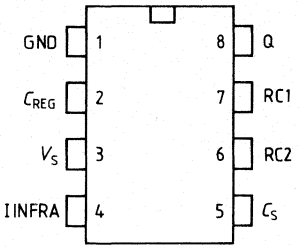
TDE 4061

Demodulating capacitance C_D

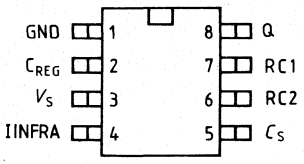
Pin C_D and D/ND remain unconnected if the same form of signal is required at the output as at the input. To prevent the carrier frequency from appearing at the output, the signal must be demodulated. This is achieved by grounding pin D/ND and connecting a capacitor between pin C_D and the ground rail. Values between 100 pF and 1 nF are appropriate, depending on the transmitted code.

Pin Configurations
(top view)

TDE 4060



TDE 4060 G

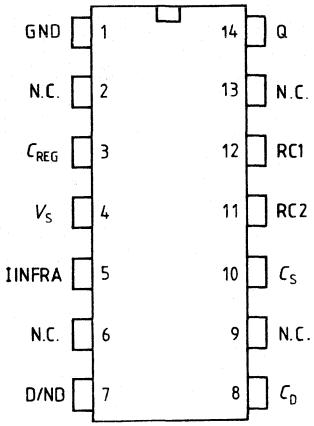


Pin Description

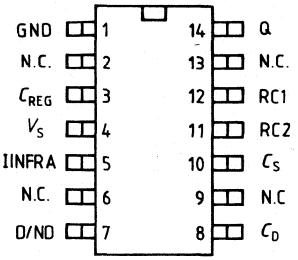
Pin	Symbol	Function
1	GND	Ground
2	C_{REG}	Time constant for gain attenuation
3	V_S	Supply voltage
4	I INFRA	Input INFRA
5	C_S	Time constant for ambient light adjustment
6 7	RC2 RC1	} Bandpass
8	Q	Output

Pin Configurations
(top view)

TDE 4061



TDE 4061 G



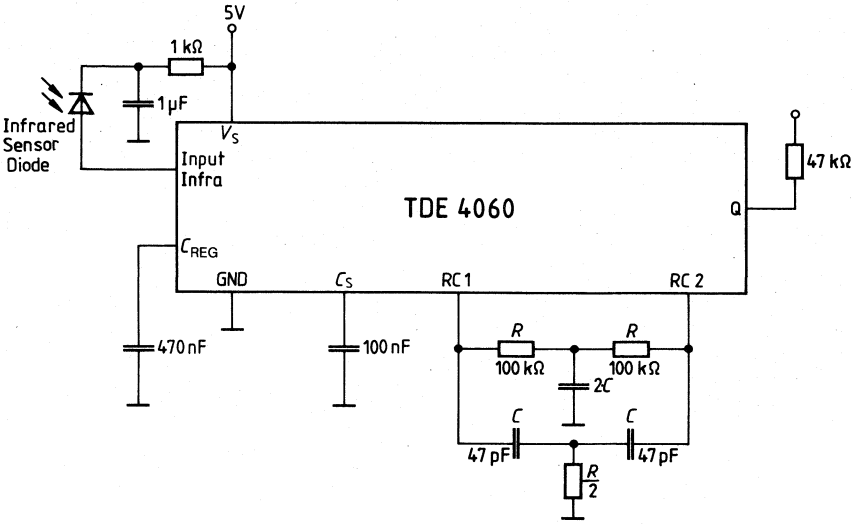
Pin Description

Pin	Symbol	Function
1	GND	Ground
2	N.C.	Not connected
3	C_{REG}	Time constant for gain attenuation
4	V_S	Supply voltage
5	I INFRA	Input Infrared
6	N.C.	Not connected
7	D/ND	Changeover demodulator
8	C_D	Time constant for demodulator
9	N.C.	Not connected
10	C_S	Time constant for ambient adjustment
11 12	RC2 RC1	} Bandpass
13	N.C.	Not connected
14	Q	Output

Application Example

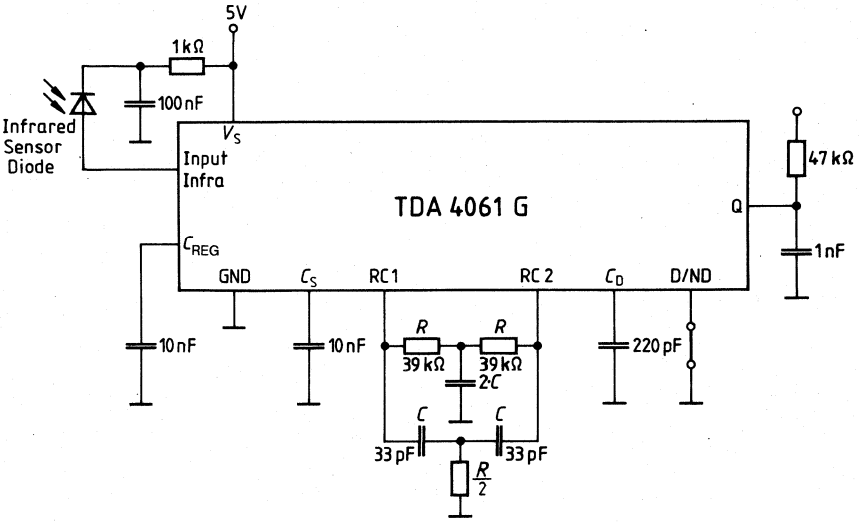
TV remote control with biphase code

Carrier frequency approx. 30 kHz



Electronic Doorkey

Carrier frequency approx. 120 kHz; output signal demodulated



Circuit Description

In addition to the desired signal, an infrared sensor diode usually receives the infrared spectrum of incident daylight, the 100 Hz line hum of light bulbs and portions from the spectrum of fluorescent tubes.

The current sink shown in the block diagram drains the unwanted low frequency diode currents and at the same time stabilizes the operating point at the input of the low-noise preamplifier to approx. 1.4 V. The capacitance of C_S must be tuned to the carrier frequency of the infrared signal.

In the low-noise preamplifier the signal is sufficiently amplified to provide the bandpass filter with a suitable amplitude. The gain of the low-noise preamplifier is regulated in accordance with the input amplitude. When the signal amplitude is larger than the interference amplitude (e.g. fluorescent light), this type of gain control prevents the interference amplitude alone from overdriving the amplifier and "swallowing up" the useful signal. It is therefore possible (with limited sensitivity) to evaluate distorted signals as well.

The bandpass filter following the low-noise preamplifier improves the signal-to-noise ratio of the signal. The edge jitter of the output signal is therefore reduced. The external RC combination should include bandstop characteristics and a dc current path. The cutoff frequency of the external RC combination is identical to the carrier frequency of the useful signal.

The driver includes an open collector output, which is high in the absence of an input signal.

For TDE 4061

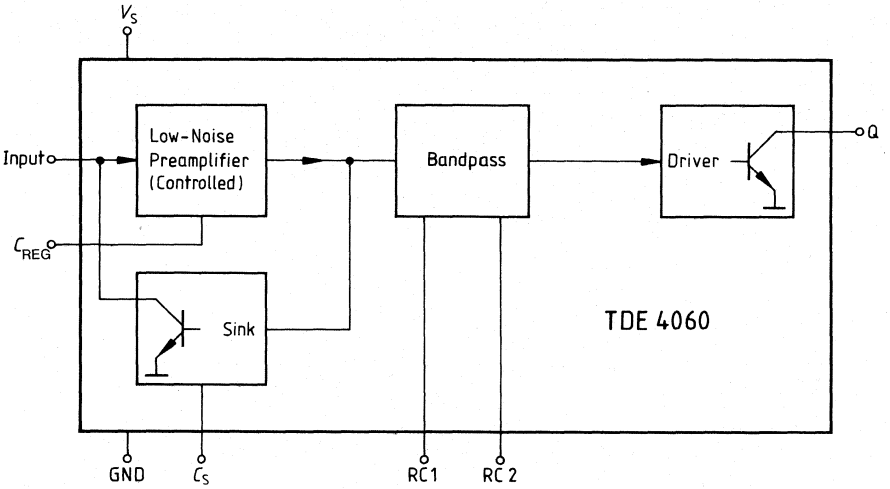
The demodulator charges or discharges capacitor C_D with constant currents. The capacitor is charged when the signal is present. When the switching threshold at C_D is exceeded, the driver output is set to Low. For interference-resistant operation, capacitor C_D is chosen such that one of the output bits switches after half the number of carrier pulses.

It is possible to select between demodulated or non-demodulated output signals. The selection "demodulated – non-demodulated" is programmed via the input D/ND.

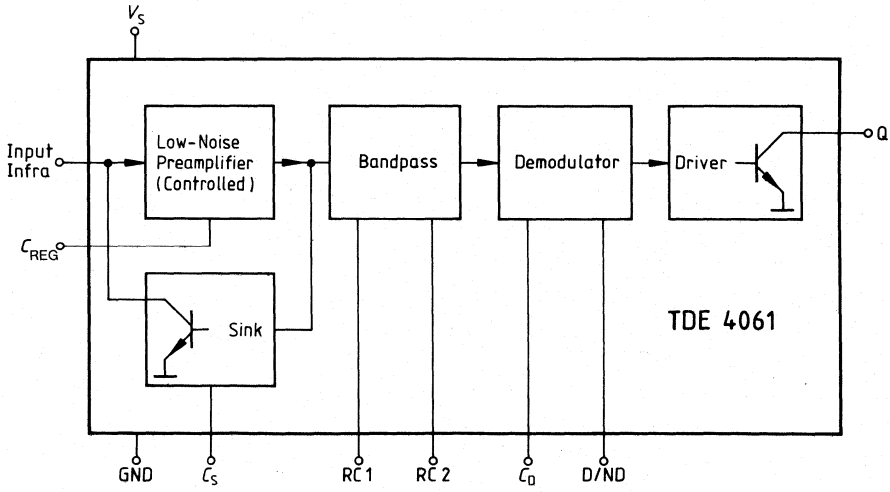
When the input D/ND is not connected and the pin for capacitor C_D is left open, the non-demodulated signal is present at the output. For generating demodulated signals, D/ND should be tied to ground and pin "C_D" connected.

Block Diagrams

TDE 4060



TDE 4061



Maximum Ratings

$T_A = -40$ to $+110$ °C

Description		Symbol	min	max	Unit
Supply voltage		V_S	−0.3	7	V
Input Infra C_S, C_D, C_{REG}		I_{Infra} $I_{CS, CD, CREG}$		10 10	mA mA
D/ND (TDE 4061) RC1, RC2		$V_{D/ND}$ $V_{RC1, RC2}$	−0.3 −0.3	V_S V_S	V V
Output		V_Q I_Q	−0.3 0	7 3	V mA
Storage temperature range		T_{stg}	−40	125	°C
Thermal resistance system – air for TDE 4060	P-DIP-8 P-DSO-8	$R_{th\ SA}$ $R_{th\ SA}$		100 180	K/W K/W
system – air for TDE 4061	P-DIP-14 P-DSO-14	$R_{th\ SA}$ $R_{th\ SA}$		65 125	K/W K/W

Operating Range

Supply voltage	V_S	4	6.5	V
Current into sink at input Infra	I_{sink}	0	2.0	mA
Input voltage $Z_{i\ Gen} < 100\ \Omega$	V_{Infra}	0.6	600	mV_{rms}
Frequency range (for carrier operation)		20	200	kHz
Ambient temperature	T_A	−40	110	°C

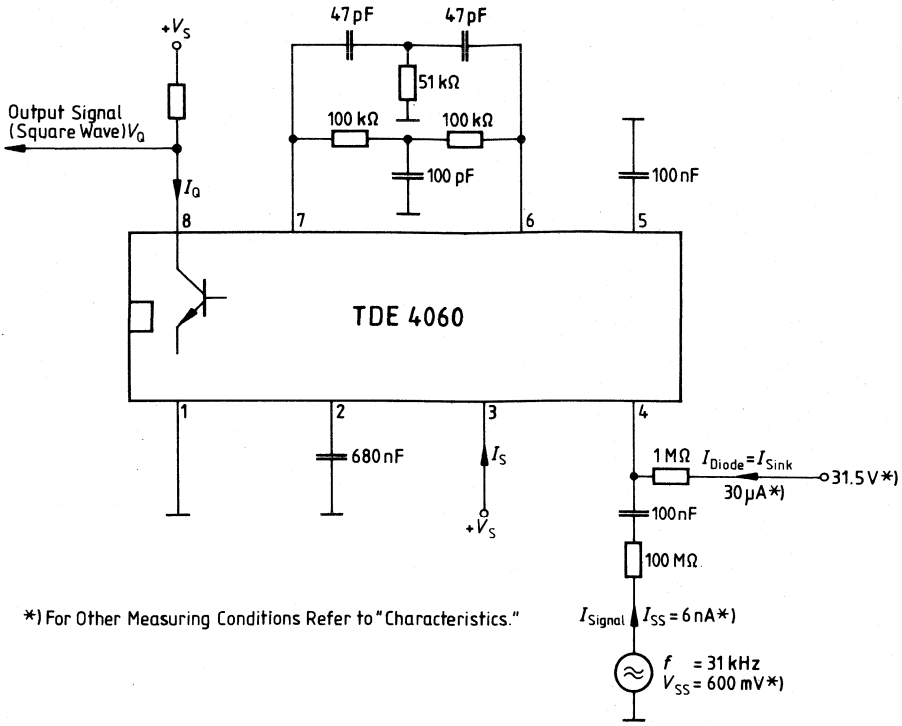
Characteristics

$V_S = 4$ V to 6.5 V
$T_A = -40$ °C to +110 °C

Description	Symbol	Measurement condition	min	typ	max	Unit
Current consumption	I_S	Open output; $I_Q = 0$ mA			650	µA
Input sensitivity for guaranteed output signal $T_A = -40$ °C to +70 °C	I_{signal}	Diode dc ($I_{Diode} = I_{sink}$) $I_{Diode} < 1$ µA		1.3		nA_{pp}
		$I_{Diode} < 10$ µA		3.4		nA_{pp}
		$I_{Diode} < 30$ µA	6.0			nA_{pp}
		$I_{Diode} < 100$ µA	12			nA_{pp}
		$I_{Diode} < 1000$ µA	15			nA_{pp}
Input sensitivity for guaranteed output signal $T_A = 70$ °C to +85 °C	I_{signal}	Diode dc ($I_{Diode} = I_{sink}$) $I_{Diode} < 1$ µA		8		nA_{pp}
		$I_{Diode} < 10$ µA		11		nA_{pp}
		$I_{Diode} < 30$ µA		13		nA_{pp}
		$I_{Diode} < 100$ µA		16		nA_{pp}
		$I_{Diode} < 1000$ µA		25		nA_{pp}
Switch-over input D/ND output demodulated TDE 4061 output non-demodulated TDE 4060	 $-I_{D/ND}$ $I_{D/ND}$	 $0 < V_{D/ND} < 0.4$ V $1\text{ V} < V_{D/ND} < V_S$		 10	 1	 µA[1)] mA
Output current (output High)	I_Q	$0 < V_Q < 7$ V			10	µA
Output voltage (output Low)	V_Q	$0 < I_Q < 1$ mA			0.4	V

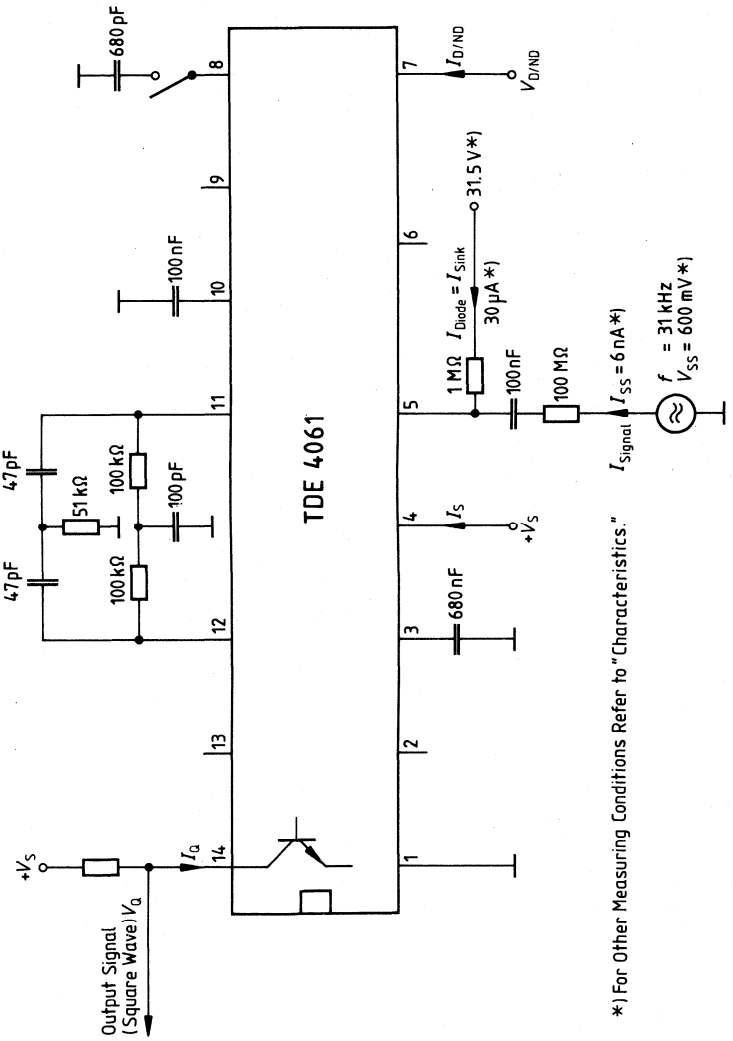
[1)] For TDE 4061: D/ND is not connected for non-demodulated output, i.e. $I_{D/ND} = 0$.

Measurement Circuit



*) For Other Measuring Conditions Refer to "Characteristics."

Measurement Circuit



*) For Other Measuring Conditions Refer to "Characteristics."

Miscellaneous ICs

MOS IC

Type	Ordering Code	Package
SLE 43215 P/SH 100	Q67120-C154	P-DIP-40

Brief Description[1)]

The SLE 43215 P/SH 100 MOS integrated circuit is a combination of the SLE 43215 single-chip microcomputer and a special SH 100 ROM program to form a heating controller that is governed by the time of day and weather conditions.

Controllers of this kind are widely used to save energy in the heating installations of buildings. They control the temperature of the hot water that is circulated, this being performed as a function of changing outdoor temperatures to produce an indoor temperature that is very constant.

Furthermore, the heating energy is fed according to the individual times of use of a building, i.e. the supply temperature is reduced from the normal heating level by a timing program.

Conventional, temperature-dependent analog heating controllers with an automatic timer that is programmed on a daily or weekly basis control the temperature of the hot water that is circulated or the boiler temperature of a central-heating installation as a function of outdoor temperature and the time of day. They can produce savings in heating costs of as much as 20%.

The relationship between outdoor temperature and the temperature of the circulated hot water is given by what is called a heating characteristic. This can be set on the heating controller and the user or fitter of the heating system will adjust it according to the technically based heating requirements of a building. If this heating curve is properly set, the indoor temperature will remain constant despite fluctuations in outdoor temperature.

Through the use of the SLE 43215 P/SH 100 microcomputer heating controllers can be markedly improved in point of:

- Accurate control algorithm
- Self-monotoring
- Attractive price/performance ratio
- Enhanced ease of use

1) An application note describes hardware and software of a complete controller as well as its operation. Technical data on the SLE 43215 P/SH 100 can be obtained from the data sheet of the SAB 80215/SLE 43215.

Functions of the Heating Controller

Combination with the program of the SLE 43215 P/SH 100 produces a heating-controller circuit with the following features:

- programmed temperature reduction over a period of seven days
- two reduction periods daily
- setting of the slope of the heating characteristic
- setting of indoor temperature through a parallel shift of the heating curve
- setting of the reduction temperature
- automatic timing
- protection of the timer (day/hrs/mins) and all input data against power failure for up to six hours
- device for measuring and indicating two temperature values with accuracy of at least ± 2 K (standard DIN 32729)
- monitoring of the sensors for line breaks and shorts (alarm signal, self-protection)
- control with adjustable integration response
- simple and safe operation
- requirement-based pump control

Features of the SLE 43215 P/SH 100

The SLE 43215 P/SH 100 comprises a complete, standard 8-bit μC and various peripheral circuits on a single chip. The core of the computer corresponds to the SAB 8021, but with 2 Kbytes of ROM and 128 bytes of RAM.

The periphery integrated into the chip, which is of particular importance for the heating controller, primarily consists of the following:

- 8-bit A/D converter with three multiplexed inputs
- timer
- multiplexed interface for 20 input functions, e.g. keys
- multiplexed interface for 40 input functions, e.g. four 7-segment and 12 LED displays
- standby supply of 5 mA for RAM, timer, and other functions
- timer/counter for 4, 8 and 12 bits

Figure 1
SLE 43215, Interfacing with Periphery

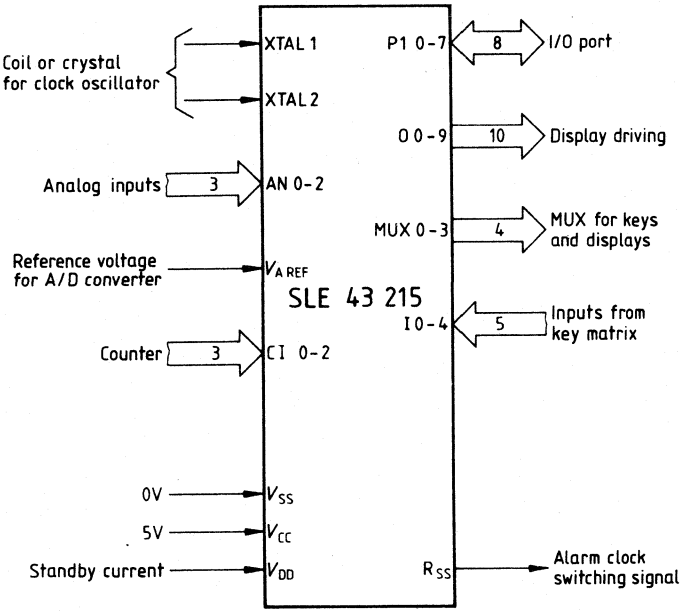
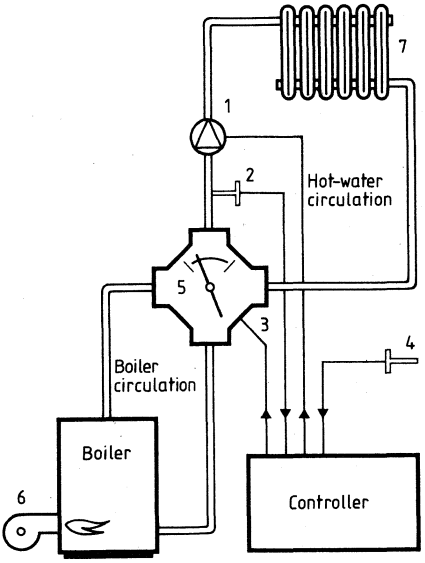


Figure 2
Schematic Diagram of the Lines of Action of the Controller in an Oil Heating System



1 Pump
2 Circulation sensor
3 Mixer motor
4 Outdoor-temperature sensor
5 Mixer valve
6 Burner
7 Radiator

Figure 3
Monovalent Heating Controller with SLE 43215 P/SH 100 (Block Diagram)

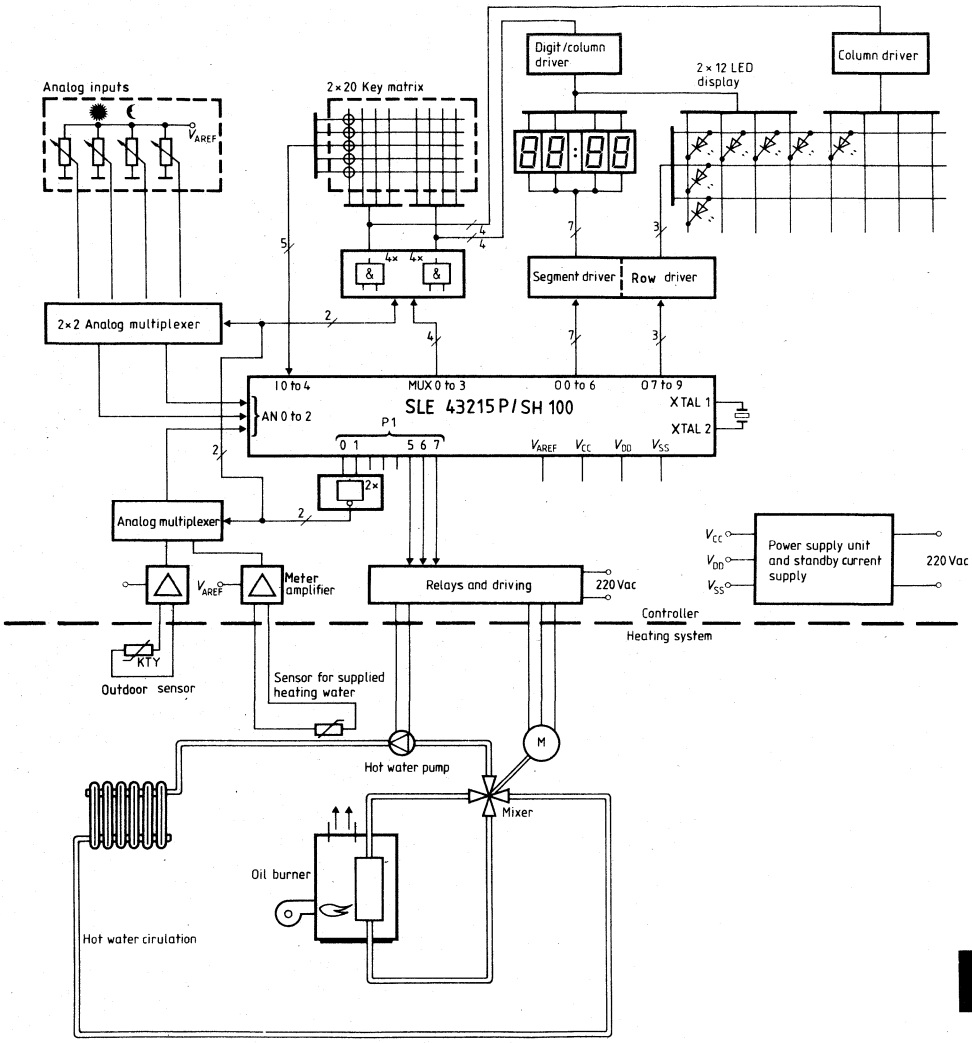


Figure 4 shows an example of a weekly program in schematic form. On each day of the week two normal heating phases are provided for. Between two normal heating phases there is a reduction phase during which the circulation temperature is reduced to save energy. The timing program consists of a sequence of stored switching points, set in increments of 10 min, at which the circulation temperature is increased or reduced. The programming of a complete week's program therefore calls for the entry of 4 x 7 = 28 switching points.

Figure 4

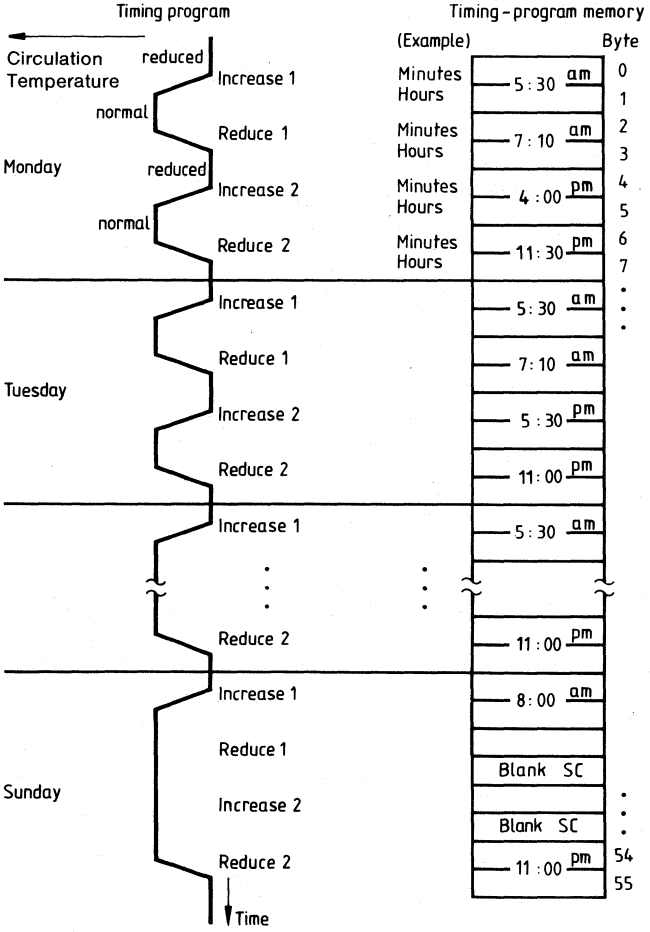


Figure 5
Description of the Program Structure (Outline)
Program Flowchart of the Heating-Controller Software

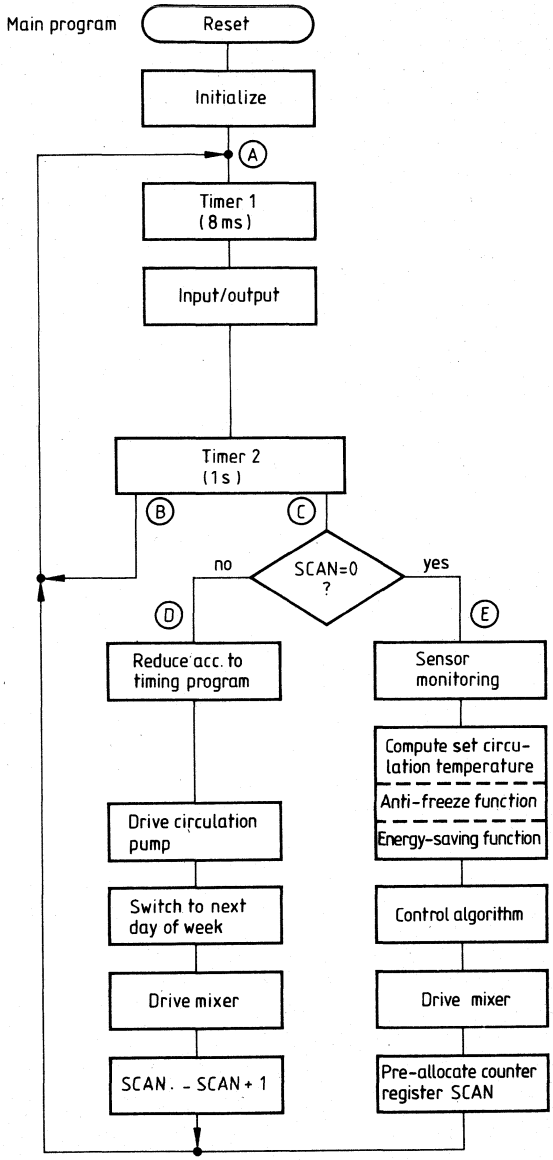
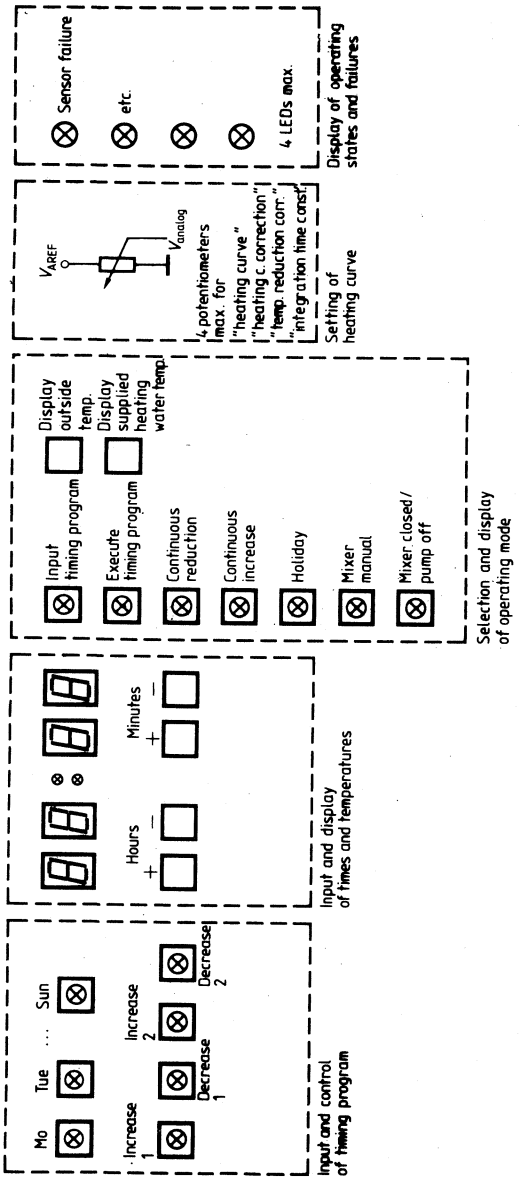


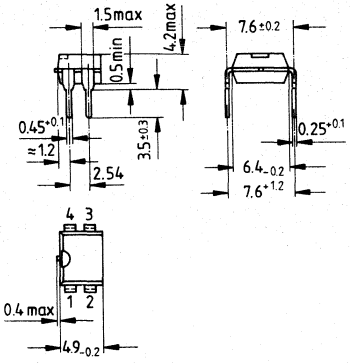
Figure 6
Schematic Diagram of the Control Panel of the Heating Controller



Package Outlines, Packaging Tubes

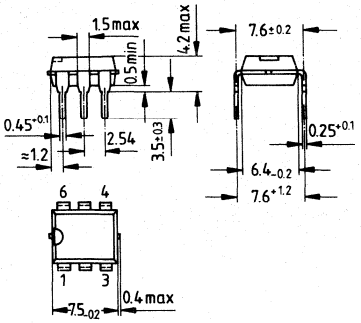
Package Outlines

Plastic Dual-in Line Package, P-DIP-4
20 A 4 DIN 41866



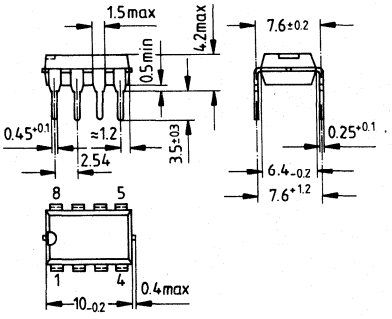
Approx. weight 0.5 g

Plastic Dual-in-Line Package, P-DIP-6
20 A 6 DIN 41866



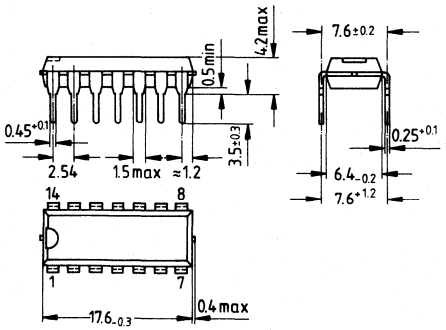
Approx. weight 0.7 g

Plastic Dual-in-Line Package, P-DIP-8
20 A 8 DIN 41870 T9



Approx. weight 0.7 g

Plastic Dual-in-Line Package, P-DIP-14
20 A 14 DIN 41870 T9

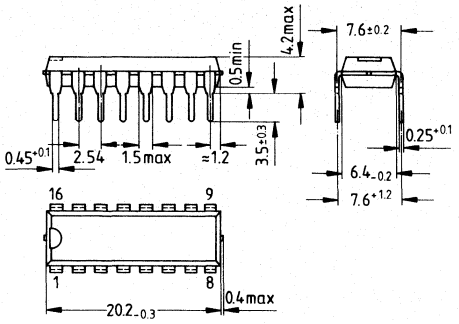


Approx. weight 1.1 g

Dimensions in mm

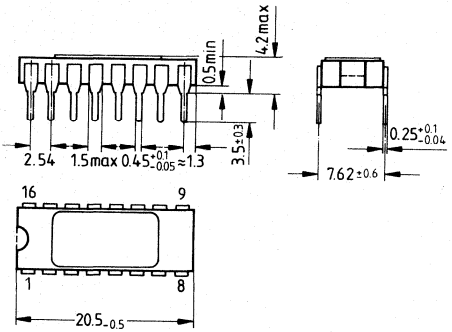
Package Outlines

Plastic Dual-in-Line Package, P-DIP-16
20 A 16 DIN 41870 T9



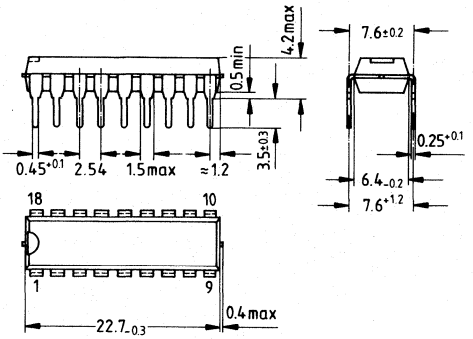
Approx. weight 1.2 g

Ceramic Dual-in-Line Package, C-DIP-16
20 A 16 DIN 41870 T9



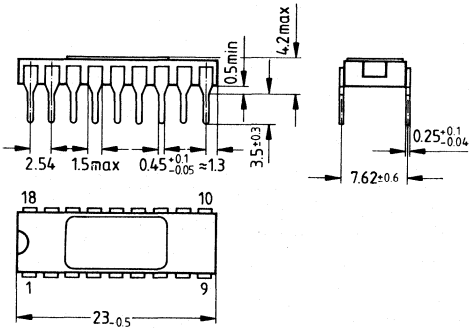
Approx. weight 1.4 g

Plastic Dual-in-Line Package, P-DIP-18
20 A 18 DIN 41870 T9



Approx. weight 1.3 g

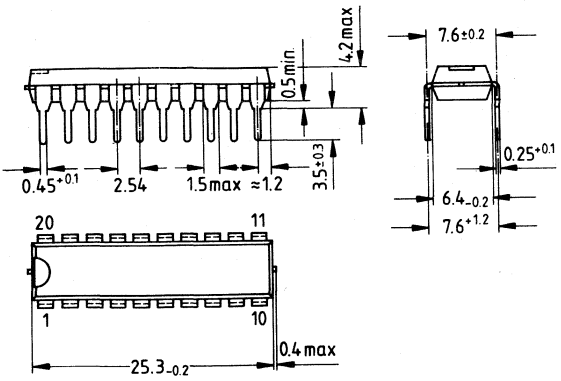
Ceramic Dual-in-Line Package, C-DIP-18
20 A 18 DIN 41870 T9



Approx. weight 1.7 g

Dimensions in mm

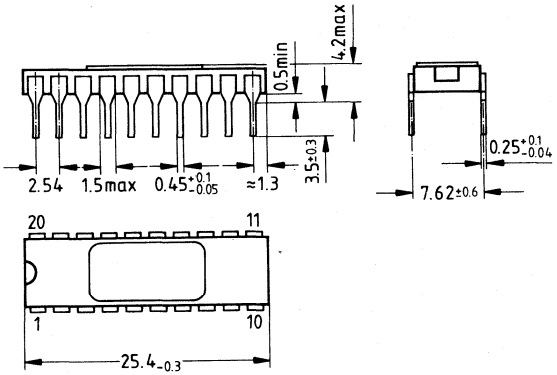
Plastic Dual-in-Line Package, P-DIP-20
20 A 20 DIN 41870 T9



Approx. weight 1.5 g

Ceramic Dual-in-Line Package, C-DIP-20
20 A 20 DIN 41870 T9

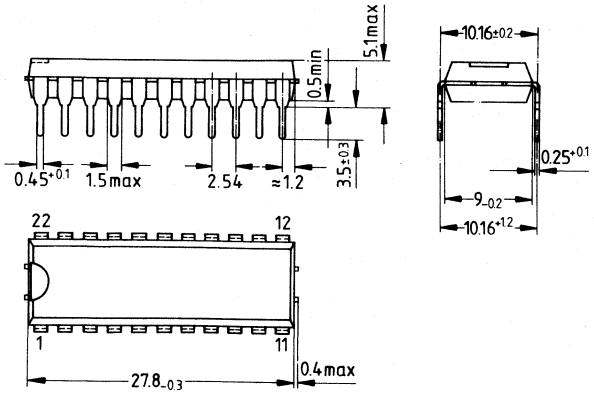
Dimensions in mm



Approx. weight 1.7 g

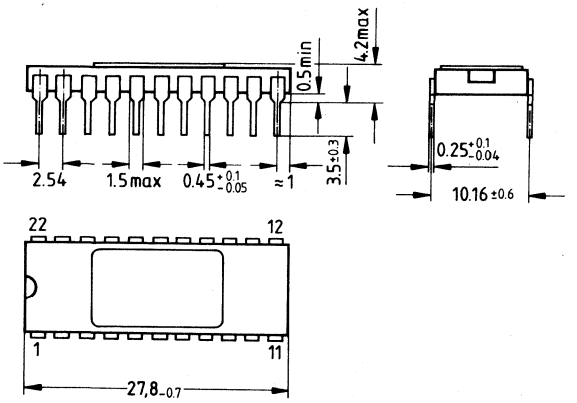
Package Outlines

Plastic Dual-in-Line Package, P-DIP-22
20 D 22 DIN 41870 T11



Approx. weight 2.1 g

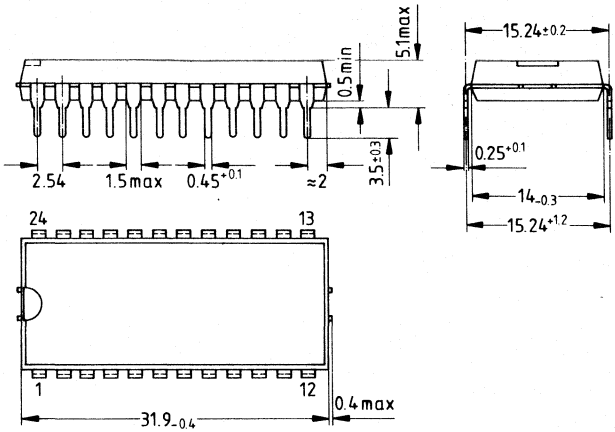
Ceramic Dual-in-Line Package, C-DIP-22
20 D 22 DIN 41870 T11



Dimensions in mm

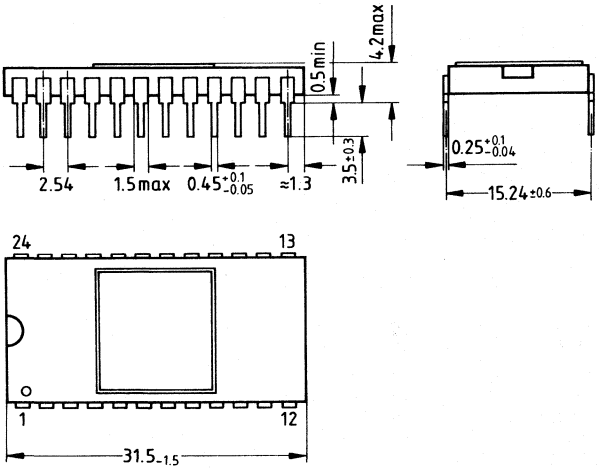
Approx. weight 2.5 g

Plastic Dual-in-Line Package, P-DIP-24
20 B 24 DIN 41870 T10



Approx. weight 2.5 g

Ceramic Dual-in-Line Package, C-DIP-24
20 B 24 DIN 41870 T10

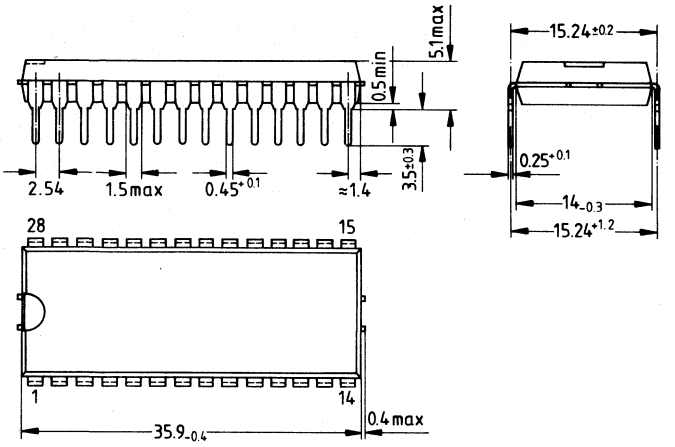


Dimensions in mm

Approx. weight 3 g

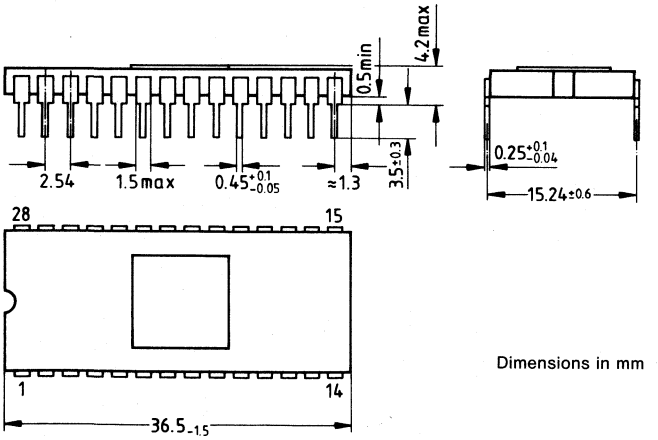
Package Outlines

Plastic Dual-in-Line Package, P-DIP-28
20 B 28 DIN 41870 T10



Approx. weight 3 g

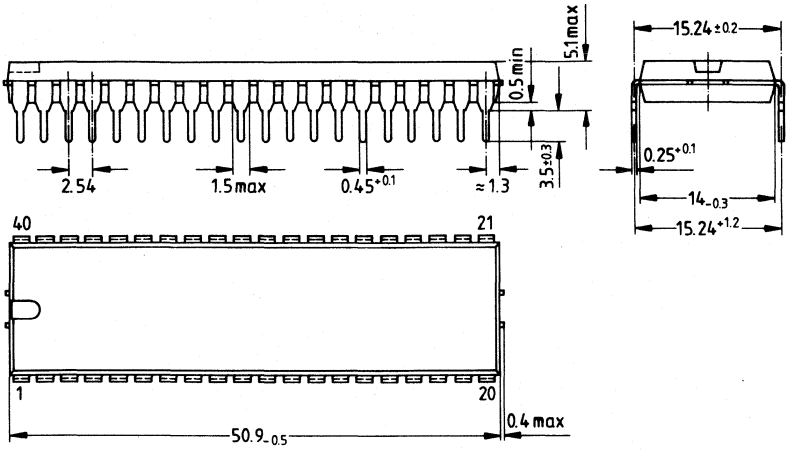
Ceramic Dual-in-Line Package, C-DIP-28
20 B 28 DIN 41870 T10



Dimensions in mm

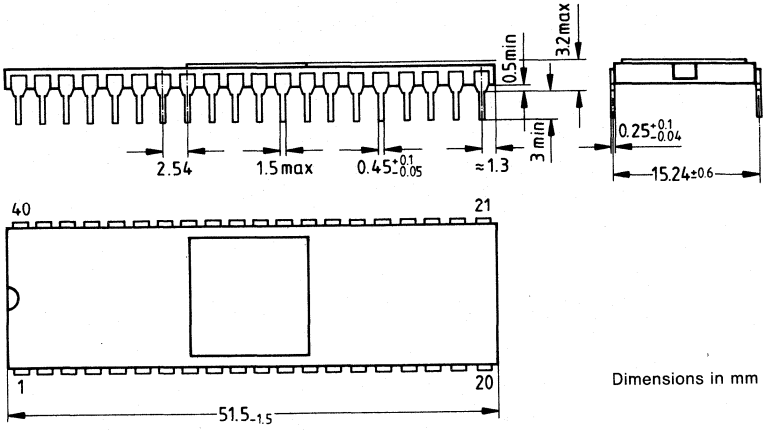
Approx. weight 3.5 g

Plastic Dual-in-Line Package, P-DIP-40
20 B 40 DIN 41870 T10



Approx. weight 5.9 g

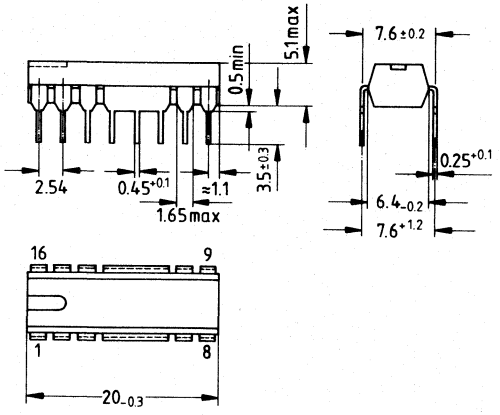
Ceramic Dual-in-Line Package, C-DIP-40
20 B 40 DIN 41870 T10



Dimensions in mm

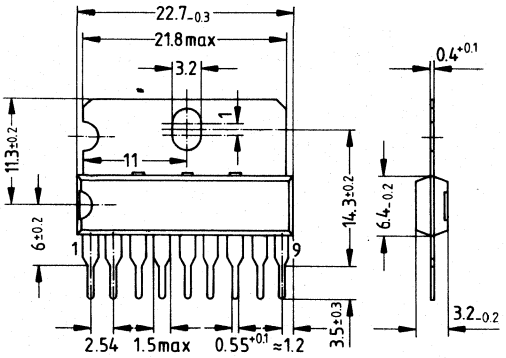
Approx. weight 6.8 g

Plastic Dual-in-Line Package for Power Applications, P-DIP-16 L10
20 A 16 DIN 41870 T9



Approx. weight 1.1 g

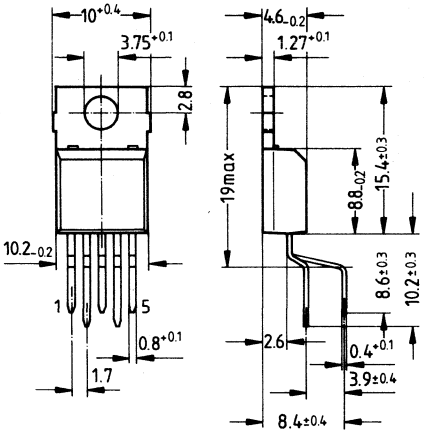
Plastic Single-in-Line Package, P-SIP-9



Approx. weight 1.9 g

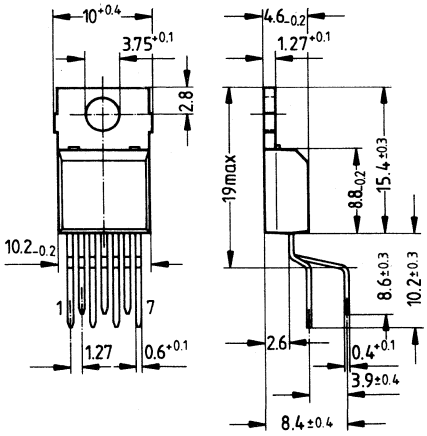
Dimensions in mm

Plastic Power Package, P-T66-5-H
(similar to TO-220)



Approx. weight 2.1 g

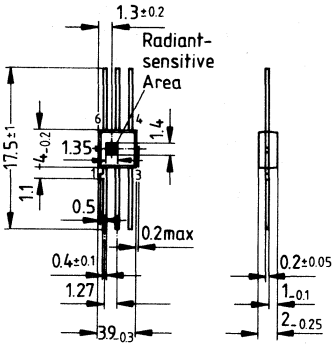
Plastic Power Package, P-T66-7-H
(similar to TO-220)



Dimensions in mm

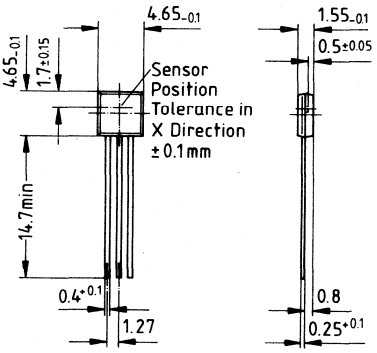
Approx. weight 2.1 g

Plastic Minipack, P-MIP-6



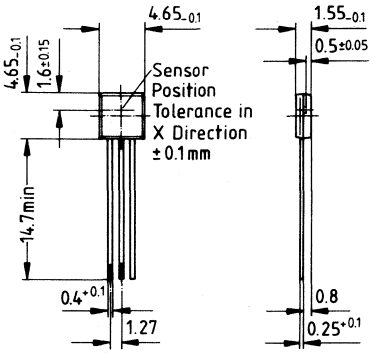
Approx. weight 0.1 g

Plastic Single-in-Line Package, P-SSO-3
(Small Outlines)
(e.g. TLE 4901 F)



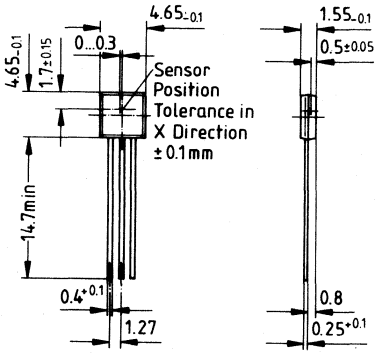
Approx. weight 0.1 g

Plastic Single-in-Line Package, P-SSO-3
(Small Outlines)
(e.g. TLE 4902 F)



Approx. weight 0.1 g

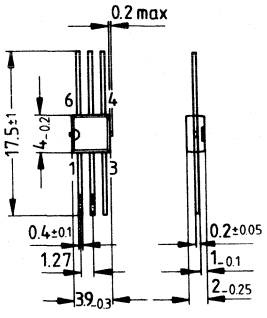
Plastic Single-in-Line Package, P-SSO-3
(Small Outlines)
(e.g. TLE 4903 F)



Approx. weight 0.1 g

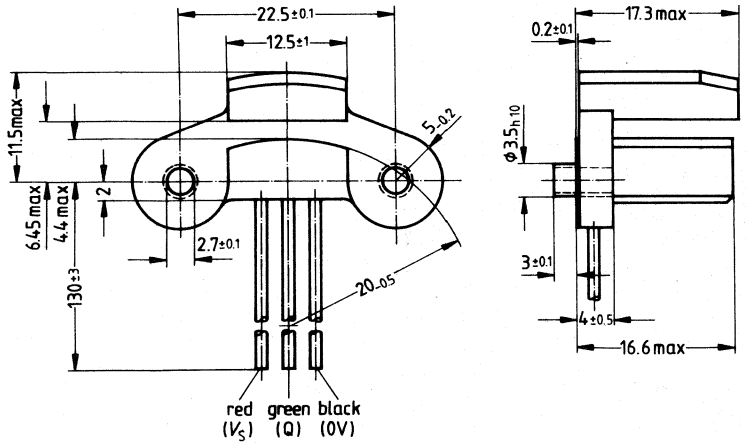
Dimensions in mm

Plastic Minipack, P-MIP-6



Approx. weight 0.1 g

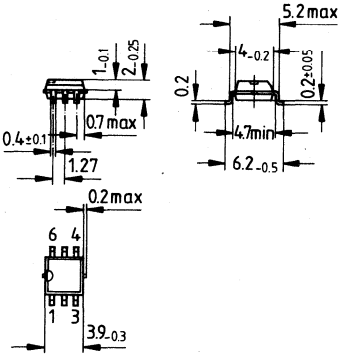
Special Package



Approx. weight 8.5 g

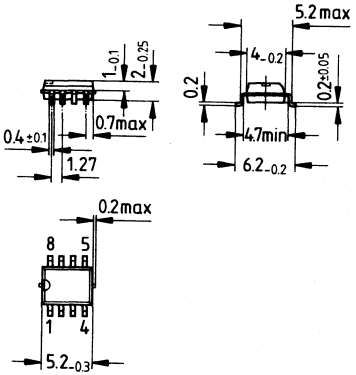
Dimensions in mm

Miniature Plastic Dual-in-Line Package,
P-MIP-6-G (SMD)
(Small Outlines)
(similar to P-DSO-6)
24 A 6 DIN 41870 T16



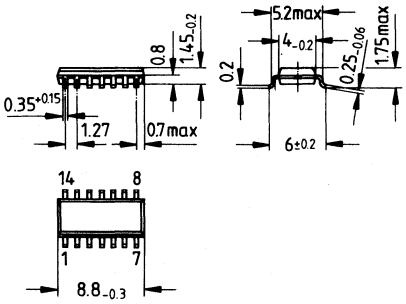
Approx. weight 0.1 g

Miniature Plastic Dual-in-Line Package,
P-MIP-8-G (SMD)
(Small Outlines)
(similar to P-DSO-8)
24 A 8 DIN 41870 T16



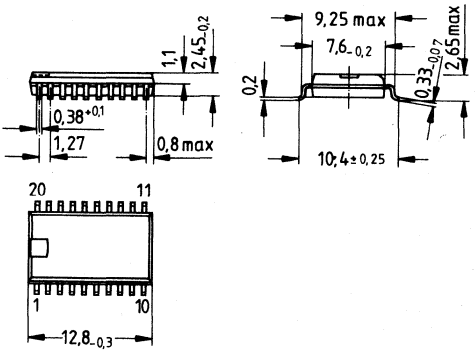
Approx. weight 0.15 g

Miniature Plastic Dual-in-Line Package,
P-DSO-14 (SMD)
(Small Outlines)
24 A 14 DIN 41870 T16



Approx. weight 0.2 g

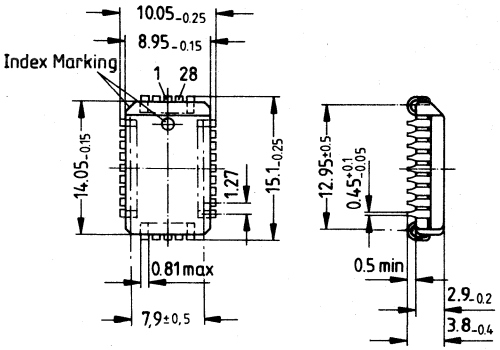
Miniature Plastic Dual-in-Line Package,
P-DSO-20 (SMD)
(Small Outlines)
24 B 20 DIN 41870 T17



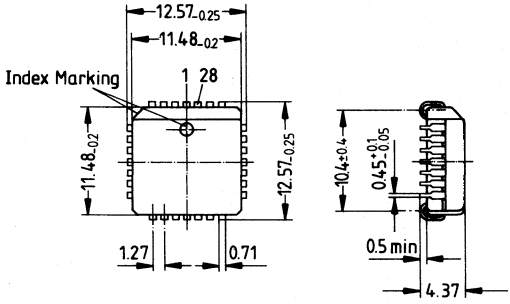
Approx. weight 0.6 g

Dimensions in mm

Plastic-Leaded Chip Carrier, PL-CC-28-R (SMD)

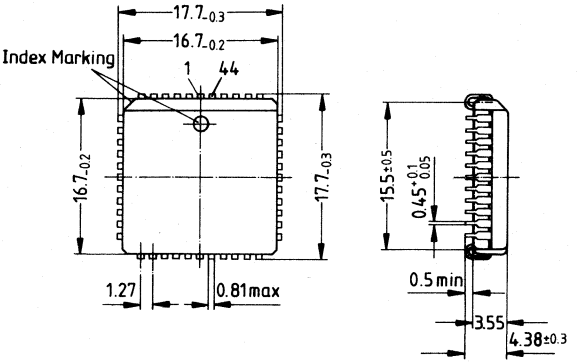


Plastic-Leaded Chip Carrier, PL-CC-28 (SMD)

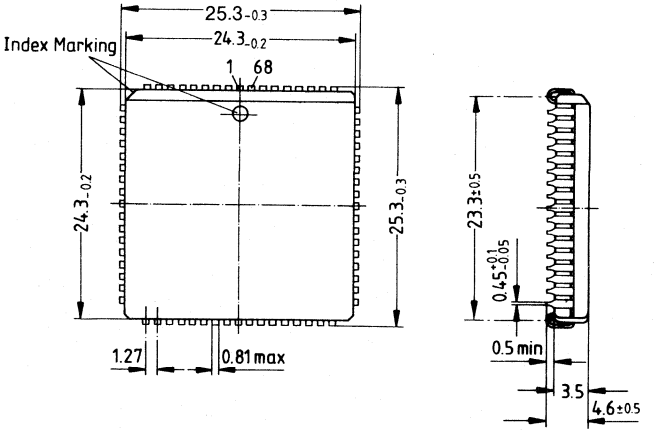


Dimensions in mm

Plastic-Leaded Chip Carrier, PL-CC-44 (SMD)

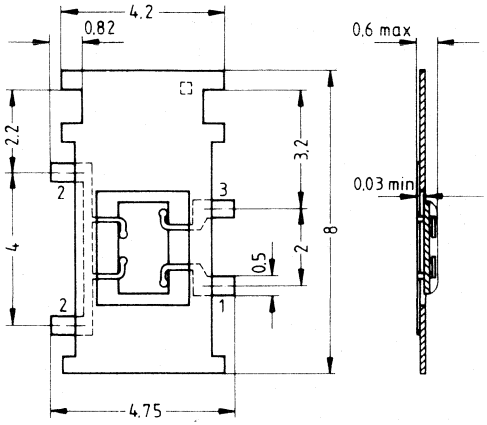


Plastic-Leaded Chip Carrier, PL-CC-68 (SMD)

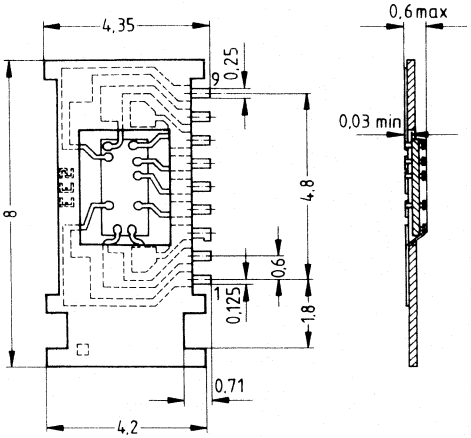


Dimensions in mm

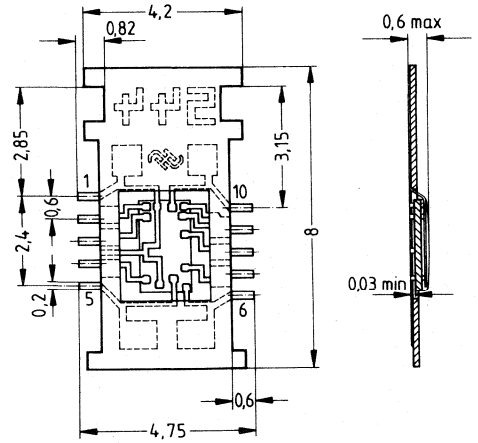
MIKROPACK 8 S, 4 pins, (SMD)
e.g. TLE 4901-K



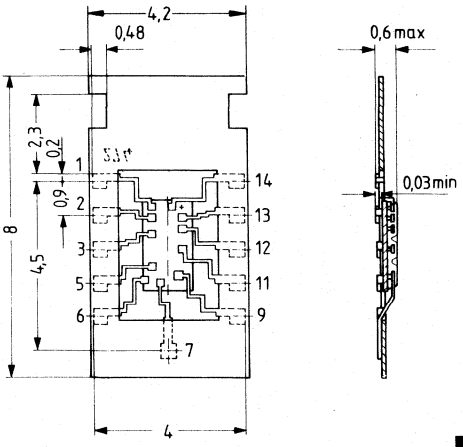
MIKROPACK 8 S, 9 pins, (SMD)
e.g. TLE 4910-K



MIKROPACK 8 S, 10 pins, (SMD)
e.g. TCA 305 K



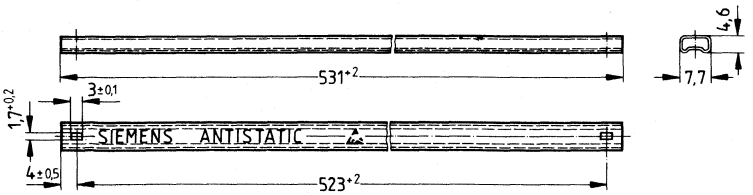
MIKROPACK 8 S, 14 pins, (SMD)
e.g. TCA 205 K



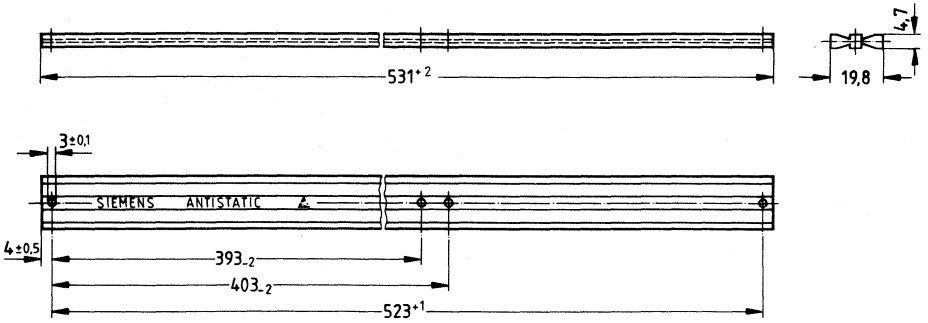
Dimensions in mm

Packaging Tubes

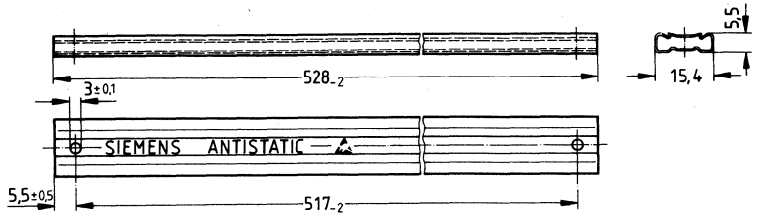
Packages: P-DSO-6; 8; 14; P-MIP-6-G; 8-G



Packages: P-MIP-6; 8



Packages: P-DSO-20

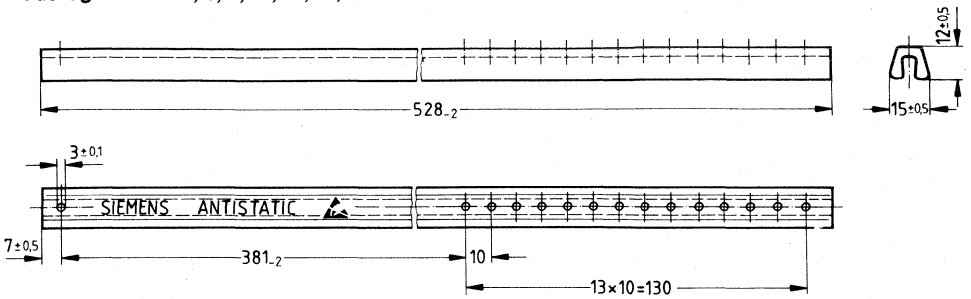


Dimensions in mm

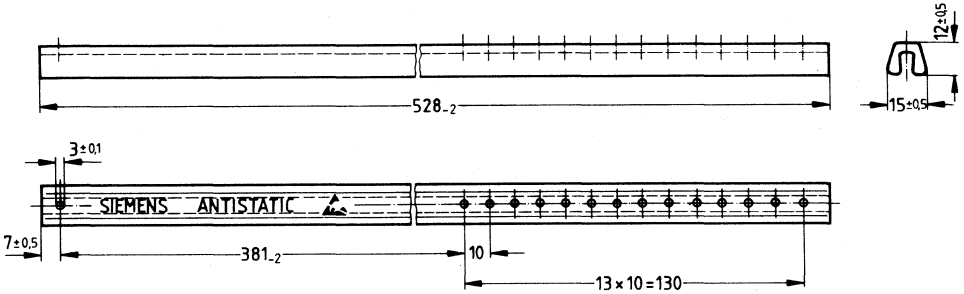
Packaging Tubes

Packaging Tubes

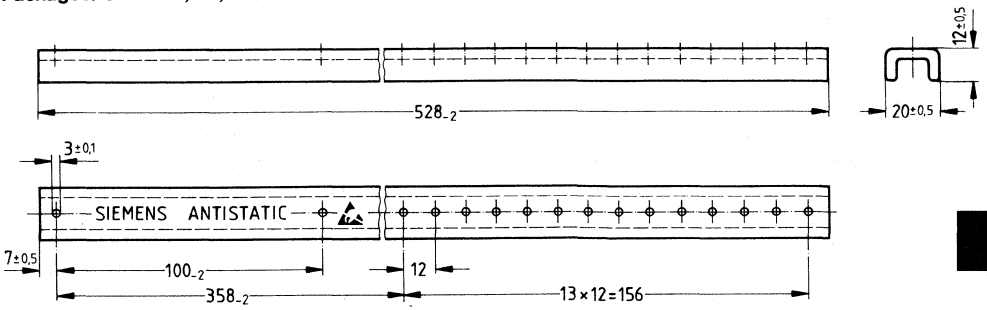
Packages: P-DIP-4; 6; 8; 14; 16; 18; 20



Packages: C-DIP-14; 16; 18; 20



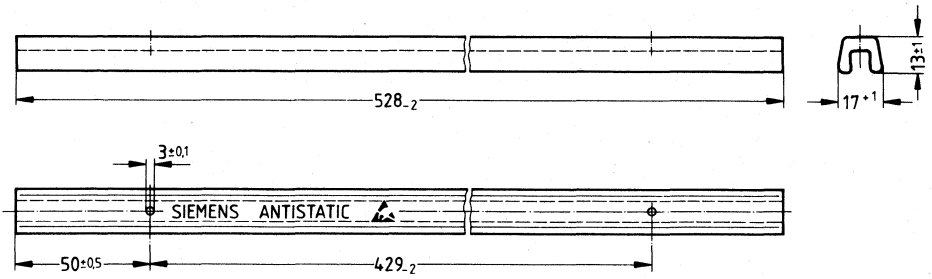
Packages: C-DIP-24; 28; 40; 48



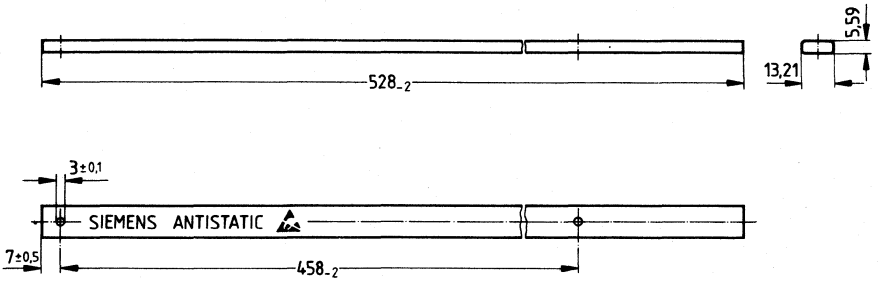
Dimensions in mm

Packaging Tubes

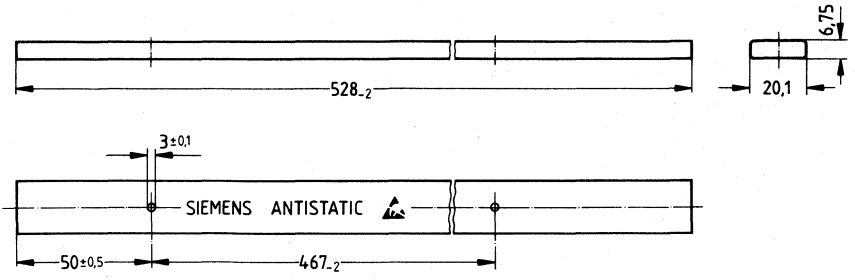
Packages: P-DIP-22



Packages: PL-CC-28



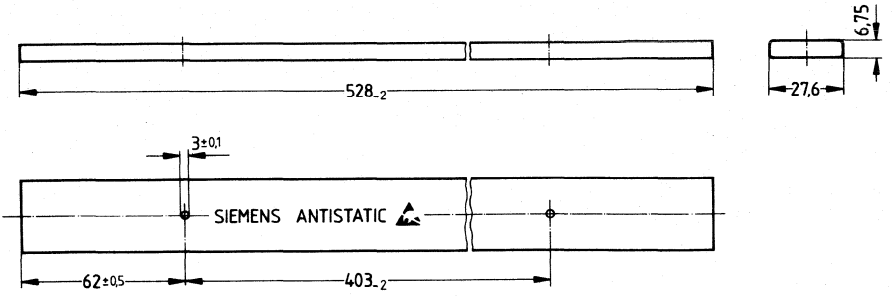
Packages: PL-CC-44



Dimensions in mm

Packaging Tubes

Packages: PL-CC-68



Dimensions in mm

Siemens Worldwide (Addresses)

Siemens AG, Bereich Bauelemente
Balanstraße 73, Postfach 80 17 09, **D-8000 München 80**
☎ (089) 41 44-0 Tx 52 108-0 FAX (089) 41 44-26 89

Siemens Worldwide

Federal Republic of Germany and Berlin (West)

Siemens AG
Salzufer 6–8
1000 Berlin 10
☎ (030) 39 39-1, Tx 1810-278
FAX (030) 3939-2630
Ttx 308190 = sieznb

Siemens AG
Lahnweg 10
Postfach 11 15
4000 Düsseldorf 1
☎ (0211) 399-0, Tx 8581301
FAX (0211) 399-2506

Siemens AG
Rödelheimer Landstraße 5–9
Postfach 111733
6000 Frankfurt 1
☎ (069) 797-0, Tx 414131-0
FAX (069) 797-2253

Siemens AG
Lindenplatz 2
Postfach 105609
2000 Hamburg 1
☎ (040) 282-1, Tx 215584-0
FAX (040) 282-2210

Siemens AG
Am Maschpark 1
Postfach 5329
3000 Hannover 1
☎ (0511) 129-0, Tx 922333
FAX (0511) 129-2799

Siemens AG
Richard-Strauss-Straße 76
Postfach 202109
8000 München
☎ (089) 9221-4380
Tx 529421-19
FAX (089) 9221-4390
Ttx 8985061

Siemens AG
Von-der-Tann-Straße 30
Postfach 4844
8500 Nürnberg 1
☎ (0911) 654-0, Tx 622251
FAX (0911) 654-4064

Siemens AG
Geschwister-Scholl-Straße 24
Postfach 120
7000 Stuttgart 1
☎ (0711) 2076-0, Tx 723941
FAX (0711) 2076-3706

EUROPE

Austria
Siemens Aktiengesellschaft
Österreich
Postfach 326
A-1031 Wien
☎ (0222) 7293-0, Tx 1372-0

Belgium
Siemens S.A.
chaussée de Charleroi 116
B-1060 Bruxelles
☎ (02) 536-2111, Tx 21347

Denmark
Siemens A/S
Borupvang 3
DK-2750 Ballerup
☎ (02) 656565, Tx 35313

Finland
Siemens Osakeyhtiö
PL 8
SF-00101 Helsinki 10
☎ (0) 1626-1, Tx 124465

France
Siemens S.A.
B.P. 109
F-93203 Saint-Denis CEDEX 1
☎ (1) 49223100, Tx 620853

Great Britain
Siemens Ltd.
Siemens House
Windmill Road
GB-Sunbury-on-Thames
Middlesex TW 16 7HS
☎ (09327) 85691, Tx 8951091

Greece
Siemens AE
Paradissou & Artemidos
P.O.B. 61011
GR-15110 Amaroussio
☎ (01) 6864 111

Ireland
Siemens Ltd.
Unit 8–11 Slaney Road
Dublin Industrial Estate
Finglas Road
Dublin 11
☎ (01) 302855, Tx 32547

Italy
Siemens Elettra S.p.A.
Via Fabio Filzi, 29
Casella Postale 10388
I-20100 Milano
☎ (02) 67661, Tx 330261

Netherlands
Siemens Nederland N.V.
Postb. 16068
NL-2500 BB Den Haag
☎ (070) 782782, Tx 31373

Norway
Siemens A/S
Østre Aker vei 90
Postboks 10, Veitvet
N-0518 Oslo 5
☎ (02) 633000, Tx 78477

Portugal
Siemens S.A.R.L.
Avenida Almirante Reis, 65
Apartado 1380
P-1100 Lisboa-1
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